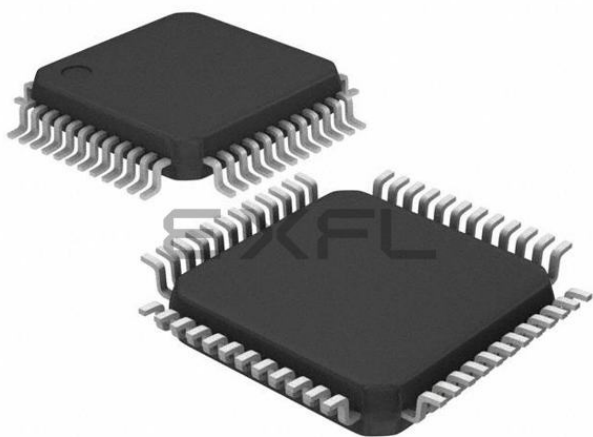




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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	F ² MC-16LX
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, SCI, UART/USART
Peripherals	POR, WDT
Number of I/O	34
Program Memory Size	64KB (64K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90387pmt-gt-111

10. I/O Map

Address	Register Abbreviation	Register	Read/Write	Resource	Initial Value
000000 _H	(Reserved area) *				
000001 _H	PDR1	Port 1 data register	R/W	Port 1	XXXXXXXX _B
000002 _H	PDR2	Port 2 data register	R/W	Port 2	XXXXXXXX _B
000003 _H	PDR3	Port 3 data register	R/W	Port 3	XXXXXXXX _B
000004 _H	PDR4	Port 4 data register	R/W	Port 4	XXXXXXXX _B
000005 _H	PDR5	Port 5 data register	R/W	Port 5	XXXXXXXX _B
000006 _H to 000010 _H	(Reserved area) *				
000011 _H	DDR1	Port 1 direction data register	R/W	Port 1	00000000 _B
000012 _H	DDR2	Port 2 direction data register	R/W	Port 2	00000000 _B
000013 _H	DDR3	Port 3 direction data register	R/W	Port 3	000X0000 _B
000014 _H	DDR4	Port 4 direction data register	R/W	Port 4	XXX00000 _B
000015 _H	DDR5	Port 5 direction data register	R/W	Port 5	00000000 _B
000016 _H to 00001A _H	(Reserved area) *				
00001B _H	ADER	Analog input permission register	R/W	8/10-bit A/D converter	11111111 _B
00001C _H to 000025 _H	(Reserved area) *				
000026 _H	SMR1	Serial mode register 1	R/W	UART1	00000000 _B
000027 _H	SCR1	Serial control register 1	R/W, W		00000100 _B
000028 _H	SIDR1/ SODR1	Serial input data register 1/ Serial output data register 1	R, W		XXXXXXXX _B
000029 _H	SSR1	Serial status data register 1	R, R/W		00001000 _B
00002A _H	(Reserved area) *				
00002B _H	CDCR1	Communication prescaler control register 1	R/W	UART1	0XXX0000 _B
00002C _H to 00002F _H	(Reserved area) *				
000030 _H	ENIR	DTP/External interrupt permission register	R/W	DTP/External interrupt	00000000 _B
000031 _H	EIRR	DTP/External interrupt permission register	R/W		XXXXXXXX _B
000032 _H	ELVR	Detection level setting register	R/W		00000000 _B
000033 _H			R/W		00000000 _B
000034 _H	ADCS	A/D control status register	R/W	8/10-bit A/D converter	00000000 _B
000035 _H			R/W, W		00000000 _B
000036 _H	ADCR	A/D data register	W, R		XXXXXXXX _B
000037 _H			R		00101XXX _B

Address	Register Abbreviation	Register	Read/ Write	Resource	Initial Value
000038 _H to 00003F _H	(Reserved area) *				
000040 _H	PPGC0	PPG0 operation mode control register	R/W, W	8/16-bit PPG timer 0/ 1	0X000XX1 _B
000041 _H	PPGC1	PPG1 operation mode control register	R/W, W		0X000001 _B
000042 _H	PPG01	PPG0/1 count clock selection register	R/W		000000XX _B
000043 _H	(Reserved area) *				
000044 _H	PPGC2	PPG2 operation mode control register	R/W, W	8/16-bit PPG timer 2/ 3	0X000XX1 _B
000045 _H	PPGC3	PPG3 operation mode control register	R/W, W		0X000001 _B
000046 _H	PPG23	PPG2/3 count clock selection register	R/W		000000XX _B
000047 _H to 00004F _H	(Reserved area) *				
000050 _H	IPCP0	Input capture data register 0	R	16-bit input/output timer	XXXXXXXX _B
000051 _H					XXXXXXXX _B
000052 _H	IPCP1	Input capture data register 1	R		XXXXXXXX _B
000053 _H					XXXXXXXX _B
000054 _H	ICS01	Input capture control status register	R/W		00000000 _B
000055 _H	ICS23				00000000 _B
000056 _H	TCDT	Timer counter data register	R/W		00000000 _B
000057 _H					00000000 _B
000058 _H	TCCS	Timer counter control status register	R/W		00000000 _B
000059 _H	(Reserved area) *				
00005A _H	IPCP2	Input capture data register 2	R	16-bit input/output timer	XXXXXXXX _B
00005B _H					XXXXXXXX _B
00005C _H	IPCP3	Input capture data register 3	R		XXXXXXXX _B
00005D _H					XXXXXXXX _B
00005E _H to 000065 _H	(Reserved area) *				
000066 _H	TMCSR0	Timer control status register	R/W	16-bit reload timer 0	00000000 _B
000067 _H			R/W		XXXX0000 _B
000068 _H	TMCSR1		R/W	16-bit reload timer 1	00000000 _B
000069 _H			R/W		XXXX0000 _B
00006A _H to 00006E _H	(Reserved area) *				
00006F _H	ROMM	ROM mirroring function selection register	W	ROM mirroring function selection module	XXXXXXXX1 _B
000070 _H to 00007F _H	(Reserved area) *				
000080 _H	BVALR	Message buffer enabling register	R/W	CAN controller	00000000 _B
000081 _H	(Reserved area) *				
000082 _H	TREQR	Send request register	R/W	CAN controller	00000000 _B

Address	Register Abbreviation	Register	Read/ Write	Resource	Initial Value
0000B0 _H	ICR00	Interrupt control register 00	R/W	Interrupt controller	00000111 _B
0000B1 _H	ICR01	Interrupt control register 01			00000111 _B
0000B2 _H	ICR02	Interrupt control register 02			00000111 _B
0000B3 _H	ICR03	Interrupt control register 03			00000111 _B
0000B4 _H	ICR04	Interrupt control register 04			00000111 _B
0000B5 _H	ICR05	Interrupt control register 05			00000111 _B
0000B6 _H	ICR06	Interrupt control register 06			00000111 _B
0000B7 _H	ICR07	Interrupt control register 07			00000111 _B
0000B8 _H	ICR08	Interrupt control register 08			00000111 _B
0000B9 _H	ICR09	Interrupt control register 09			00000111 _B
0000BA _H	ICR10	Interrupt control register 10			00000111 _B
0000BB _H	ICR11	Interrupt control register 11			00000111 _B
0000BC _H	ICR12	Interrupt control register 12			00000111 _B
0000BD _H	ICR13	Interrupt control register 13			00000111 _B
0000BE _H	ICR14	Interrupt control register 14			00000111 _B
0000BF _H	ICR15	Interrupt control register 15			00000111 _B
0000C0 _H to 0000FF _H	(Reserved area) *				
001FF0 _H	PADR0	Detection address setting register 0 (low-order)	R/W	Address matching detection function	XXXXXXXX _B
001FF1 _H		Detection address setting register 0 (middle-order)			XXXXXXXX _B
001FF2 _H		Detection address setting register 0 (high-order)			XXXXXXXX _B
001FF3 _H	PADR1	Detection address setting register 1 (low-order)	R/W		XXXXXXXX _B
001FF4 _H		Detection address setting register 1 (middle-order)			XXXXXXXX _B
001FF5 _H		Detection address setting register 1 (high-order)			XXXXXXXX _B
003900 _H	TMR0/ TMRLR0	16-bit timer register 0/16-bit reload register	R,W	16-bit reload timer 0	XXXXXXXX _B
003901 _H					XXXXXXXX _B
003902 _H	TMR1/ TMRLR1	16-bit timer register 1/16-bit reload register	R,W	16-bit reload timer 1	XXXXXXXX _B
003903 _H					XXXXXXXX _B
003904 _H to 00390F _H	(Reserved area) *				

Address	Register Abbreviation	Register	Read/ Write	Resource	Initial Value
003C38 _H , 003C39 _H	DLCR4	DLC register 4	R/W	CAN controller	XXXXXXXX _B , XXXXXXXX _B
003C3A _H , 003C3B _H	DLCR5	DLC register 5	R/W		XXXXXXXX _B , XXXXXXXX _B
003C3C _H , 003C3D _H	DLCR6	DLC register 6	R/W		XXXXXXXX _B , XXXXXXXX _B
003C3E _H , 003C3F _H	DLCR7	DLC register 7	R/W		XXXXXXXX _B , XXXXXXXX _B
003C40 _H to 003C47 _H	DTR0	Data register 0	R/W		XXXXXXXX _B to XXXXXXXX _B
003C48 _H to 003C4F _H	DTR1	Data register 1	R/W		XXXXXXXX _B to XXXXXXXX _B
003C50 _H to 003C57 _H	DTR2	Data register 2	R/W		XXXXXXXX _B to XXXXXXXX _B
003C58 _H to 003C5F _H	DTR3	Data register 3	R/W		XXXXXXXX _B to XXXXXXXX _B
003C60 _H to 003C67 _H	DTR4	Data register 4	R/W		XXXXXXXX _B to XXXXXXXX _B
003C68 _H to 003C6F _H	DTR5	Data register 5	R/W		XXXXXXXX _B to XXXXXXXX _B
003C70 _H to 003C77 _H	DTR6	Data register 6	R/W		XXXXXXXX _B to XXXXXXXX _B
003C78 _H to 003C7F _H	DTR7	Data register 7	R/W		XXXXXXXX _B to XXXXXXXX _B
003C80 _H to 003CFF _H	(Reserved area) *				
003D00 _H , 003D01 _H	CSR	Control status register	R/W, R	CAN controller	0XXXX001 _B , 00XXX000 _B
003D02 _H	LEIR	Last event display register	R/W		000XX000 _B
003D03 _H	(Reserved area) *				
003D04 _H , 003D05 _H	RTEC	Send/receive error counter	R	CAN controller	00000000 _B , 00000000 _B
003D06 _H , 003D07 _H	BTR	Bit timing register	R/W		11111111 _B , X1111111 _B
003D08 _H	IDER	IDE register	R/W		XXXXXXXX _B
003D09 _H	(Reserved area) *				
003D0A _H	TRTRR	Send RTR register	R/W	CAN controller	00000000 _B
003D0B _H	(Reserved area) *				
003D0C _H	RFWTR	Remote frame receive wait register	R/W	CAN controller	XXXXXXXX _B

11. Interrupt Sources, Interrupt Vectors, And Interrupt Control Registers

Interrupt Source	EI ² OS Readiness	Interrupt Vector			Interrupt Control Register		Priority* ³
		Number		Address	ICR	Address	
Reset	×	#08	08 _H	FFFFDC _H	—	—	High ↑
INT 9 instruction	×	#09	09 _H	FFFFD8 _H	—	—	
Exceptional treatment	×	#10	0A _H	FFFFD4 _H	—	—	
CAN controller reception completed (RX)	✓	#11	0B _H	FFFFD0 _H	ICR00	0000B0 _H * ¹	
CAN controller transmission completed (TX) / Node status transition (NS)	✓	#12	0C _H	FFFFCC _H			
Reserved	×	#13	0D _H	FFFFC8 _H	ICR01	0000B1 _H	
Reserved	×	#14	0E _H	FFFFC4 _H			
CAN wakeup	Δ	#15	0F _H	FFFFC0 _H	ICR02	0000B2 _H * ¹	
Time-base timer	×	#16	10 _H	FFFFBC _H			
16-bit reload timer 0	Δ	#17	11 _H	FFFFB8 _H	ICR03	0000B3 _H * ¹	
8/10-bit A/D converter	Δ	#18	12 _H	FFFFB4 _H			
16-bit free-run timer overflow	Δ	#19	13 _H	FFFFB0 _H	ICR04	0000B4 _H * ¹	
Reserved	×	#20	14 _H	FFFFAC _H			
Reserved	×	#21	15 _H	FFFFA8 _H	ICR05	0000B5 _H * ¹	
PPG timer ch0, ch1 underflow	✓	#22	16 _H	FFFFA4 _H			
Input capture 0-input	Δ	#23	17 _H	FFFFA0 _H	ICR06	0000B6 _H * ¹	
External interrupt (INT4/INT5)	Δ	#24	18 _H	FFFF9C _H			
Input capture 1-input	Δ	#25	19 _H	FFFF98 _H	ICR07	0000B7 _H * ²	
PPG timer ch2, ch3 underflow	✓	#26	1A _H	FFFF94 _H			
External interrupt (INT6/INT7)	Δ	#27	1B _H	FFFF90 _H	ICR08	0000B8 _H * ¹	
Watch timer	Δ	#28	1C _H	FFFF8C _H			
Reserved	×	#29	1D _H	FFFF88 _H	ICR09	0000B9 _H * ¹	
Input capture 2-input Input capture 3-input	✓	#30	1E _H	FFFF84 _H			
Reserved	×	#31	1F _H	FFFF80 _H	ICR10	0000BA _H * ¹	
Reserved	×	#32	20 _H	FFFF7C _H			
Reserved	×	#33	21 _H	FFFF78 _H	ICR11	0000BB _H * ¹	
Reserved	×	#34	22 _H	FFFF74 _H			
Reserved	×	#35	23 _H	FFFF70 _H	ICR12	0000BC _H * ¹	
16-bit reload timer 1	○	#36	24 _H	FFFF6C _H			

12.4 16-bit Input/Output Timer

The 16-bit input/output timer is a compound module composed of 16-bit free-run timer, (1 unit) and input capture (2 units, 4 input pins). The timer, using the 16-bit free-run timer as a basis, enables measurement of clock cycle of an input signal and its pulse width.

Configuration of 16-bit Input/Output Timer

The 16-bit input/output timer is composed of the following modules:

- 16-bit free-run timer (1 unit)
- Input capture (2 units, 2 input pins per unit)

Functions of 16-bit Input/Output Timer

Functions of 16-bit Free-run Timer

The 16-bit free-run timer is composed of 16-bit up counter, timer counter control status register, and prescaler. The 16-bit up counter increments in synchronization with dividing ratio of machine clock.

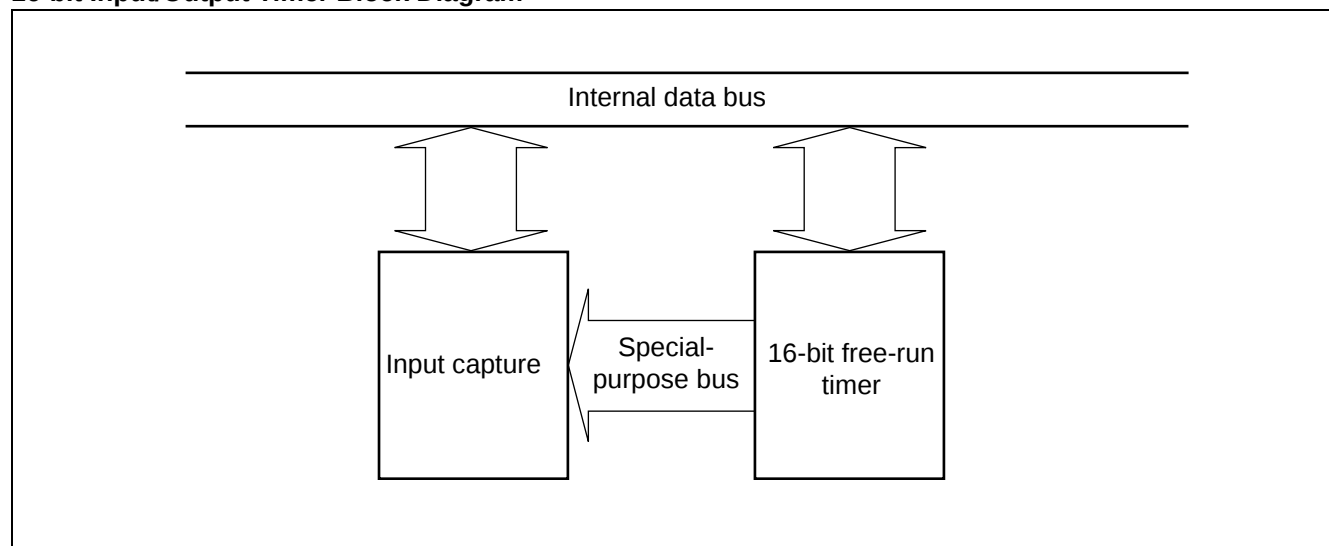
- Count clock is set among four types of machine clock dividing rates.
- Generation of interrupt is allowed by counter value overflow.
- Activation of expanded intelligent I/O service (EI²OS) is allowed by interrupt generation.
- Counter value of 16-bit free-run timer is cleared to "0000_H" by either resetting or software-clearing with timer count clear bit (TCCS: CLR).
- Counter value of 16-bit free-run timer is output to input capture, which is available as base time for capture operation.

Functions of Input Capture

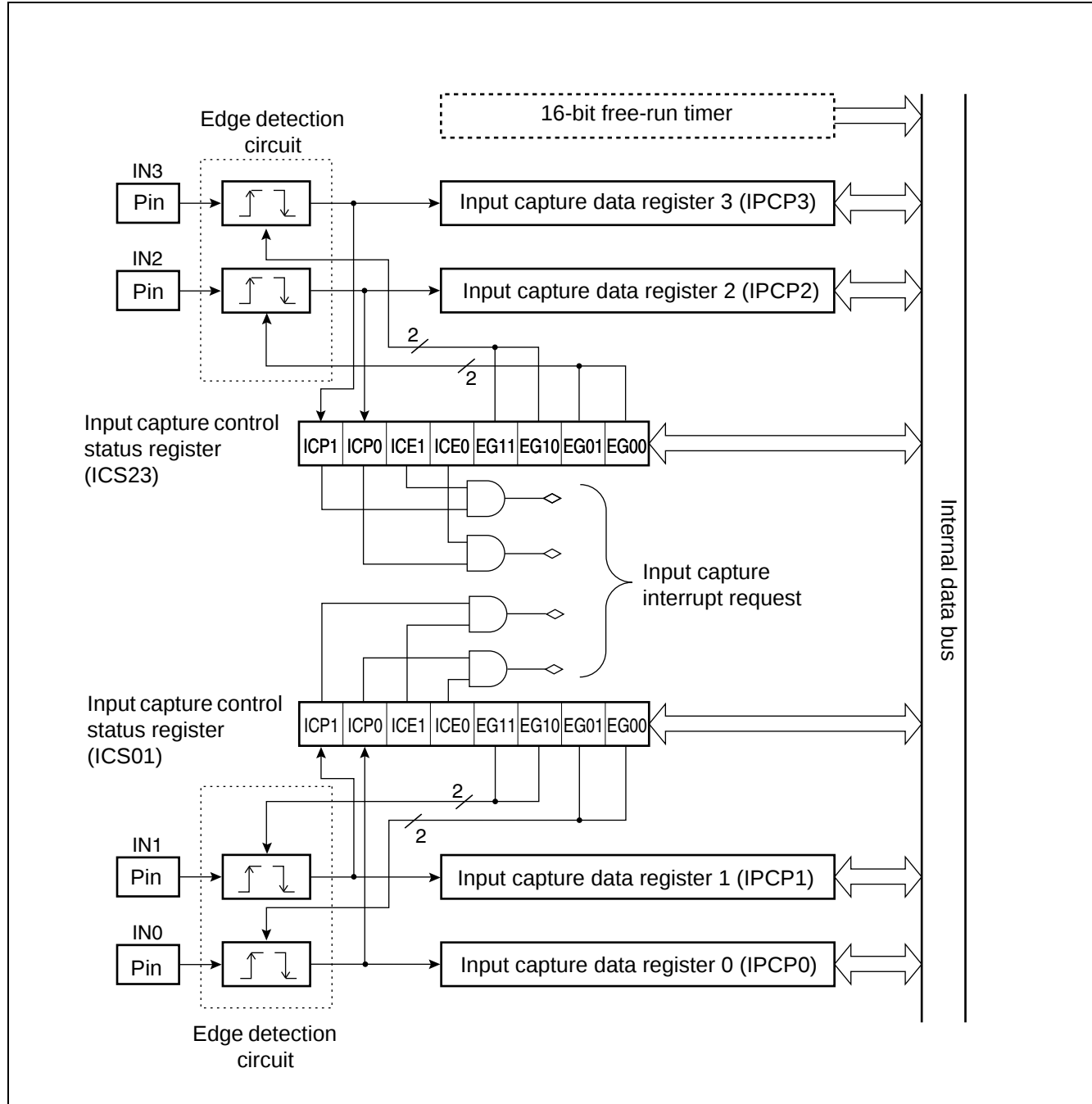
The input capture, upon detecting an edge of a signal input to the input pin from external device, stores a counter value of 16-bit free-run timer at the time of detection into the input capture data register. The function includes the input capture data registers corresponding to four input pins, input capture control status register, and edge detection circuit.

- Rising edge, falling edge, and both edges are selectable for detection.
- Generating interrupt on CPU is allowed by detecting an edge of input signal.
- Expanded intelligent I/O service (EI²OS) is activated by interrupt generation.
- The four input capture input pins and input capture data registers allows monitoring of a maximum of four events.

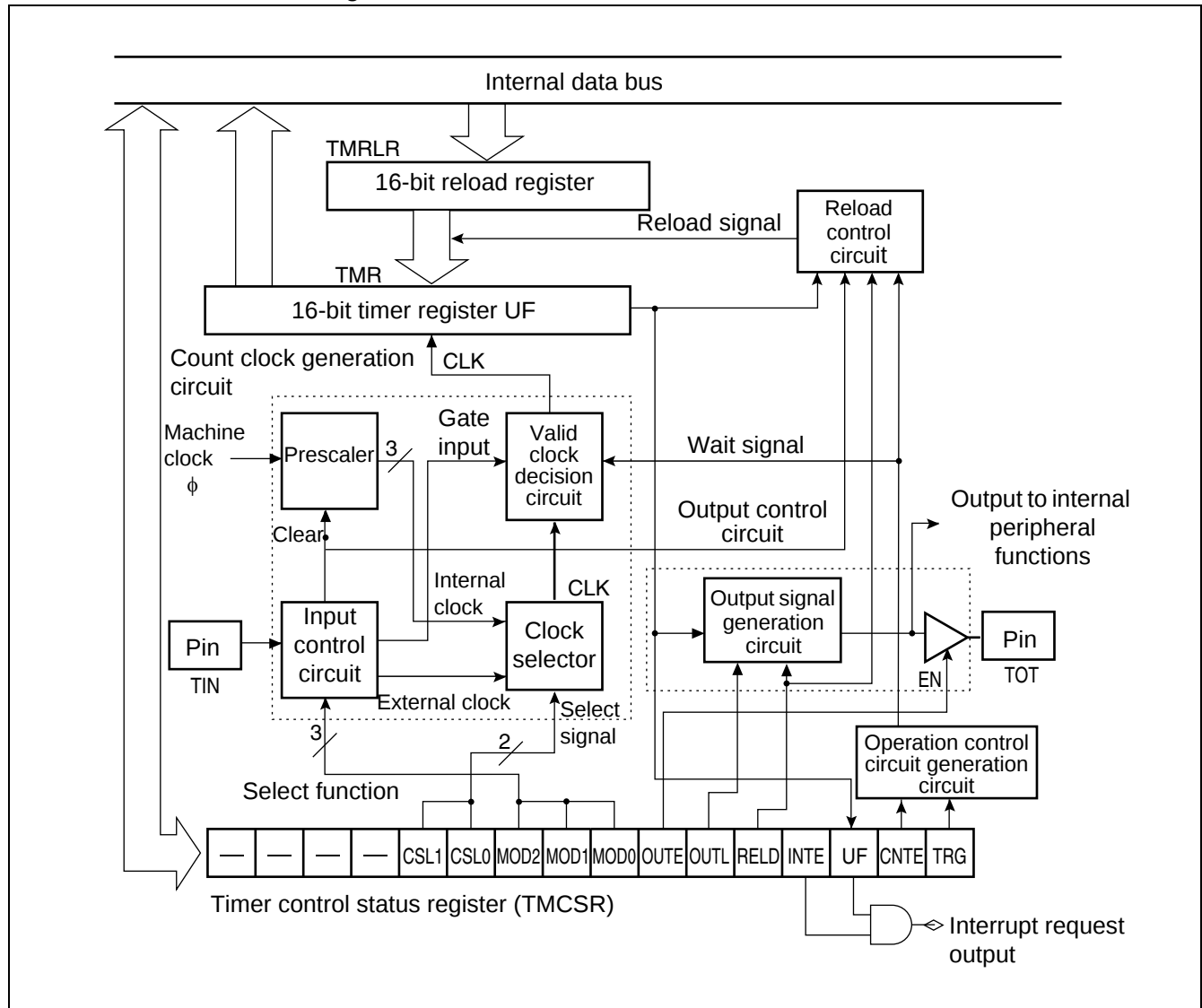
16-bit Input/Output Timer Block Diagram



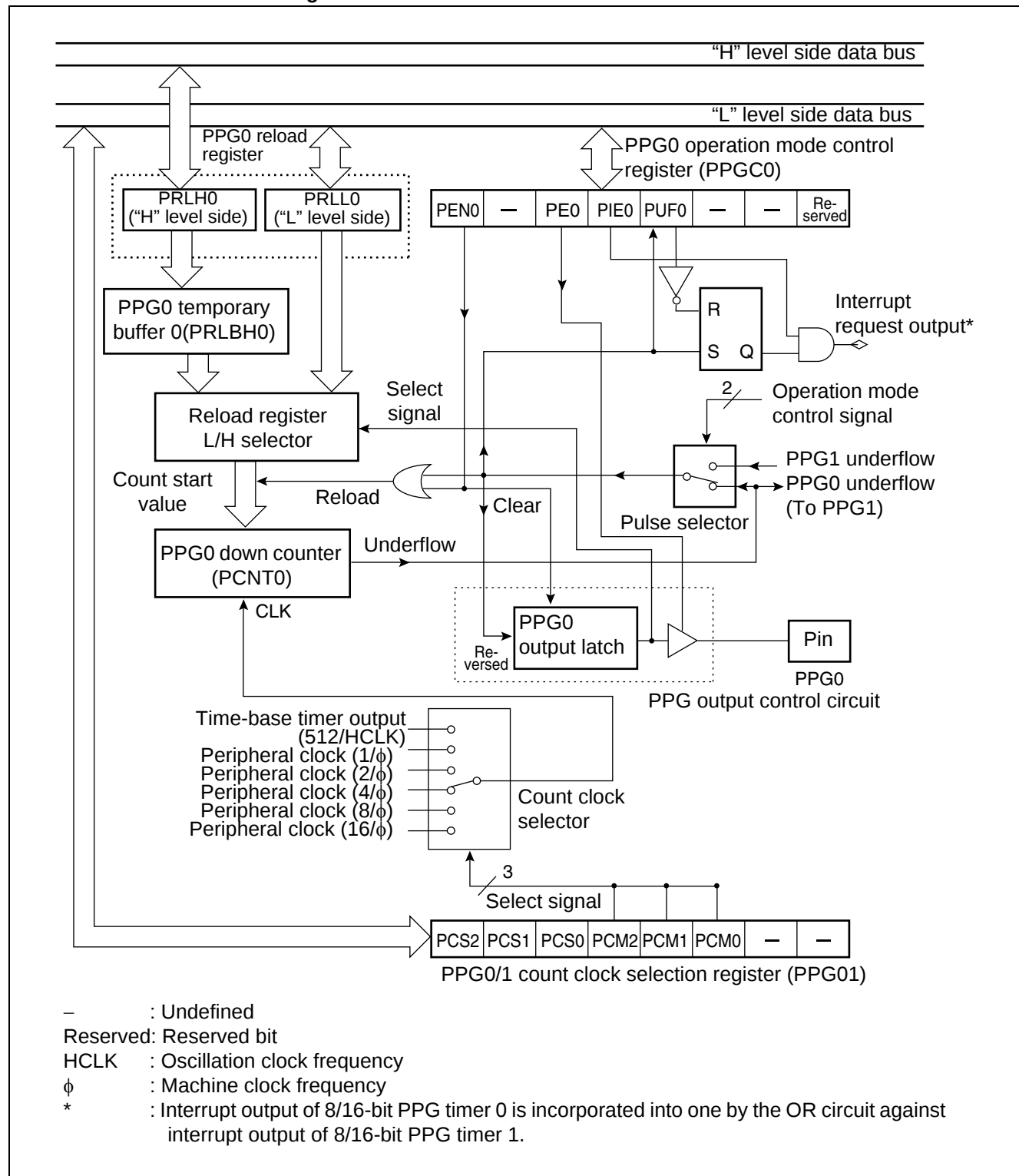
Input Capture Block Diagram



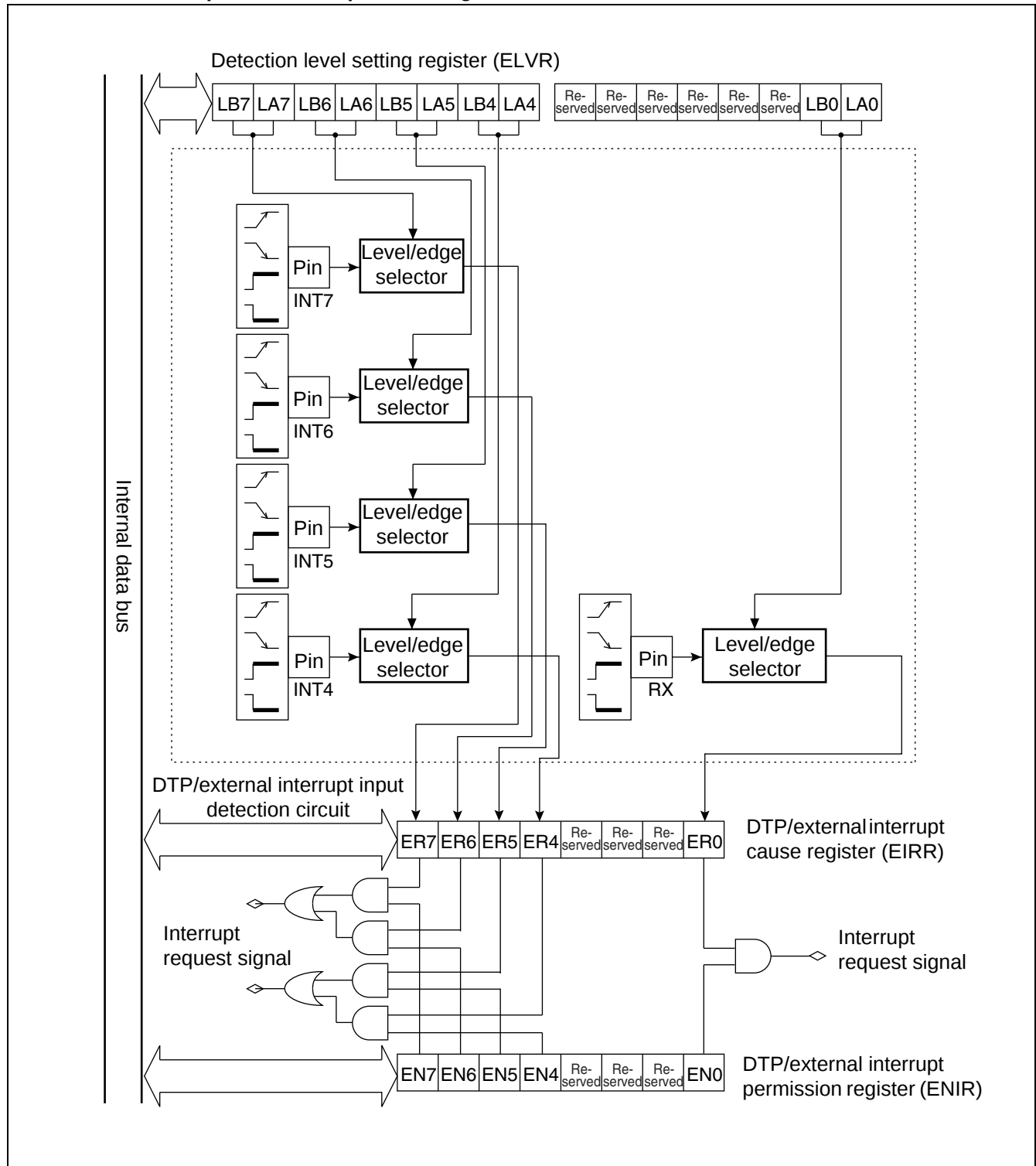
16-bit Reload Timer Block Diagram



8/16-bit PPG Timer 0 Block Diagram



DTP/External Interrupt/CAN Wakeup Block Diagram



12.12 CAN Controller

The Controller Area Network (CAN) is a serial communication protocol compliant with CANVer2.0A and Ver2.0B. The protocol allows data transmission and reception in both standard frame format and expanded frame format.

Features of CAN Controller

- CAN controller format is compliant with CANVer2.0A and Ver2.0B.
- The protocol allows data transmission and reception in standard frame format and expanded frame format.
- Automatic transmission of data frame by remote frame reception is allowed.
- Baud rate ranges from 10 kbps to 1 Mbps (with 16-MHz machine clock).

Table 12-5. Data Transmission Baud Rate

Machine Clock	Baud Rate (Max)
16 MHz	1 Mbps
12 MHz	1 Mbps
8 MHz	1 Mbps
4 MHz	500 kbps
2 MHz	250 kbps

- Provided with 8 transmission/reception message buffers.
- Transmission/reception is allowed at ID 11 bit in standard format, and at ID 29 bit in expanded frame format.
- Specifying 0 byte to 8 bytes is allowed in message data.
- Multi-level message buffer configuration is allowed.
- CAN controller has two built-in acceptance masks. Mask settings are independently allowed for the two acceptance masks on reception IDs.
- The two acceptance masks allow reception in standard frame format and expanded frame format.
- For types of masking, all-bit comparison, all-bit masking, and partial masking with acceptance mask register 0/1, are specifiable.

13.4.4 UART Timing

($V_{CC} = 4.5\text{ V to }5.5\text{ V}$, $V_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$)

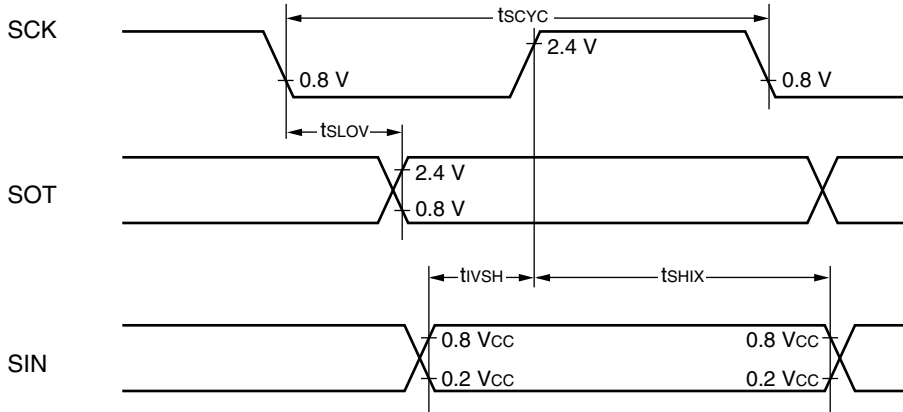
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK1	Internal shift clock mode output pin is: CL = 80 pF+1TTL.	$4\ t_{CP}^*$	–	ns	
SCK ↓ → SOT delay time	t_{SLOV}	SCK1, SOT1		–80	+80	ns	
Valid SIN → SCK ↑	t_{IVSH}	SCK1, SIN1		100	–	ns	
SCK ↑ → valid SIN hold time	t_{SHIX}	SCK1, SIN1		60	–	ns	
Serial clock “H” pulse width	t_{SHSL}	SCK1	External shift clock mode output pin is: CL = 80 pF+1TTL.	$2\ t_{CP}^*$	–	ns	
Serial clock “L” pulse width	t_{SLSH}	SCK1		$2\ t_{CP}^*$	–	ns	
SCK ↓ → SOT delay time	t_{SLOV}	SCK1, SOT1		–	150	ns	
Valid SIN → SCK ↑	t_{IVSH}	SCK1, SIN1		60	–	ns	
SCK ↑ → valid SIN hold time	t_{SHIX}	SCK1, SIN1		60	–	ns	

*: Refer to Clock Timing ratings for t_{CP} (internal operation clock cycle time).

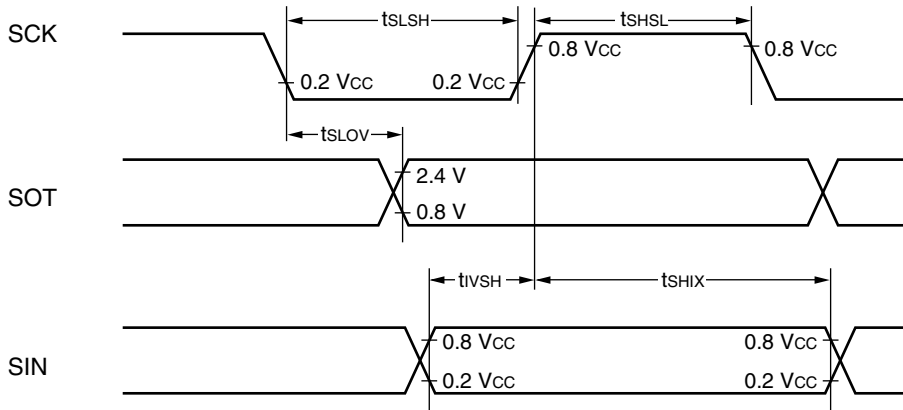
Notes:

- AC Characteristics in CLK synchronous mode.
- C_L is a load capacitance value on pins for testing.

• Internal shift clock mode



• External shift clock mode



13.4.5 Timer Input Timing

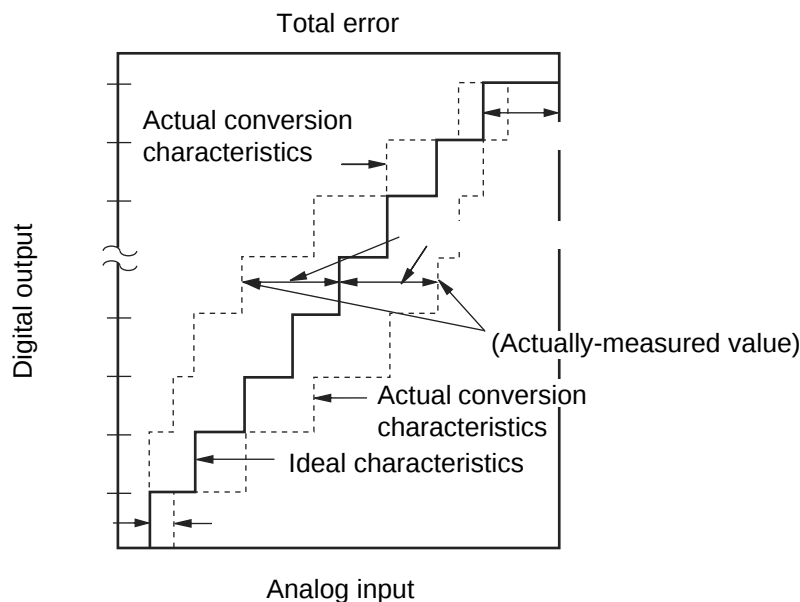
($V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$, $V_{SS} = 0.0 \text{ V}$, $T_A = -40 \text{ }^{\circ}\text{C to } +105 \text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH}	TIN0, TIN1	—	$4 t_{CP}^*$	—	ns	
	t_{TIWL}	IN0 to IN3					

*: Refer to Clock Timing ratings for t_{CP} (internal operation clock cycle time).

13.6 Definition of A/D Converter Terms

Resolution:	Analog variation that is recognized by an A/D converter.
Linear error:	Deviation between a line across zero-transition line ("00 0000 00 0 0" ↔ "00 0000 0001") and full-scale transition line ("11 1111 11 1 0" ↔ "11 1111 1111") and actual conversion characteristics.
Differential linear error:	Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.
Total error:	Difference between an actual value and an ideal value. A total error includes zero transition error, full-scale transition error, and linear error.



$$\text{Total error of digital output "N"} = \frac{V_{NT} - \{1 \text{ LSB} \times (N - 1) + 0.5 \text{ LSB}\}}{1 \text{ LSB}} \quad [\text{LSB}]$$

$$1 \text{ LSB} = (\text{Ideal value}) \frac{AVR - AV_{SS}}{1024} \quad [\text{V}]$$

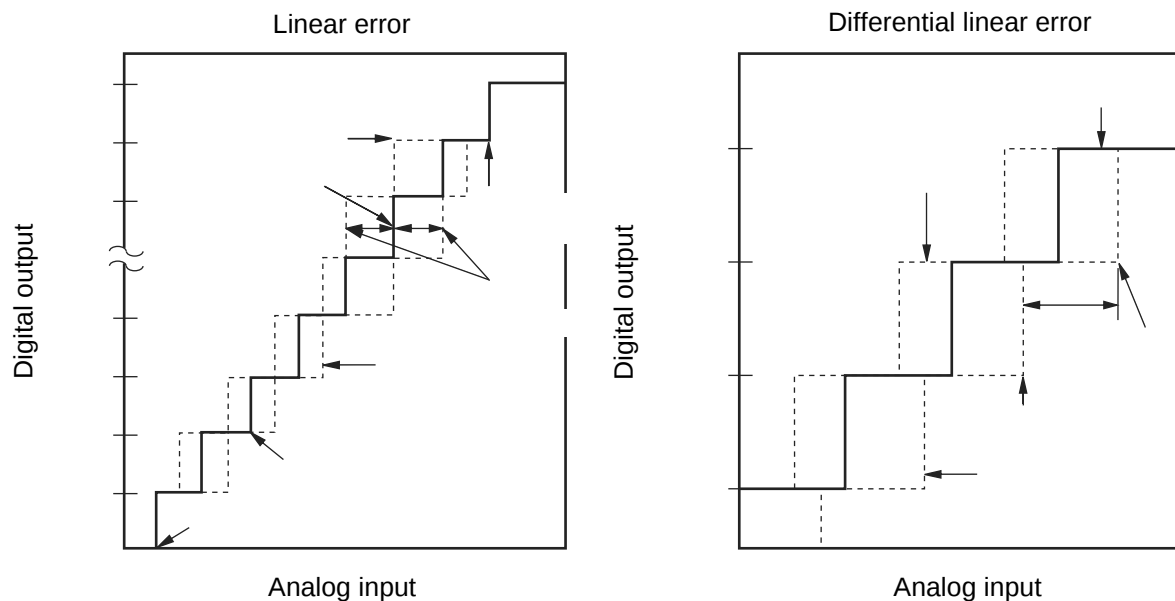
$$V_{OT} (\text{Ideal value}) = AV_{SS} + 0.5 \text{ LSB} \quad [\text{V}]$$

$$V_{FST} (\text{Ideal value}) = AVR - 1.5 \text{ LSB} \quad [\text{V}]$$

V_{NT} : A voltage at which digital output transits from $(N-1)_H$ to N_H .

(Continued)

(Continued)



$$\text{Linear error of digital output } N = \frac{V_{NT} - \{1 \text{ LSB} \times (N - 1) + V_{OT}\}}{1 \text{ LSB}} [\text{LSB}]$$

$$\text{Differential linear error of digital output } N = \frac{V_{(N+1)T} - V_{NT}}{1 \text{ LSB}} - 1 \text{ LSB} [\text{LSB}]$$

$$1 \text{ LSB} = \frac{V_{FST} - V_{OT}}{1022} [\text{V}]$$

V_{OT} : Voltage at which digital output transits from "000_H" to "001_H."

V_{FST} : Voltage at which digital output transits from "3FE_H" to "3FF_H."

13.7 Notes on A/D Converter Section

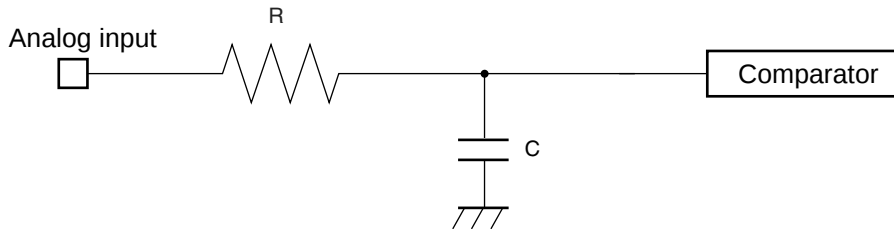
Use the device with external circuits of the following output impedance for analog inputs:

Recommended output impedance of external circuits are: Approx. 3.9 k Ω or lower ($4.5\text{ V} \leq AV_{CC} \leq 5.5\text{ V}$) (sampling period=2.00 μs at 16 MHz machine clock), Approx. 11 k Ω or lower ($4.0\text{ V} \leq AV_{CC} < 4.5\text{ V}$) (sampling period=8.0 μs at 16 MHz machine clock).

If an external capacitor is used, in consideration of the effect by tap capacitance caused by external capacitors and on-chip capacitors, capacitance of the external one is recommended to be several thousand times as high as internal capacitor.

If output impedance of an external circuit is too high, a sampling period for an analog voltage may be insufficient.

• Analog input circuit model



MB90F387/S, MB90387/S

$4.5\text{ V} \leq AV_{CC} \leq 5.5\text{ V}$

$R \cong 2.35\text{ k}\Omega$, $C \cong 36.4\text{ pF}$

$4.0\text{ V} \leq AV_{CC} < 4.5\text{ V}$

$R \cong 16.4\text{ k}\Omega$, $C \cong 36.4\text{ pF}$

Note: Use the values in the figure only as a guideline.

About errors

As [AVR-AVss] become smaller, values of relative errors grow larger.

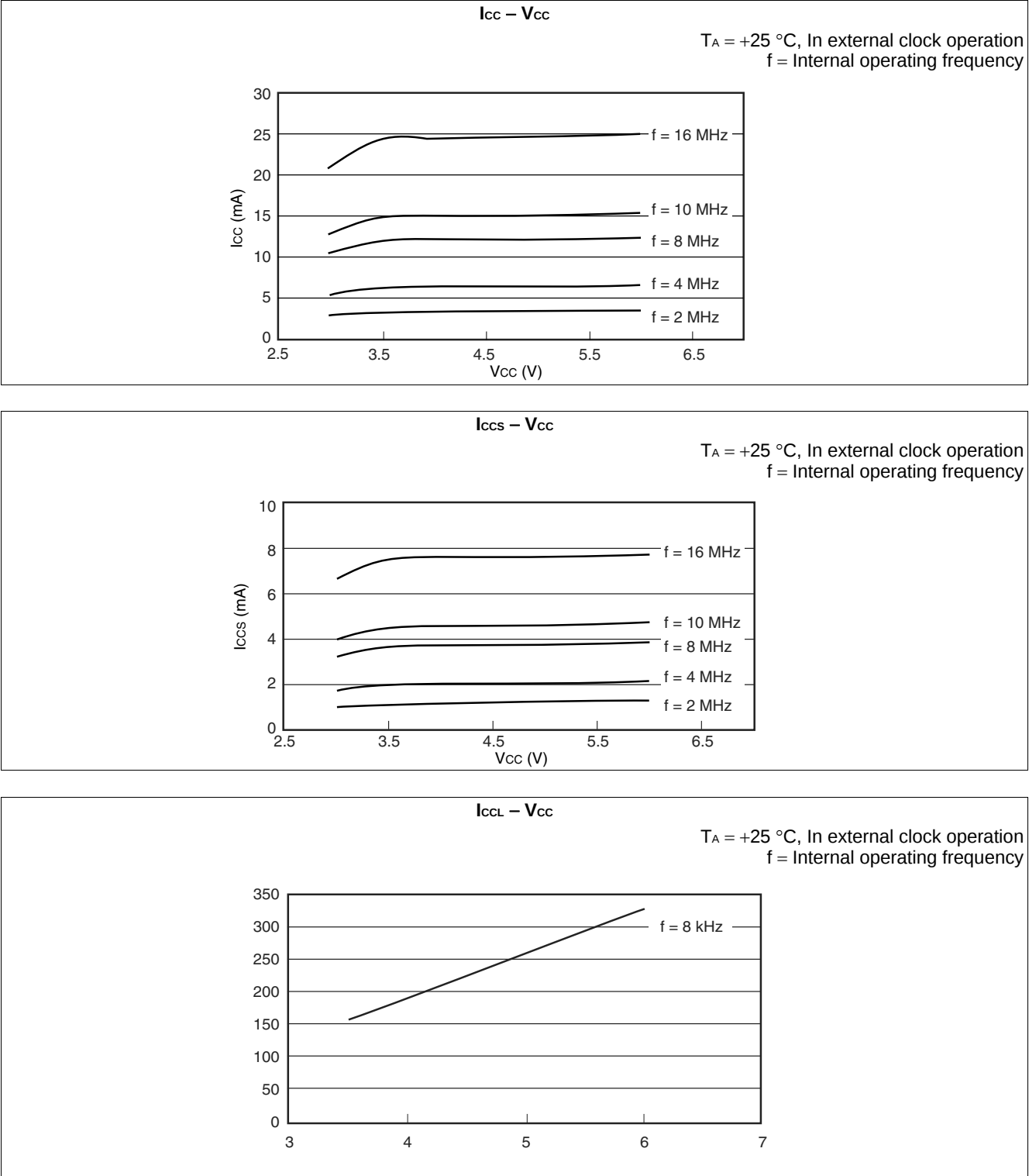
13.8 Flash Memory Program/Erase Characteristics

Parameter	Conditions	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	$T_A = +25\text{ }^\circ\text{C}$ $V_{CC} = 5.0\text{ V}$	—	1	15	s	Excludes 00H programming prior to erasure
Chip erase time		—	4	—	s	Excludes 00H programming prior to erasure
Word (16-bit width) programming time		—	16	3,600	μs	Except for the over head time of the system
Program/Erase cycle	—	10,000	—	—	cycle	
Flash Data Retention Time	Average $T_A = +85\text{ }^\circ\text{C}$	20	—	—	Year	*

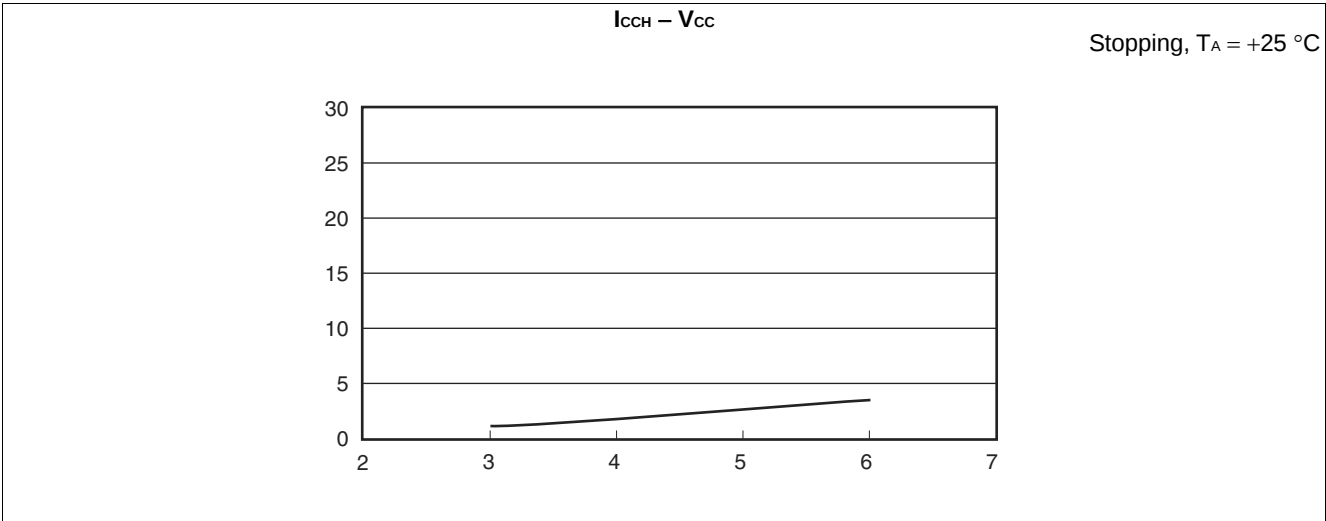
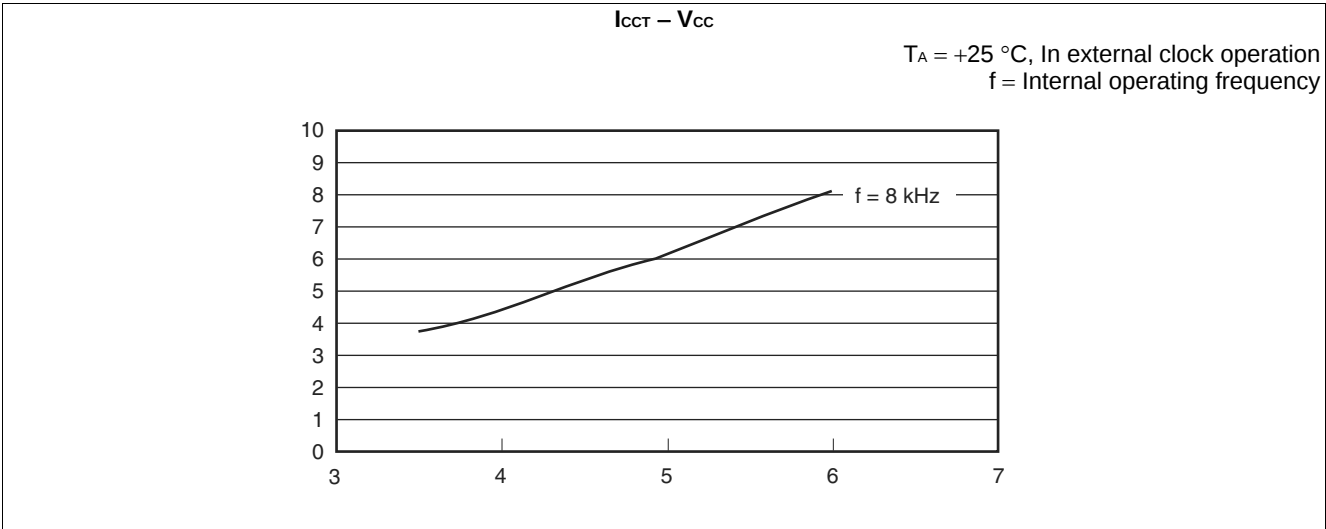
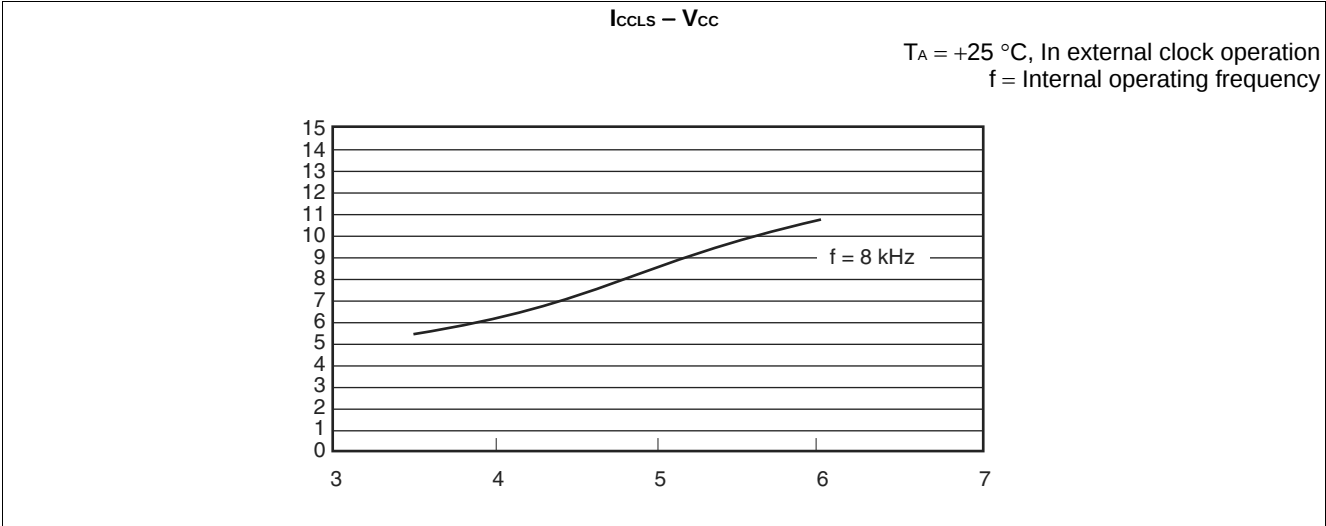
*: This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at +85 $^\circ\text{C}$).

14. Example Characteristics

MB90F387

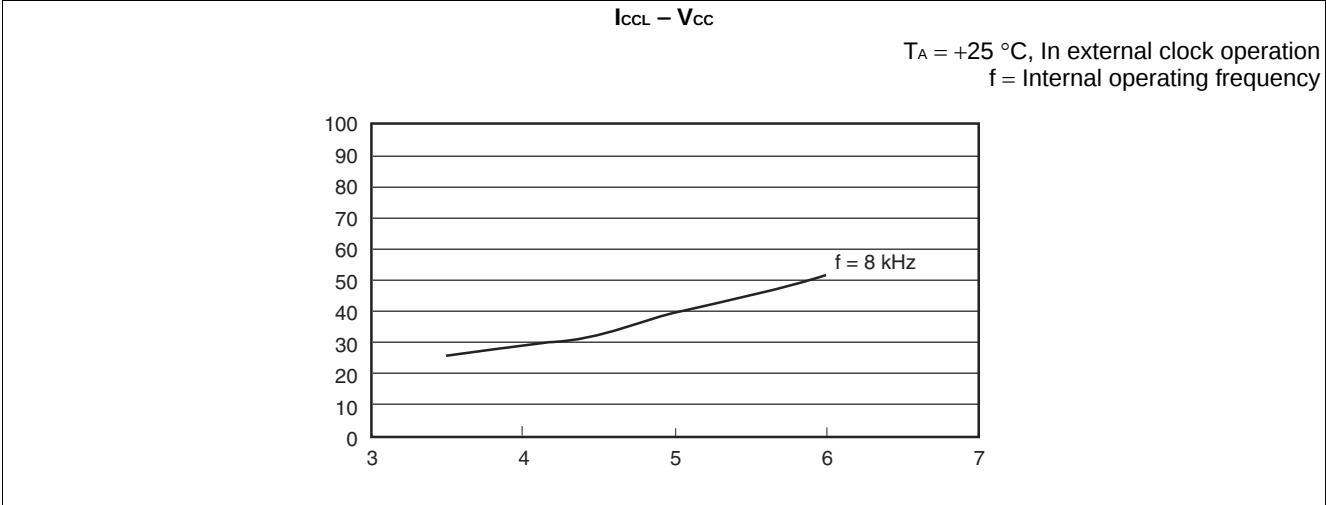
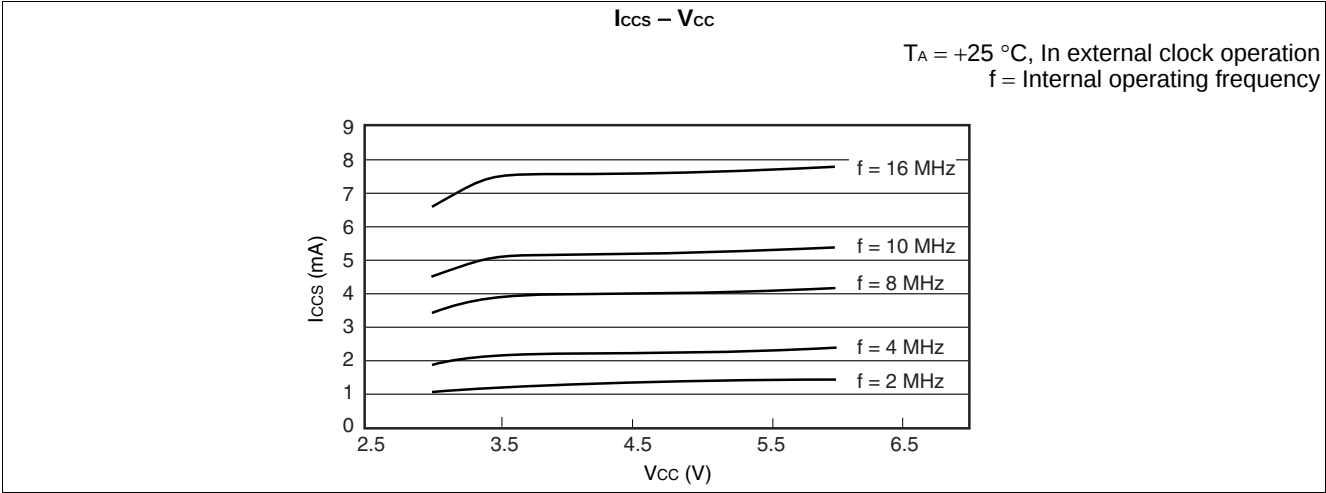
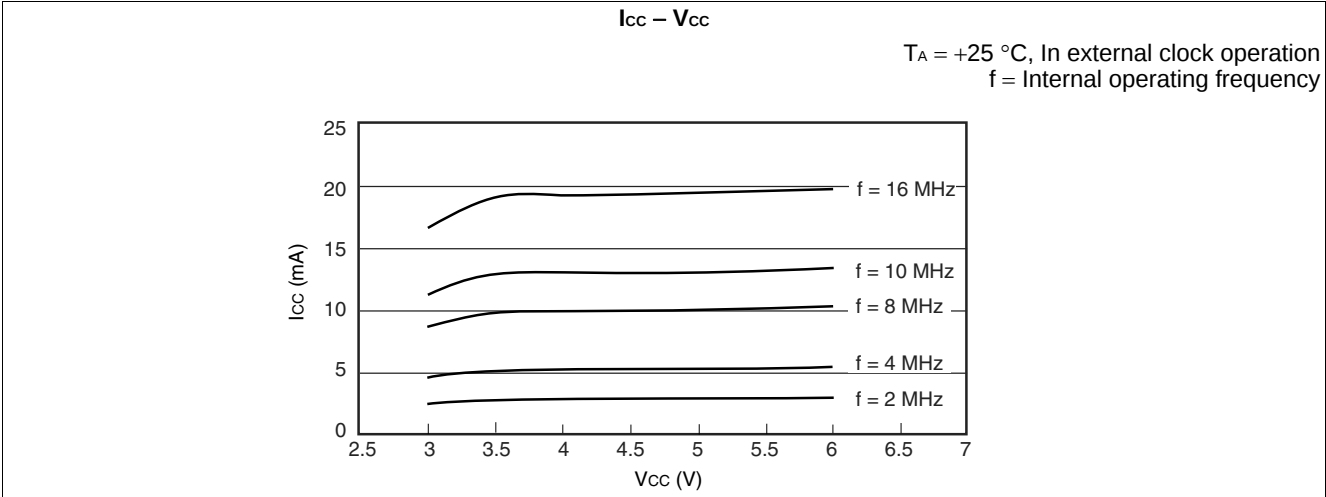


(Continued)



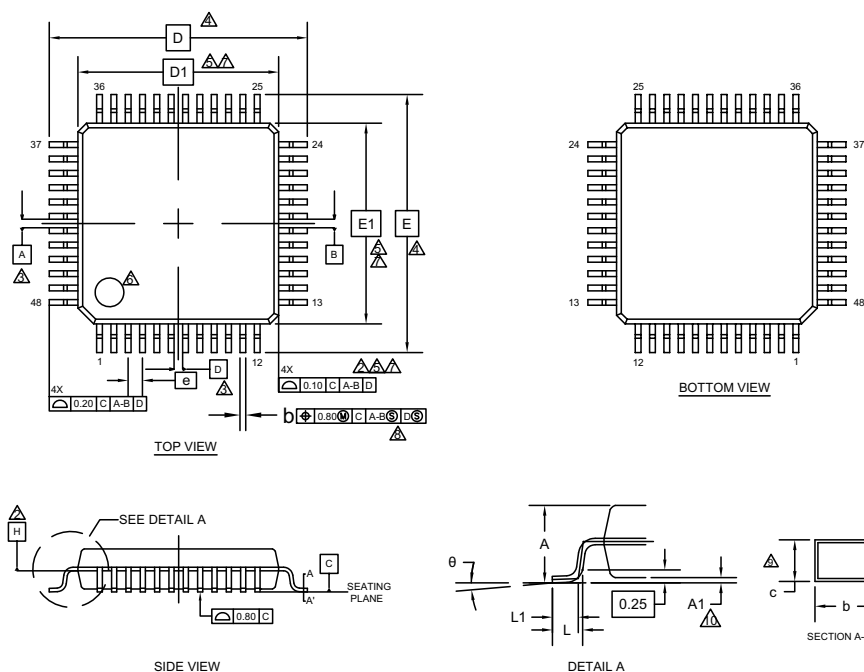
(Continued)

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16. Package Dimension



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.00	—	0.20
b	0.15	—	0.27
c	0.09	—	0.20
D	9.00 BSC		
D1	7.00 BSC		
e	0.50 BSC		
E	9.00 BSC		
E1	7.00 BSC		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
θ	0°	—	8°

NOTES

- ALL DIMENSIONS ARE IN MILLIMETERS.
- DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
- DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
- TO BE DETERMINED AT SEATING PLANE C.
- DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
- DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
- REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS, DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
- DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBER PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
- THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
- A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-13731 **

PACKAGE OUTLINE, 48 LEAD LQFP
7.0X7.0X1.7 MM LQA048 REV**