Infineon Technologies - MB90387SPMT-G-383SN-YE1 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

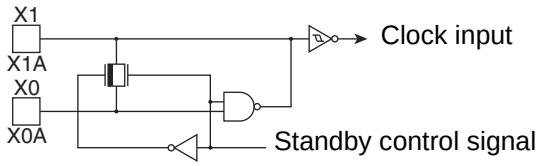
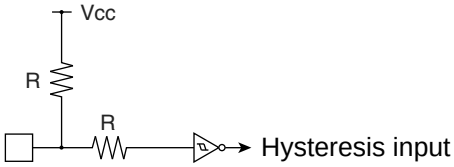
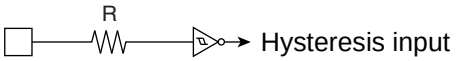
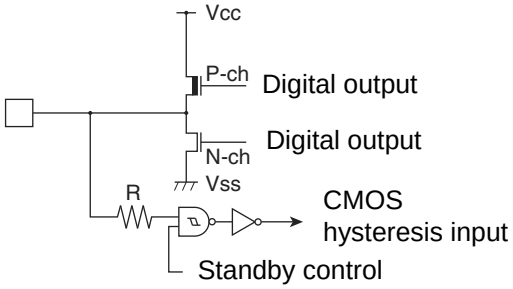
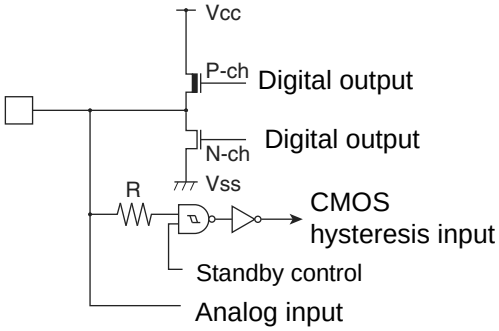
Details	
Product Status	Obsolete
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, SCI, UART/USART
Peripherals	POR, WDT
Number of I/O	36
Program Memory Size	64KB (64K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90387spmt-g-383sn-ye1

Contents

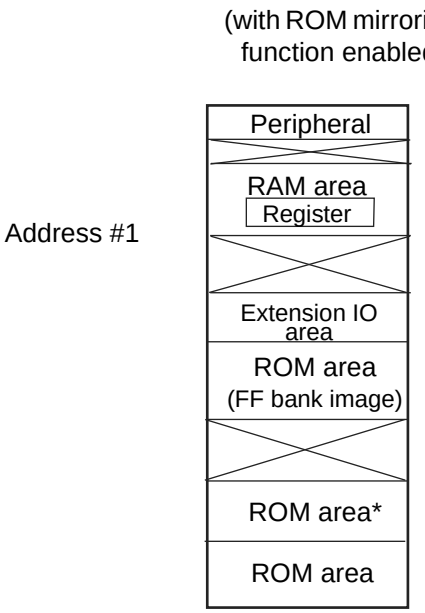
1. Product Lineup

Parameter \ Part Number		MB90F387 MB90F387S	MB90387 MB90387S	MB90V495G
Classification		Flash ROM	Mask ROM	Evaluation product
ROM capacity		64 Kbytes		–
RAM capacity		2 Kbytes		6 Kbytes
Process		CMOS		
Package		LQFP-48 (pin pitch 0.50 mm)		PGA-256
Operating power supply voltage		3.5 V to 5.5 V		4.5 V to 5.5 V
Special power supply for emulator*1		–		None
CPU functions		Number of basic instructions : 351 instructions Instruction bit length : 8 bits and 16 bits Instruction length : 1 byte to 7 bytes Data bit length : 1 bit, 8 bits, 16 bits		
		Minimum instruction execution time: 62.5 ns (at 16 MHz machine clock)		
		Interrupt processing time: 1.5 μs at minimum (at 16 MHz machine clock)		
Low power consumption (standby) mode		Sleep mode / Watch mode / Time-base timer mode / Stop mode / CPU intermittent		
I/O port		General-purpose input/output ports (CMOS output): 34 ports (36 ports*2) including 4 high-current output ports (P14 to P17)		
Time-base timer		18-bit free-run counter Interrupt cycle: 1.024 ms, 4.096 ms, 16.834 ms, 131.072 ms (with oscillation clock frequency at 4 MHz)		
Watchdog timer		Reset generation cycle: 3.58 ms, 14.33 ms, 57.23 ms, 458.75 ms (with oscillation clock frequency at 4 MHz)		
16-bit input/ output timer	16-bit free-run timer	Number of channels: 1 Interrupt upon occurrence of overflow		
	Input capture	Number of channels: 4 Retaining free-run timer value set by pin input (rising edge, falling edge, and both edges)		
16-bit reload timer		Number of channels: 2 16-bit reload timer operation Count clock cycle: 0.25 μs, 0.5 μs, 2.0 μs (at 16-MHz machine clock frequency) External event count is allowed.		
Watch timer		15-bit free-run counter Interrupt cycle: 31.25 ms, 62.5 ms, 12 ms, 250 ms, 500 ms, 1.0 s, 2.0 s (with 8.192 kHz sub clock)		
8/16-bit PPG timer		Number of channels: 2 (four 8-bit channels are available also.) PPG operation is allowed with four 8-bit channels or two 16-bit channels. Outputting pulse wave of arbitrary cycle or arbitrary duty is allowed. Count clock: 62.5 ns to 1 μs (with 16 MHz machine clock)		
Delay interrupt generator module		Interrupt generator module for task switching. Used for realtime OS.		
DTP/External interrupt		Number of inputs: 4 Activated by rising edge, falling edge, “H” level or “L” level input. External interrupt or expanded intelligent I/O service (EI^{2}OS) is available.		

6. I/O Circuit Type

Type	Circuit	Remarks
A		■ High-rate oscillation feedback resistor, approx.1 MΩ ■ Low-rate oscillation feedback resistor, approx.10 MΩ
B		■ Hysteresis input with pull-up resistor. ■ Pull-up resistor, approx.50 kΩ
C		■ Hysteresis input
D		■ CMOS hysteresis input ■ CMOS level output ■ Standby control provided
E		■ CMOS hysteresis input ■ CMOS level output ■ Shared for analog input pin ■ Standby control provided

9.2 Memory Map



Model	Address #1
	001900_H
	000900_H
	000900_H

: Internal access memory

: Access disallowed

*: On MB90387/S or MB90F387/S, to read "$FE0000_H$" to "$FEFFFF_H$" is to read out "$FF0000_H$" to "$FFFFFF_H$".

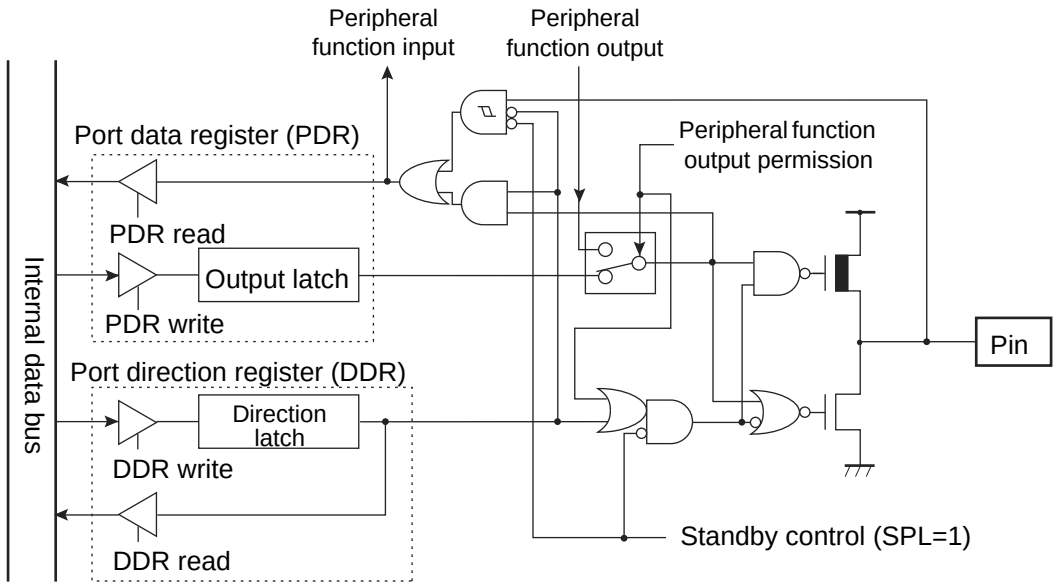
Note: When internal ROM is operating, F²MC-16LX allows viewing ROM data image on FF bank at upper-level of 00 bank. This function is called "mirroring ROM," which allows effective use of C compiler small model.
F²MC-16LX assigns the same low order 16-bit address to FF bank and 00 bank, which allows referencing table in ROM without specifying "far" using pointer.
For example, when accessing to "$00C000_H$", ROM data at "$FFC000_H$" is accessed actually. However, because ROM area of FF bank exceeds 48 Kbytes, viewing all areas is not possible on 00 bank image. Because ROM data of "$FF4000_H$" to "$FFFFFF_H$" is viewed on "004000_H" to "$00FFFF_H$" image, store a ROM data table in area "$FF4000_H$" to "$FFFFFF_H$."

10. I/O Map

Address	Register Abbreviation	Register	Read/ Write	Resource	Initial Value
000000H	(Reserved area) *				
000001H	PDR1	Port 1 data register	R/W	Port 1	XXXXXXXXB
000002H	PDR2	Port 2 data register	R/W	Port 2	XXXXXXXXB
000003H	PDR3	Port 3 data register	R/W	Port 3	XXXXXXXXB
000004H	PDR4	Port 4 data register	R/W	Port 4	XXXXXXXXB
000005H	PDR5	Port 5 data register	R/W	Port 5	XXXXXXXXB
000006H to 000010H	(Reserved area) *				
000011H	DDR1	Port 1 direction data register	R/W	Port 1	00000000B
000012H	DDR2	Port 2 direction data register	R/W	Port 2	00000000B
000013H	DDR3	Port 3 direction data register	R/W	Port 3	000X0000B
000014H	DDR4	Port 4 direction data register	R/W	Port 4	XXX00000B
000015H	DDR5	Port 5 direction data register	R/W	Port 5	00000000B
000016H to 00001AH	(Reserved area) *				
00001BH	ADER	Analog input permission register	R/W	8/10-bit A/D converter	11111111B
00001CH to 000025H	(Reserved area) *				
000026H	SMR1	Serial mode register 1	R/W	UART1	00000000B
000027H	SCR1	Serial control register 1	R/W, W		00000100B
000028H	SIDR1/ SODR1	Serial input data register 1/ Serial output data register 1	R, W		XXXXXXXXB
000029H	SSR1	Serial status data register 1	R, R/W		00001000B
00002AH	(Reserved area) *				
00002BH	CDCR1	Communication prescaler control register 1	R/W	UART1	0XXX0000B
00002CH to 00002FH	(Reserved area) *				
000030H	ENIR	DTP/External interrupt permission register	R/W	DTP/External interrupt	00000000B
000031H	EIRR	DTP/External interrupt permission register	R/W		XXXXXXXXB
000032H	ELVR	Detection level setting register	R/W		00000000B
000033H			R/W		00000000B
000034H	ADCS	A/D control status register	R/W	8/10-bit A/D converter	00000000B
000035H			R/W, W		00000000B
000036H	ADCR	A/D data register	W, R		XXXXXXXXB
000037H			R		00101XXXB

Address	Register Abbreviation	Register	Read/ Write	Resource	Initial Value
0000B0H	ICR00	Interrupt control register 00	R/W	Interrupt controller	00000111B
0000B1H	ICR01	Interrupt control register 01			00000111B
0000B2H	ICR02	Interrupt control register 02			00000111B
0000B3H	ICR03	Interrupt control register 03			00000111B
0000B4H	ICR04	Interrupt control register 04			00000111B
0000B5H	ICR05	Interrupt control register 05			00000111B
0000B6H	ICR06	Interrupt control register 06			00000111B
0000B7H	ICR07	Interrupt control register 07			00000111B
0000B8H	ICR08	Interrupt control register 08			00000111B
0000B9H	ICR09	Interrupt control register 09			00000111B
0000BAH	ICR10	Interrupt control register 10			00000111B
0000BBH	ICR11	Interrupt control register 11			00000111B
0000BCH	ICR12	Interrupt control register 12			00000111B
0000BDH	ICR13	Interrupt control register 13			00000111B
0000BEH	ICR14	Interrupt control register 14			00000111B
0000BFH	ICR15	Interrupt control register 15			00000111B
0000C0H to 0000FFH	(Reserved area) *				
001FF0H	PADR0	Detection address setting register 0 (low-order)	R/W	Address matching detection function	XXXXXXXXB
001FF1H		Detection address setting register 0 (middle-order)			XXXXXXXXB
001FF2H		Detection address setting register 0 (high-order)			XXXXXXXXB
001FF3H	PADR1	Detection address setting register 1 (low-order)	R/W		XXXXXXXXB
001FF4H		Detection address setting register 1 (middle-order)			XXXXXXXXB
001FF5H		Detection address setting register 1 (high-order)			XXXXXXXXB
003900H	TMR0/ TMRLR0	16-bit timer register 0/16-bit reload register	R,W	16-bit reload timer 0	XXXXXXXXB
003901H					XXXXXXXXB
003902H	TMR1/ TMRLR1	16-bit timer register 1/16-bit reload register	R,W	16-bit reload timer 1	XXXXXXXXB
003903H					XXXXXXXXB
003904H to 00390FH	(Reserved area) *				

Port 3 Pins Block Diagram (general-purpose input/output port)



Standby control: Control among Stop mode (SPL=1), Time-base timer mode (SPL=1), and watch mode (SPL=1).

Port 3 Registers

■ Port 3 registers include port 3 data register (PDR3) and port 3 direction register (DDR3).

■ The bits configuring the register correspond to port 3 pins on a one-to-one basis.

Relation between Port 3 Registers and Pins

Port Name	Bits of Register and Corresponding Pins								
Port 3	PDR3, DDR3	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	Corresponding pins	P37	P36*	P35*	–	P33	P32	P31	P30

*: P35 and P36 do not exist on MB90387and MB90F387.

12.4 16-bit Input/Output Timer

The 16-bit input/output timer is a compound module composed of 16-bit free-run timer, (1 unit) and input capture (2 units, 4 input pins). The timer, using the 16-bit free-run timer as a basis, enables measurement of clock cycle of an input signal and its pulse width.

Configuration of 16-bit Input/Output Timer

The 16-bit input/output timer is composed of the following modules:

- 16-bit free-run timer (1 unit)
- Input capture (2 units, 2 input pins per unit)

Functions of 16-bit Input/Output Timer

Functions of 16-bit Free-run Timer

The 16-bit free-run timer is composed of 16-bit up counter, timer counter control status register, and prescaler. The 16-bit up counter increments in synchronization with dividing ratio of machine clock.

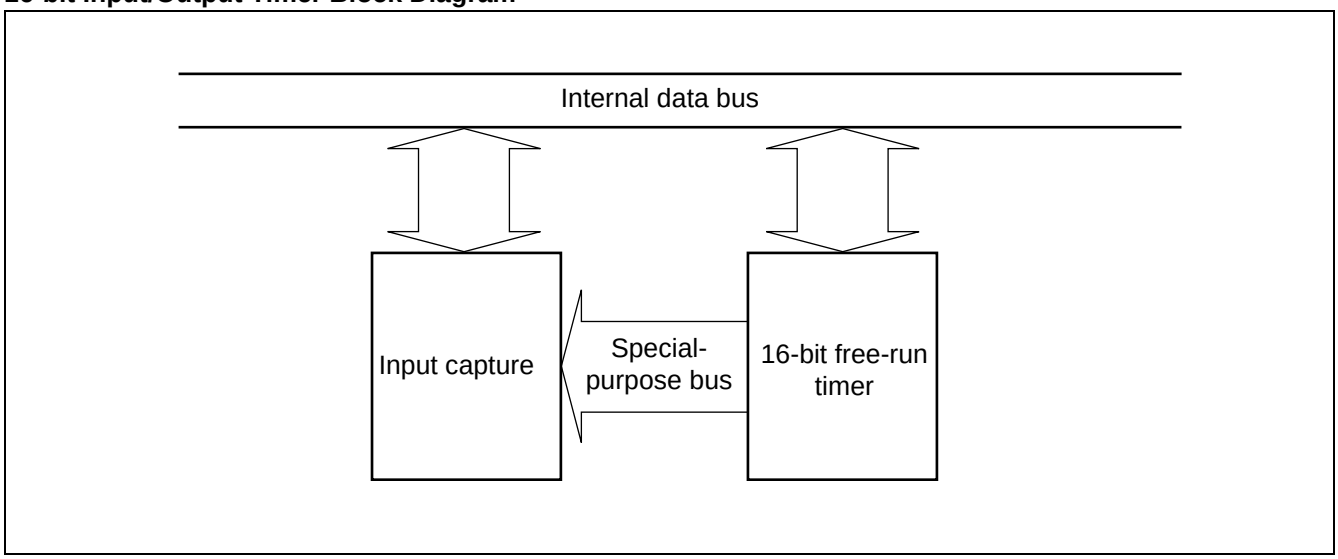
- Count clock is set among four types of machine clock dividing rates.
- Generation of interrupt is allowed by counter value overflow.
- Activation of expanded intelligent I/O service (EI^{2}OS) is allowed by interrupt generation.
- Counter value of 16-bit free-run timer is cleared to "0000$_H$" by either resetting or software-clearing with timer count clear bit (TCCS: CLR).
- Counter value of 16-bit free-run timer is output to input capture, which is available as base time for capture operation.

Functions of Input Capture

The input capture, upon detecting an edge of a signal input to the input pin from external device, stores a counter value of 16-bit free-run timer at the time of detection into the input capture data register. The function includes the input capture data registers corresponding to four input pins, input capture control status register, and edge detection circuit.

- Rising edge, falling edge, and both edges are selectable for detection.
- Generating interrupt on CPU is allowed by detecting an edge of input signal.
- Expanded intelligent I/O service (EI^{2}OS) is activated by interrupt generation.
- The four input capture input pins and input capture data registers allows monitoring of a maximum of four events.

16-bit Input/Output Timer Block Diagram



12.7 8/16-bit PPG Timer Outline

The 8/16-bit PPG timer is a 2-channel reload timer module (PPG0 and PPG1) that allows outputting pulses of arbitrary cycle and duty cycle. Combination of the two channels allows selection among the following operations:

- 8-bit PPG output 2-channel independent operation mode
- 16-bit PPG output operation mode
- 8-bit and 8-bit PPG output operation mode

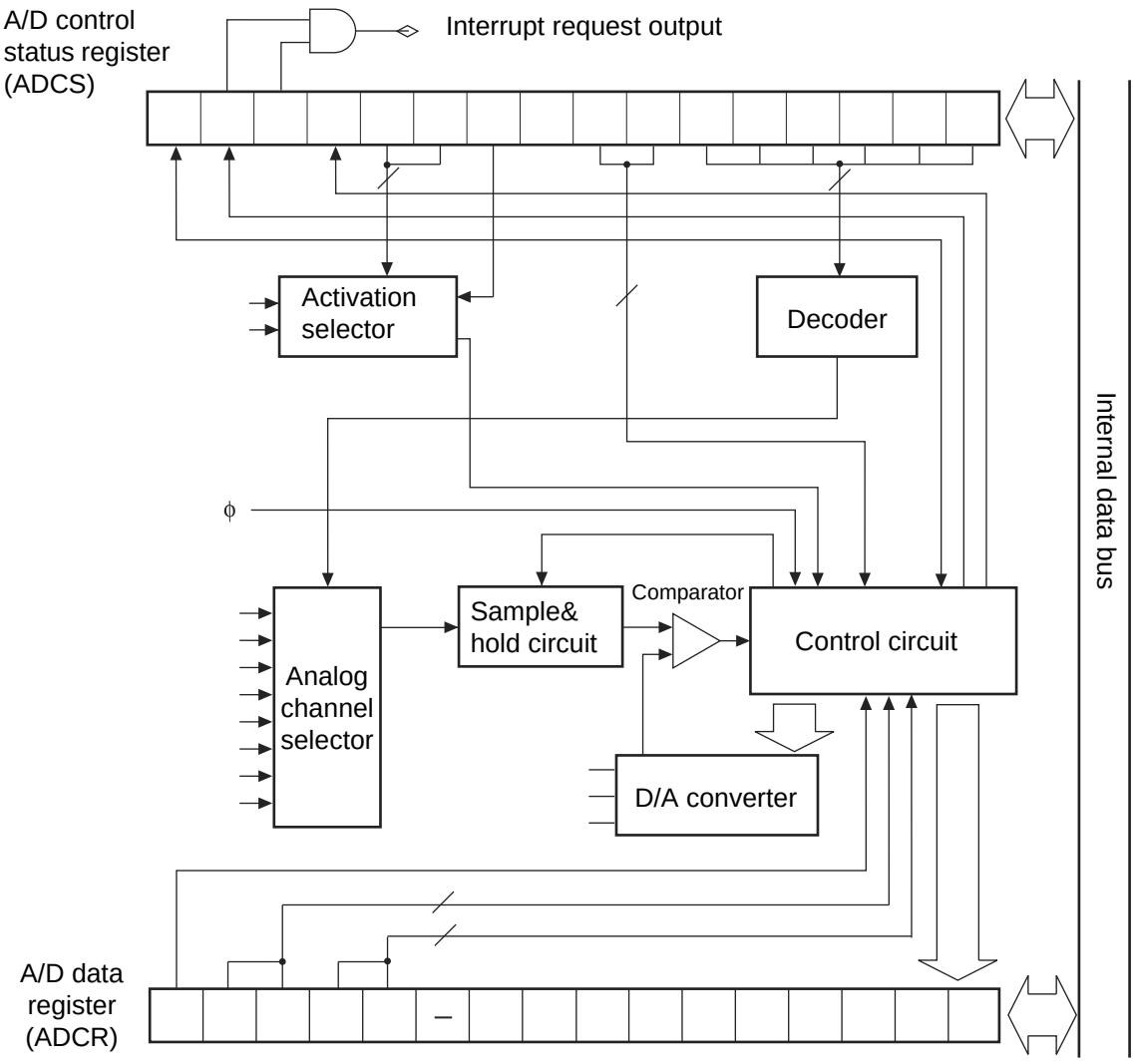
MB90385 series device has two 8/16-bit built-in PPG timers. This section describes functions of PPG0/1. PPG2/3 have the same functions as those of PPG0/1.

Functions of 8/16-bit PPG Timer

The 8/16-bit PPG timer is composed of four 8-bit reload register (PRLH0/PRLL0, PRLH1/PRLL1) and two PPG down counters (PCNT0, PCNT1).

- Widths of “H” and “L” in output pulse are specifiable independently. Cycle and duty factor of output pulse is specifiable arbitrarily.
- Count clock is selectable among 6 internal clocks.
- The timer is usable as an interval timer, by generating interrupt requests for each interval.
- The time is usable as a D/A converter, with an external circuit.

8/10-bit A/D Converter Block Diagram



TO : Internal timer output
– : Not defined
Reserved: Be sure to set to “0”
ϕ : Machine clock

12.11 UART Outline

UART is a general-purpose serial data communication interface for synchronous and asynchronous communication using external devices.

- Provided with bi-directional communication function for both clock-synchronous and clock-asynchronous modes.
- Provided with master/slave communication function (multi-processor mode). (Only master side is available.)
- Interrupt request is generated upon completion of reception, completion of transmission and detection of reception error.
- Ready for expanded intelligent service, EI^{2}OS.

Table 12-3. UART Functions

	Description
Data buffer	Full-duplex double buffer
Transmission mode	Clock synchronous (No start/stop bit, no parity bit) Clock asynchronous (start-stop synchronous)
Baud rate	Built-in special-purpose baud-rate generator. Setting is selectable among 8 values. Input of external values is allowed. Use of clock from external timer (16-bit reload timer 0) is allowed.
Data length	7 bits (only asynchronous normal mode) 8 bits
Signaling system	Non Return to Zero (NRZ) system
Reception error detection	Framing error Overrun error Parity error (not detectable in operation mode 1 (multi-processor mode))
Interrupt request	Receive interrupt (reception completed, reception error detected) Transmission interrupt (transmission completed) Ready for expanded intelligent I/O service (EI^{2}OS) in both transmission and reception
Master/slave communication function (asynchronous, multi-processor mode)	Communication between 1 (master) and n (slaves) are available (usable as master only).

Note: Start/stop bit is not added upon clock-synchronous transmission. Data only is transmitted.

Table 12-4. UART Operation Modes

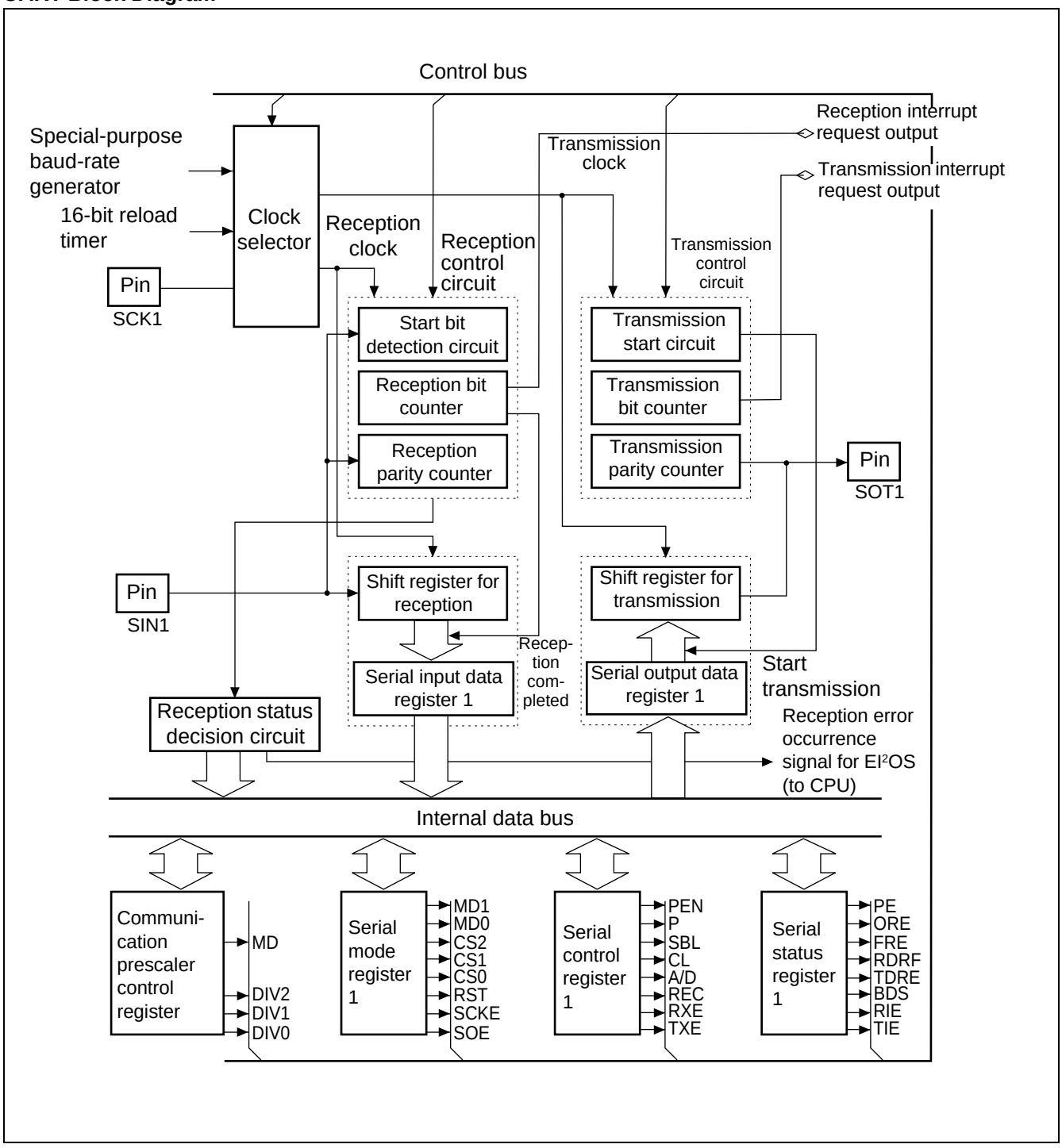
Operation Mode		Data Length		Synchronization	Stop Bit Length
		With Parity	Without Parity		
0	Asynchronous mode (normal mode)	7-bit or 8-bit		Asynchronous	1- bit or 2-bit *2
1	Multi processor mode	8+1*1	–	Asynchronous	
2	Synchronous mode	8	–	Synchronous	No

–: Disallowed

1: “+1” is an address/data selection bit used for communication control (bit 11 of SCR1 register: A/D).

2: Only 1 bit is detected as a stop bit on data reception.

UART Block Diagram



12.12 CAN Controller

The Controller Area Network (CAN) is a serial communication protocol compliant with CANVer2.0A and Ver2.0B. The protocol allows data transmission and reception in both standard frame format and expanded frame format.

Features of CAN Controller

- CAN controller format is compliant with CANVer2.0A and Ver2.0B.
- The protocol allows data transmission and reception in standard frame format and expanded frame format.
- Automatic transmission of data frame by remote frame reception is allowed.
- Baud rate ranges from 10 kbps to 1 Mbps (with 16-MHz machine clock).

Table 12-5. Data Transmission Baud Rate

Machine Clock	Baud Rate (Max)
16 MHz	1 Mbps
12 MHz	1 Mbps
8 MHz	1 Mbps
4 MHz	500 kbps
2 MHz	250 kbps

- Provided with 8 transmission/reception message buffers.
- Transmission/reception is allowed at ID 11 bit in standard format, and at ID 29 bit in expanded frame format.
- Specifying 0 byte to 8 bytes is allowed in message data.
- Multi-level message buffer configuration is allowed.
- CAN controller has two built-in acceptance masks. Mask settings are independently allowed for the two acceptance masks on reception IDs.
- The two acceptance masks allow reception in standard frame format and expanded frame format.
- For types of masking, all-bit comparison, all-bit masking, and partial masking with acceptance mask register 0/1, are specifiable.

Sector Configuration of 512 Kbit Flash Memory

Flash memory	CPU address	Writer address*
SA0 (32 Kbytes)	FF0000H FF7FFFH	70000H 77FFFH
SA1 (8 Kbytes)	FF8000H FF9FFFH	78000H 79FFFH
SA2 (8 Kbytes)	FFA000H FFBFFFH	7A000H 7BFFFH
SA3 (16 Kbytes)	FFC000H FFFFFFH	7C000H 7FFFFH

*: “Writer address” is an address equivalent to CPU address, which is used when data is written on Flash memory, using parallel writer. When writing/deleting data with general-purpose writer, the writer address is used for writing and deleting.

13.4 AC Characteristics

13.4.1 Clock Timing

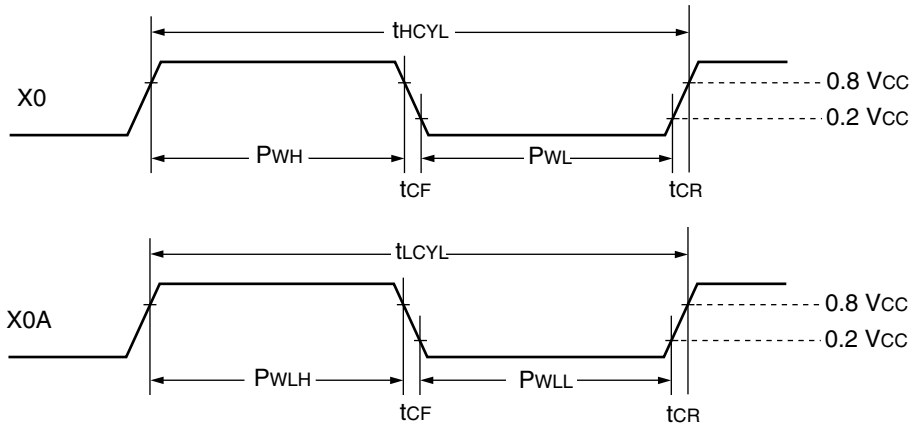
(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_C	X0, X1	3	—	8	MHz	When crystal or ceramic resonator is used*2
			3	—	16	MHz	External clock input*1, *2
			4	—	16	MHz	PLL Multiply by 1 *2
			4	—	8	MHz	PLL Multiply by 2 *2
			4	—	5.33	MHz	PLL Multiply by 3 *2
			4	—	4	MHz	PLL Multiply by 4 *2
	f_{CL}	X0A, X1A	—	32.768	—	kHz	
Clock cycle time	t_{HCYL}	X0, X1	125	—	333	ns	
	t_{LCYL}	X0A, X1A	—	30.5	—	µs	
Input clock pulse width	P_{WH}, P_{WL}	X0	10	—	—	ns	Set duty factor at 30% to 70% as a guideline.
	P_{WLH},P_{WLL}	X0A	—	15.2	—	µs	
Input clock rise time and fall time	t_{CR}, t_{CF}	X0	—	—	5	ns	When external clock is used
Internal operation clock frequency	f_{CP}	—	1.5	—	16	MHz	When main clock is used
	f_{LCP}	—	—	8.192	—	kHz	When sub clock is used
Internal operation clock cycle time	t_{CP}	—	62.5	—	666	ns	When main clock is used
	t_{LCP}	—	—	122.1	—	µs	When sub clock is used

*1: Internal operation clock frequency should not exceed 16 MHz.

*2: When selecting the PLL clock, the range of clock frequency is limited. Use this product within range as mentioned in “Relation among external clock frequency and internal clock frequency”.

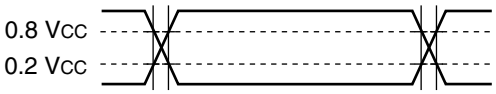
• Clock timing



Rating values of alternating current is defined by the measurement reference voltage values shown below:

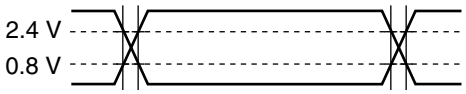
- Input signal waveform

Hysteresis input pin



- Output signal waveform

Output pin



13.4.2 Reset Input Timing

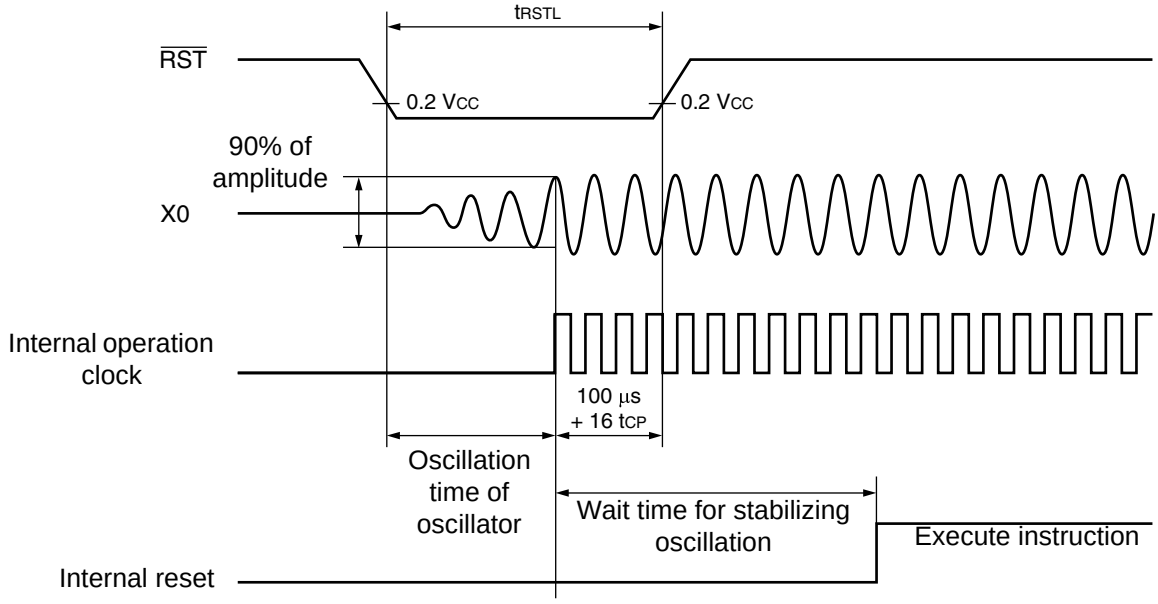
Parameter	Symbol	Pin Name	Value		Unit	Remarks
			Min	Max		
Reset input time	t_{RSTL}	RST	16 t_{CP}*3	–	ns	Normal operation
			Oscillation time of oscillator*1 + 100 μs + 16 t_{CP}*3	–	–	In sub clock*2, sub sleep*2, watch*2 and stop mode
			100	–	μs	In timebase timer

*1: Oscillation time of oscillator is time that the amplitude reached the 90%. In the crystal oscillator, the oscillation time is between several ms to tens of ms. In ceramic oscillator, the oscillation time is between hundreds of μs to several ms. In the external clock, the oscillation time is 0 ms.

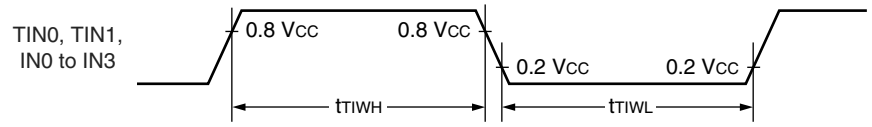
*2: Except for MB90F387S and MB90387S.

*3: Refer to "(1) Clock timing" ratings for t_{CP} (internal operation clock cycle time).

- In sub clock, sub sleep, watch and stop mode



• Timer input timing



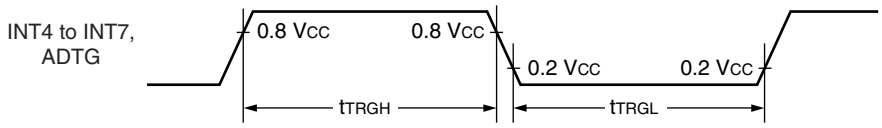
13.4.6 Trigger Input Timing

(V_{CC} = 4.5 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH} t_{TRGL}	INT4 to INT7, ADTG	–	5 t_{CP} *	–	ns	

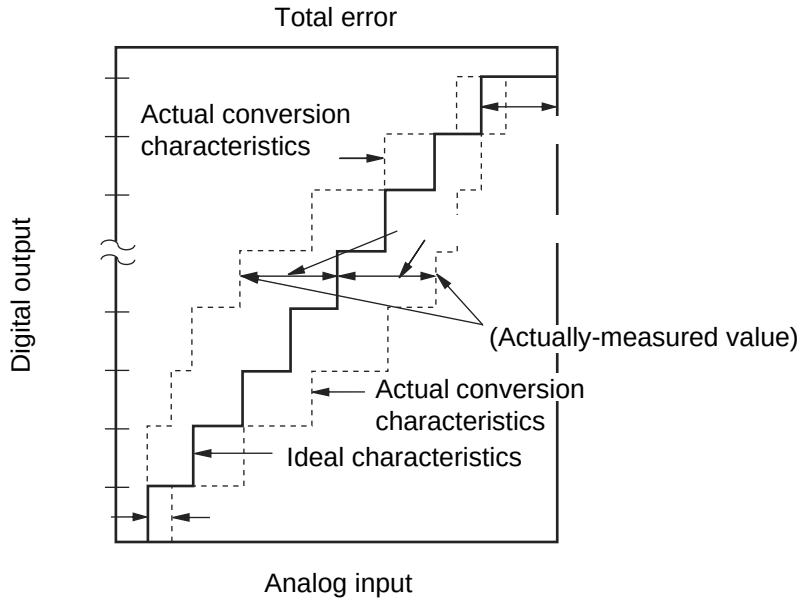
*: Refer to Clock Timing ratings for t_{CP} (internal operation clock cycle time).

• Trigger input timing



13.6 Definition of A/D Converter Terms

Resolution:	Analog variation that is recognized by an A/D converter.
Linear error:	Deviation between a line across zero-transition line (“00 0000 00 0 0” ←→“00 0000 0001”) and full-scale transition line (“11 1111 11 1 0” ←→ “11 1111 1111”) and actual conversion characteristics.
Differential linear error:	Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.
Total error:	Difference between an actual value and an ideal value. A total error includes zero transition error, full-scale transition error, and linear error.



$$\text{Total error of digital output “N”} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}} \quad [\text{LSB}]$$

$$1\ \text{LSB} = (\text{Ideal value})\ \frac{AVR - AV_{SS}}{1024}\ [V]$$

V_{OT} (Ideal value) = AV_{SS} + 0.5 LSB [V]

V_{FST} (Ideal value) = AVR − 1.5 LSB [V]

V_{NT}: A voltage at which digital output transits from $(N\text{-}1)_H$ to N_H.

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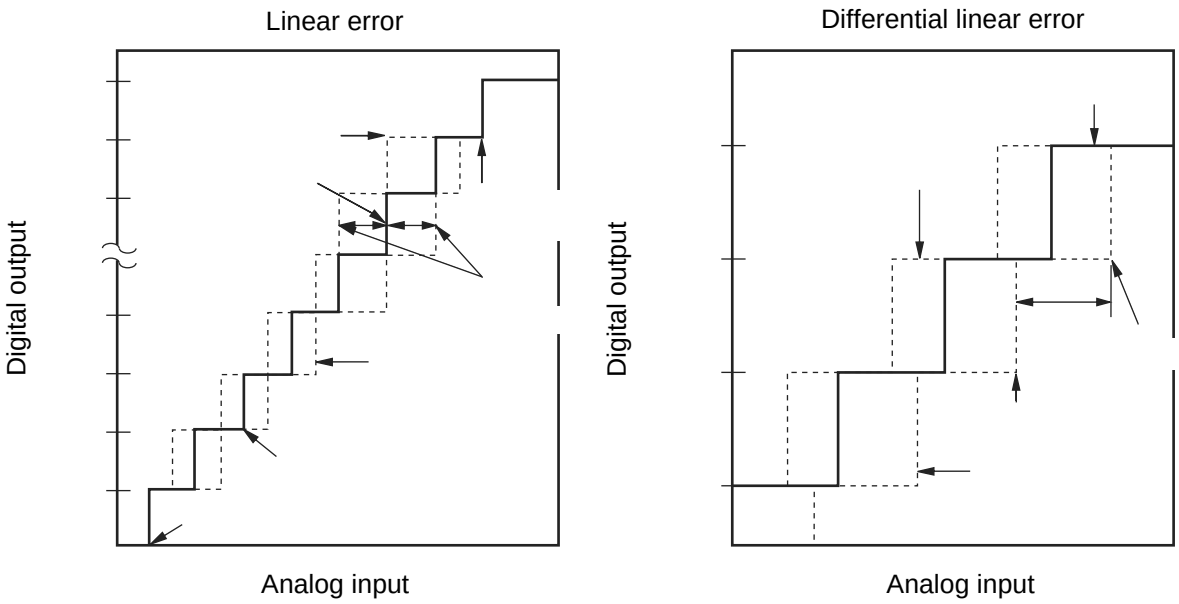


$$\text{Linear error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + V_{OT}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$\text{Differential linear error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\text{LSB}\ [\text{LSB}]$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ [\text{V}]$$

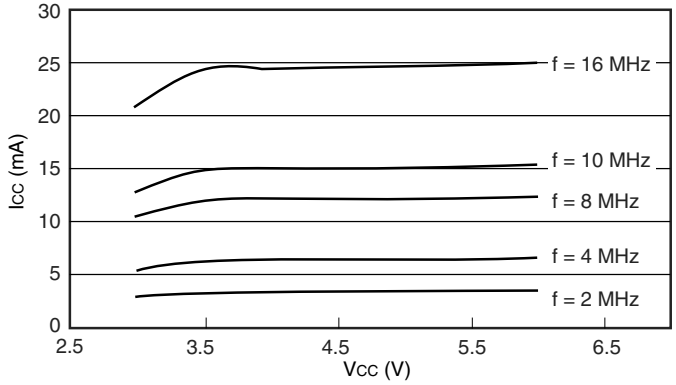
V_{OT}: Voltage at which digital output transits from “000_H” to “001_H.”
V_{FST}: Voltage at which digital output transits from “$3FE_H$” to “$3FF_H$.”

14. Example Characteristics

MB90F387

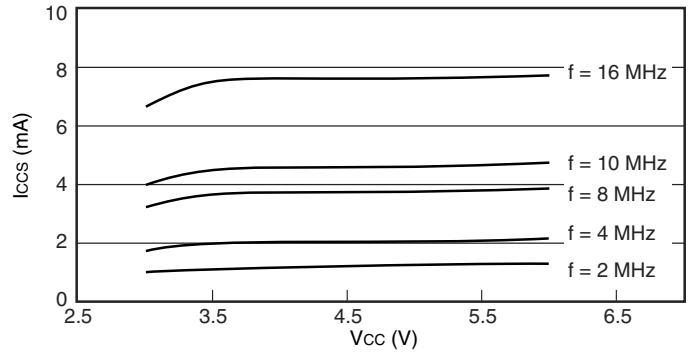
I_{CC} – V_{CC}

T_A = +25 °C, In external clock operation
f = Internal operating frequency



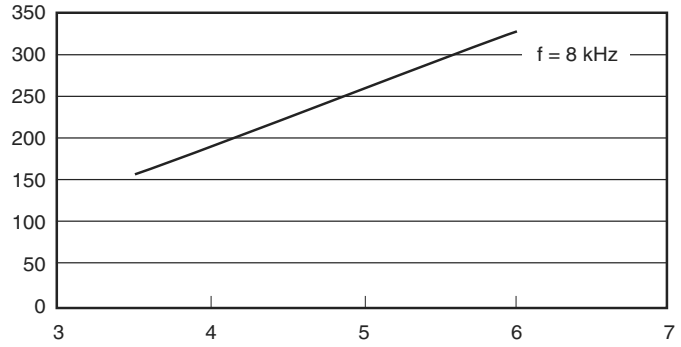
I_{CCS} – V_{CC}

T_A = +25 °C, In external clock operation
f = Internal operating frequency



I_{CCL} – V_{CC}

T_A = +25 °C, In external clock operation
f = Internal operating frequency



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