Infineon Technologies - MB90387SPMT-G-392SN-YE1 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, SCI, UART/USART
Peripherals	POR, WDT
Number of I/O	36
Program Memory Size	64KB (64K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90387spmt-g-392sn-ye1

DTP/External Interrupt: 4 channels, CAN wakeup: 1channel

- Module for activation of expanded intelligent I/O service (EI^2OS), and generation of external interrupt.

Delay Interrupt Generator Module

- Generates interrupt request for task switching.

8/10-bit A/D Converter: 8 channels

- Resolution is selectable between 8-bit and 10-bit.
- Activation by external trigger input is allowed.
- Conversion time: 6.125 μs (at 16 MHz machine clock, including sampling time)

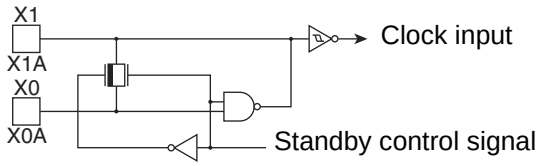
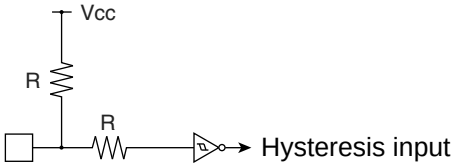
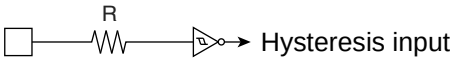
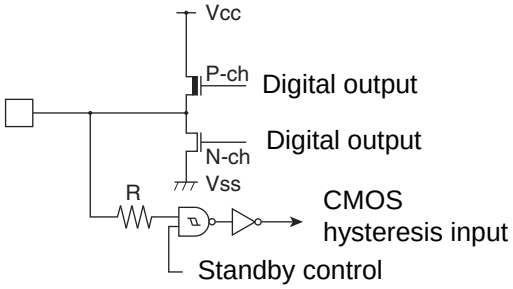
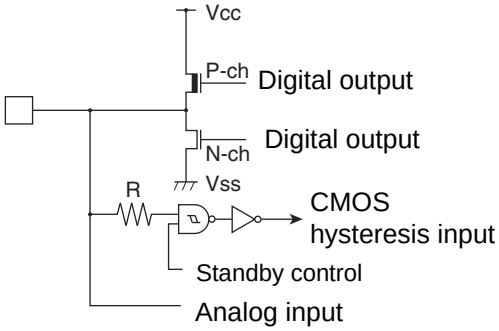
Program Patch Function

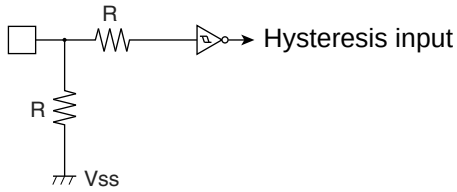
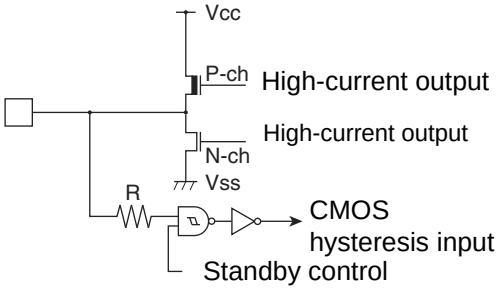
- Address matching detection for 2 address pointers.

5. Pin Description

Pin No.	Pin Name	Circuit Type	Function
1	AVcc	–	Vcc power input pin for A/D converter.
2	AVR	–	Power (Vref+) input pin for A/D converter. Use as input for Vcc or lower.
3 to 10	P50 to P57	E	General-purpose input/output ports.
	AN0 to AN7		Functions as analog input pins for A/D converter. Valid when analog input setting is “enabled.”
11	P37	D	General-purpose input/output port.
	ADTG		Function as an external trigger input pin for A/D converter. Use the pin by setting as input port.
12	P20	D	General-purpose input/output port.
	TIN0		Function as an event input pin for reload timer 0. Use the pin by setting as input port.
13	P21	D	General-purpose input/output port.
	TOT0		Function as an event output pin for reload timer 0. Valid only when output setting is “enabled.”
14	P22	D	General-purpose input/output port.
	TIN1		Function as an event input pin for reload timer 1. Use the pin by setting as input port.
15	P23	D	General-purpose input/output port.
	TOT1		Function as an event output pin for reload timer 1. Valid only when output setting is “enabled.”
16 to 19	P24 to P27	D	General-purpose input/output ports.
	INT4 to INT7		Functions as external interrupt input pins. Use the pins by setting as input port.
20	MD2	F	Input pin for specifying operation mode. Connect directly to Vss.
21	MD1	C	Input pin for specifying operation mode. Connect directly to Vcc.
22	MD0	C	Input pin for specifying operation mode. Connect directly to Vcc.
23	RST	B	External reset input pin.
24	Vcc	–	Power source (5 V) input pin.
25	Vss	–	Power source (0 V) input pin.
26	C	–	Capacitor pin for stabilizing power source. Connect a ceramic capacitor of approximately 0.1 μF.
27	X0	A	Pin for high-rate oscillation.
28	X1	A	Pin for high-rate oscillation.
29 to 32	P10 to P13	D	General-purpose input/output ports.
	IN0 to IN3		Functions as trigger input pins of input capture ch.0 to ch.3. Use the pins by setting as input ports.
33 to 36	P14 to P17	G	General-purpose input/output ports. High-current output ports.
	PPG0 to PPG3		Functions as output pins of PPG timers 01 and 23. Valid when output setting is “enabled.”
37	P40	D	General-purpose input/output port.
	SIN1		Serial data input pin for UART. Use the pin by setting as input port.
38	P41	D	General-purpose input/output port.
	SCK1		Serial clock input pin for UART. Valid only when serial clock input/output setting on UART is “enabled.”

6. I/O Circuit Type

Type	Circuit	Remarks
A		■ High-rate oscillation feedback resistor, approx.1 MΩ ■ Low-rate oscillation feedback resistor, approx.10 MΩ
B		■ Hysteresis input with pull-up resistor. ■ Pull-up resistor, approx.50 kΩ
C		■ Hysteresis input
D		■ CMOS hysteresis input ■ CMOS level output ■ Standby control provided
E		■ CMOS hysteresis input ■ CMOS level output ■ Shared for analog input pin ■ Standby control provided

Type	Circuit	Remarks
F		■ Hysteresis input with pull-down resistor ■ Pull-down resistor, approx. 50 kΩ ■ Flash product is not provided with pull-down resistor.
G		■ CMOS hysteresis input ■ CMOS level output (high-current output) ■ Standby control provided

7. Handling Devices

Do Not Exceed Maximum Rating (preventing “latch up”)

■ On a CMOS IC, latch-up may occur when applying a voltage higher than Vcc or a voltage lower than Vss to input or output pin, which has no middle or high withstand voltage. Latch-up may also occur when a voltage exceeding maximum rating is applied across Vcc pin and Vss pin.

■ Latch-up causes drastic increase of power current, which may lead to destruction of elements by heat. Extreme caution must be taken not to exceed maximum rating.

■ When turning on and off analog power source, take extra care not to apply an analog power voltages (AVcc and AVR) and analog input voltage that are higher than digital power voltage (Vcc).

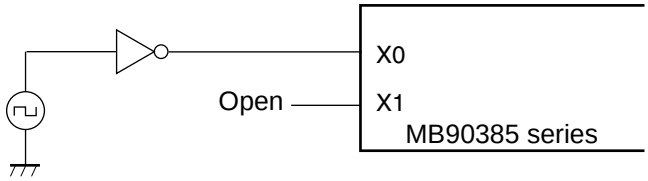
Handling Unused Pins

■ Leaving unused input pins open may cause permanent destruction by malfunction or latch-up. Apply pull-up or pull-down process to the unused pins using resistors of 2 kΩ or higher. Leave unused input/output pins open under output status, or process as input pins if they are under input status.

Using External Clock

■ When using an external clock, drive only X0 pin and leave X1 pin open. An example of using an external clock is shown below.

• Using external clock



Notes When Using No Sub Clock

■ If an oscillator is not connected to X0A and X1A pin, apply pull-down resistor to X0A pin and leave X1A pin open.

About Power Supply Pins

■ If two or more Vcc and Vss pins exist, the pins that should be at the same potential are connected to each other inside the device. For reducing unwanted emissions and preventing malfunction of strobe signals caused by increase of ground level, however, be sure to connect the Vcc and Vss pins to the power source and the ground externally.

■ Pay attention to connect a power supply to Vcc and Vss of MB90385 series device in a lowest-possible impedance.

■ Near pins of MB90385 series device, connecting a bypass capacitor is recommended at 0.1 μF across Vcc pin and Vss pin.

Crystal Oscillator Circuit

■ Noises around X0 and X1 pins cause malfunctions on a MB90385 series device. Design a print circuit so that X0 and X1 pins, an crystal oscillator (or a ceramic oscillator), and bypass capacitor to the ground become as close as possible to each other. Furthermore, avoid wires to X0 and X1 pins crossing each other as much as possible.

■ Print circuit designing that surrounds X0 and X1 pins with grounding wires, which ensures stable operation, is strongly recommended.

Caution on Operations during PLL Clock Mode

■ If the PLL clock mode is selected, the microcontroller attempt to be working with the self-oscillating circuit even when there is no external oscillator or external clock input is stopped. Performance of this operation, however, cannot be guaranteed.

Sequence of Turning on Power of A/D Converter and Applying Analog Input

■ Be sure to turn on digital power (Vcc) before applying signals to the A/D converter and applying analog input signals (AN0 to AN7 pins).

■ Be sure to turn off the power of A/D converter and analog input before turning off the digital power source.

■ Be sure not to apply AVR exceeding AVcc when turning on and off. (No problems occur if analog and digital power is turned on and off simultaneously.)

Handling Pins When A/D Converter is Not Used

■ If the A/D converter is not used, connect the pins under the following conditions: “AVcc=AVR=Vcc,” and “AVss=Vss”

Note on Turning on Power

■ For preventing malfunctions on built-in step-down circuit, maintain a minimum of 50 μs of voltage rising time (between 0.2 V and 2.7V) when turning on the power.

Stabilization of Supply Voltage

■ A sudden change in the supply voltage may cause the device to malfunction even within the specified V_{CC} supply voltage operating range. Therefore, the V_{CC} supply voltage should be stabilized.
For reference, the supply voltage should be controlled so that V_{CC} ripple variations (peak-to-peak values) at commercial frequencies (50 Hz / 60 Hz) fall below 10% of the standard V_{CC} supply voltage and the coefficient of fluctuation does not exceed 0.1 V/ms at instantaneous power switching.

Address	Register Abbreviation	Register	Read/ Write	Resource	Initial Value
000038H to 00003FH	(Reserved area) *				
000040H	PPGC0	PPG0 operation mode control register	R/W, W	8/16-bit PPG timer 0/1	0X000XX1B
000041H	PPGC1	PPG1 operation mode control register	R/W, W		0X000001B
000042H	PPG01	PPG0/1 count clock selection register	R/W		000000XXB
000043H	(Reserved area) *				
000044H	PPGC2	PPG2 operation mode control register	R/W, W	8/16-bit PPG timer 2/3	0X000XX1B
000045H	PPGC3	PPG3 operation mode control register	R/W, W		0X000001B
000046H	PPG23	PPG2/3 count clock selection register	R/W		000000XXB
000047H to 00004FH	(Reserved area) *				
000050H	IPCP0	Input capture data register 0	R	16-bit input/output timer	XXXXXXXXB
000051H					XXXXXXXXB
000052H	IPCP1	Input capture data register 1	R		XXXXXXXXB
000053H					XXXXXXXXB
000054H	ICS01	Input capture control status register	R/W		00000000B
000055H	ICS23				00000000B
000056H	TCDT	Timer counter data register	R/W		00000000B
000057H					00000000B
000058H	TCCS	Timer counter control status register	R/W		00000000B
000059H	(Reserved area) *				
00005AH	IPCP2	Input capture data register 2	R	16-bit input/output timer	XXXXXXXXB
00005BH					XXXXXXXXB
00005CH	IPCP3	Input capture data register 3	R		XXXXXXXXB
00005DH					XXXXXXXXB
00005EH to 000065H	(Reserved area) *				
000066H	TMCSR0	Timer control status register	R/W	16-bit reload timer 0	00000000B
000067H			R/W		XXXX0000B
000068H	TMCSR1		R/W	16-bit reload timer 1	00000000B
000069H			R/W		XXXX0000B
00006AH to 00006EH	(Reserved area) *				
00006FH	ROMM	ROM mirroring function selection register	W	ROM mirroring function selection module	XXXXXXX1B
000070H to 00007FH	(Reserved area) *				
000080H	BVALR	Message buffer enabling register	R/W	CAN controller	00000000B
000081H	(Reserved area) *				
000082H	TREQR	Send request register	R/W	CAN controller	00000000B

Address	Register Abbreviation	Register	Read/ Write	Resource	Initial Value
003910H	PRLL0	PPG0 reload register L	R/W	8/16-bit PPG timer	XXXXXXXXB
003911H	PRLH0	PPG0 reload register H	R/W		XXXXXXXXB
003912H	PRLL1	PPG1 reload register L	R/W		XXXXXXXXB
003913H	PRLH1	PPG1 reload register H	R/W		XXXXXXXXB
003914H	PRLL2	PPG2 reload register L	R/W		XXXXXXXXB
003915H	PRLH2	PPG2 reload register H	R/W		XXXXXXXXB
003916H	PRLL3	PPG3 reload register L	R/W		XXXXXXXXB
003917H	PRLH3	PPG3 reload register H	R/W		XXXXXXXXB
003918H to 00392FH	(Reserved area) *				
003930H to 003BFFH	(Reserved area) *				
003C00H to 003C0FH	RAM (General-purpose RAM)				
003C10H to 003C13H	IDR0	ID register 0	R/W	CAN controller	XXXXXXXXB to XXXXXXXXB
003C14H to 003C17H	IDR1	ID register 1	R/W		XXXXXXXXB to XXXXXXXXB
003C18H to 003C1BH	IDR2	ID register 2	R/W		XXXXXXXXB to XXXXXXXXB
003C1CH to 003C1FH	IDR3	ID register 3	R/W		XXXXXXXXB to XXXXXXXXB
003C20H to 003C23H	IDR4	ID register 4	R/W		XXXXXXXXB to XXXXXXXXB
003C24H to 003C27H	IDR5	ID register 5	R/W		XXXXXXXXB to XXXXXXXXB
003C28H to 003C2BH	IDR6	ID register 6	R/W		XXXXXXXXB to XXXXXXXXB
003C2CH to 003C2FH	IDR7	ID register 7	R/W		XXXXXXXXB to XXXXXXXXB
003C30H, 003C31H	DLCR0	DLC register 0	R/W		XXXXXXXXB, XXXXXXXXB
003C32H, 003C33H	DLCR1	DLC register 1	R/W		XXXXXXXXB, XXXXXXXXB
003C34H, 003C35H	DLCR2	DLC register 2	R/W		XXXXXXXXB, XXXXXXXXB
003C36H, 003C37H	DLCR3	DLC register 3	R/W		XXXXXXXXB, XXXXXXXXB

11. Interrupt Sources, Interrupt Vectors, And Interrupt Control Registers

Interrupt Source	EI²OS Readiness	Interrupt Vector			Interrupt Control Register		Priority*3
		Number		Address	ICR	Address	
Reset	×	#08	08H	FFFFDCH	–	–	High
INT 9 instruction	×	#09	09H	FFFFD8H	–	–	↑
Exceptional treatment	×	#10	0AH	FFFFD4H	–	–	
CAN controller reception completed (RX)	´	#11	0BH	FFFFD0H	ICR00	0000B0H*1	
CAN controller transmission completed (TX) / Node status transition (NS)	´	#12	0CH	FFFFCCH			
Reserved	×	#13	0DH	FFFFC8H	ICR01	0000B1H	
Reserved	×	#14	0EH	FFFFC4H			
CAN wakeup	Δ	#15	0FH	FFFFC0H	ICR02	0000B2H*1	
Time-base timer	×	#16	10H	FFFFBCH			
16-bit reload timer 0	Δ	#17	11H	FFFFB8H	ICR03	0000B3H*1	
8/10-bit A/D converter	Δ	#18	12H	FFFFB4H			
16-bit free-run timer overflow	Δ	#19	13H	FFFFB0H	ICR04	0000B4H*1	
Reserved	×	#20	14H	FFFFACH			
Reserved	×	#21	15H	FFFFA8H	ICR05	0000B5H*1	
PPG timer ch0, ch1 underflow	´	#22	16H	FFFFA4H			
Input capture 0-input	Δ	#23	17H	FFFFA0H	ICR06	0000B6H*1	
External interrupt (INT4/INT5)	Δ	#24	18H	FFFF9CH			
Input capture 1-input	Δ	#25	19H	FFFF98H	ICR07	0000B7H*2	
PPG timer ch2, ch3 underflow	´	#26	1AH	FFFF94H			
External interrupt (INT6/INT7)	Δ	#27	1BH	FFFF90H	ICR08	0000B8H*1	
Watch timer	Δ	#28	1CH	FFFF8CH			
Reserved	×	#29	1DH	FFFF88H	ICR09	0000B9H*1	
Input capture 2-input Input capture 3-input	´	#30	1EH	FFFF84H			
Reserved	×	#31	1FH	FFFF80H	ICR10	0000BAH*1	
Reserved	×	#32	20H	FFFF7CH			
Reserved	×	#33	21H	FFFF78H	ICR11	0000BBH*1	
Reserved	×	#34	22H	FFFF74H			
Reserved	×	#35	23H	FFFF70H	ICR12	0000BCH*1	↓
16-bit reload timer 1	○	#36	24H	FFFF6CH			Low

12.2 Time-Base Timer

The time-base time is an 18-bit free-run counter (time-base timer counter) that counts up in synchronization with the main clock (dividing main oscillation clock by 2).

- Four choices of interval time are selectable, and generation of interrupt request is allowed for each interval time.
- Provides operation clock signal to oscillation stabilizing wait timer and peripheral functions.

Interval Timer Function

- When the counter of time-base timer reaches an interval time specified by interval time selection bit (TBTC:TBC1, TBC0), an overflow (carrying-over) occurs (TBTC: TBOF=1) and interrupt request is generated.
- If an interrupt by overflow is permitted (TBTC: TBIE=1), an interrupt is generated when overflow occurs (TBTC: TBOF=1).
- The following four interval time settings are selectable:

Interval Time of Time-base Timer

Count Clock	Interval Time
2/HCLK (0.5 μs)	2^{12}/HCLK (Approx. 1.0 ms)
	2^{14}/HCLK (Approx. 4.1 ms)
	2^{16}/HCLK (Approx. 16.4 ms)
	2^{19}/HCLK (Approx. 131.1 ms)

HCLK: Oscillation clock

Values in parentheses “( )” are those under operation of 4-MHz oscillation clock.

12.3 Watchdog Timer

The watchdog timer is a 2-bit counter that uses time-base timer or watch timer as count clock. If the counter is not cleared within an interval time, CPU is reset.

Watchdog Timer Functions

- The watchdog timer is a timer counter that prevents runaway of a program. Once a watchdog timer is activated, the counter of watchdog timer must always be cleared within a specified time of interval. If specified interval time elapses without clearing the counter of a watchdog timer, CPU resetting occurs. This is the function of a watchdog timer.
- The interval time of a watchdog timer is determined by a clock cycle, which is input as a count clock. Watchdog resetting occurs between a minimum time and a maximum time specified.
- The output target of a clock source is specified by the watchdog clock selection bit (WTC: WDCS) in the watch timer control register.
- Interval time of a watchdog timer is specified by the time-base timer output selection bit / watch timer output selection bit (WDTC: WT1, WT0) in the watchdog timer control register.

Interval Timer of Watchdog Timer

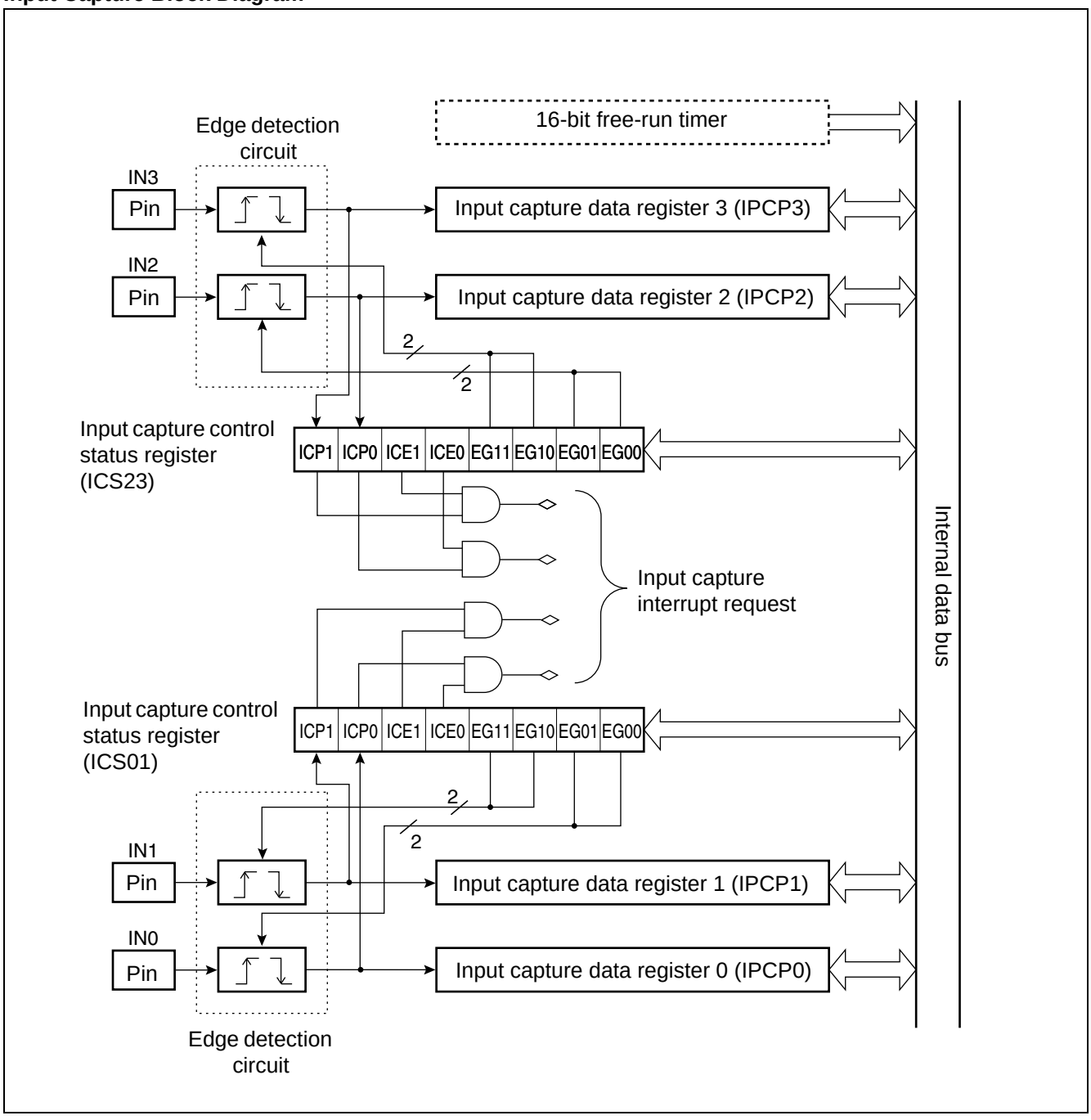
Min	Max	Clock Cycle	Min	Max	Clock Cycle
Approx. 3.58 ms	Approx. 4.61 ms	$(2^{14}\pm2^{11})$ /HCLK	Approx. 0.457 s	Approx. 0.576 s	$(2^{12}\pm2^{9})$ /SCLK
Approx. 14.33 ms	Approx. 18.3 ms	$(2^{16}\pm2^{13})$ /HCLK	Approx. 3.584 s	Approx. 4.608 s	$(2^{15}\pm2^{12})$ /SCLK
Approx. 57.23 ms	Approx. 73.73 ms	$(2^{18}\pm2^{15})$ /HCLK	Approx. 7.168 s	Approx. 9.216 s	$(2^{16}\pm2^{13})$ /SCLK
Approx. 458.75 ms	Approx. 589.82 ms	$(2^{21}\pm2^{18})$ /HCLK	Approx. 14.336 s	Approx. 18.432 s	$(2^{17}\pm2^{14})$ /SCLK

HCLK: Oscillation clock (4 MHz), CSCLK: Sub clock (8.192 kHz)

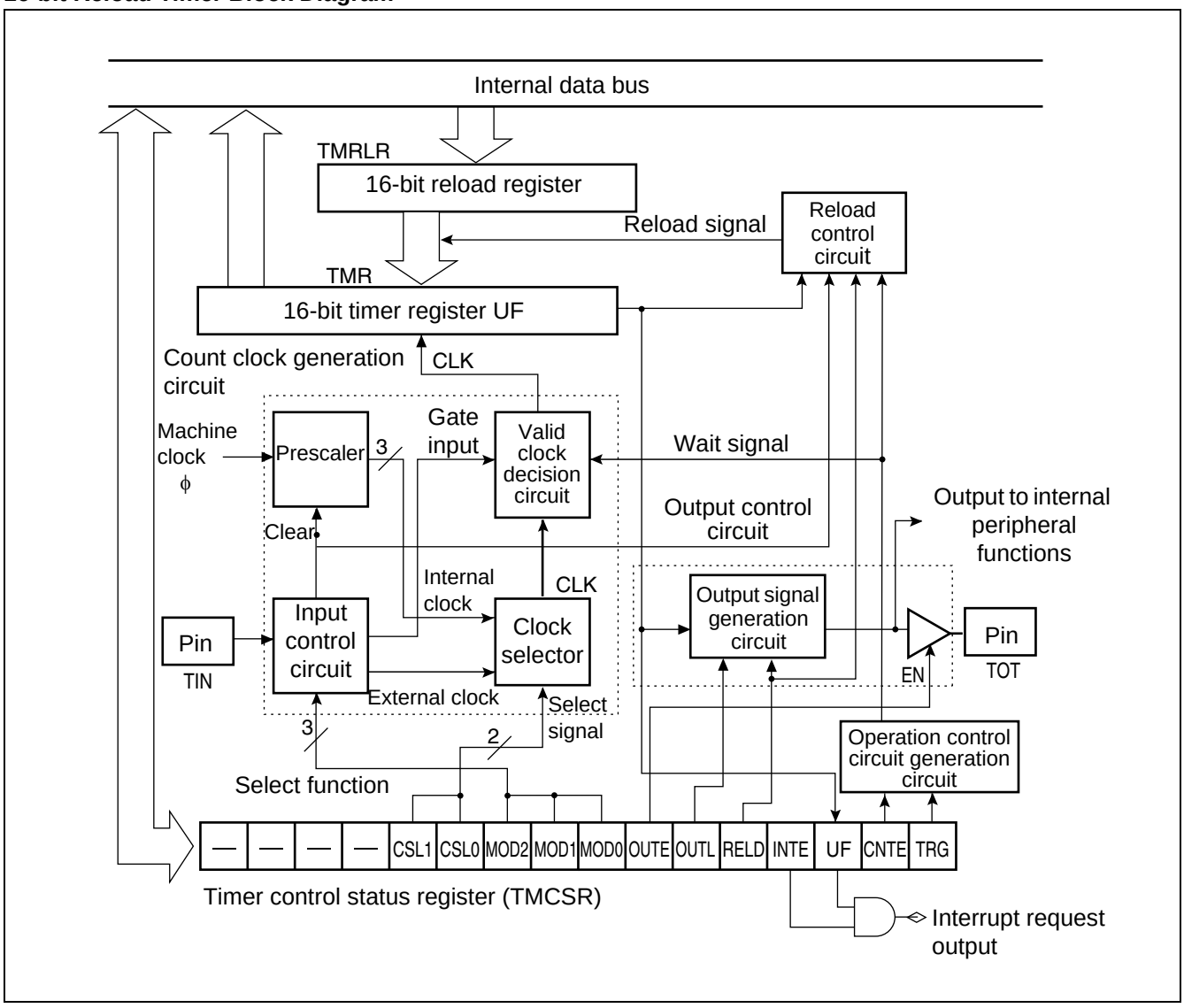
Notes:

- If the time-base timer is cleared when watchdog timer count clock is used as time base timer output (carry-over signal), watchdog reset time may become longer.
- When using the sub clock as machine clock, be sure to specify watchdog timer clock source selection bit (WDCS) in watch timer control register (WTC) at “0,” selecting output of watch timer.

Input Capture Block Diagram



16-bit Reload Timer Block Diagram



12.6 Watch Timer Outline

The watch timer is a 15-bit free-run counter that increments in synchronization with sub clock.

- Interval time is selectable among 7 choices, and generation of interrupt request is allowed for each interval.
- Provides operation clock to the subclock oscillation stabilizing wait timer and watchdog timer.
- Always uses subclock as a count clock regardless of settings of clock selection register (CKSCR).

Interval Timer Function

- In the watch timer, a bit corresponding to the interval time overflows (carry-over) when an interval time, which is specified by interval time selection bit, is reached. Then overflow flag bit is set (WTC: WTOF=1).
- If an interrupt by overflow is permitted (WTC: WTIE=1), an interrupt request is generated upon setting an overflow flag bit.
- Interval time of watch timer is selectable among the following seven choices:

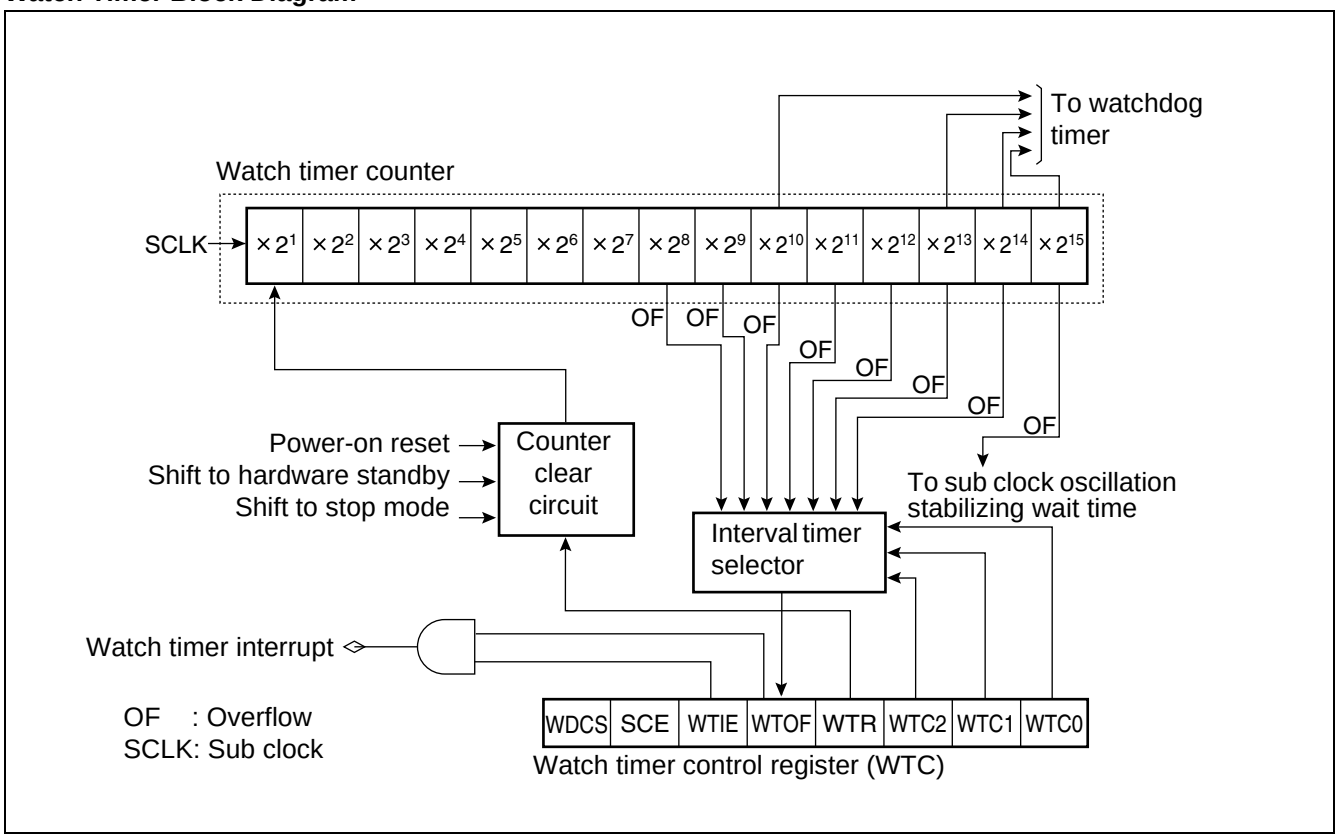
Interval Time of Watch Timer

Sub Clock Cycle	Interval Time
1/SCLK (122 μs)	2^8/SCLK (31.25 ms)
	2^9/SCLK (62.5 ms)
	2^{10}/SCLK (125 ms)
	2^{11}/SCLK (250 ms)
	2^{12}/SCLK (500 ms)
	2^{13}/SCLK (1.0 s)
	2^{14}/SCLK (2.0 s)

SCLK: Sub clock frequency

Values in parentheses “( )” are calculation when operating with 8.192 kHz clock.

Watch Timer Block Diagram



Actual interrupt request number of watch timer is as follows:
Interrupt request number: #28 ($1C_H$)

Watch Timer Counter

A 15-bit up counter that uses sub clock (SCLK) as a count clock.

Counter Clear Circuit

A circuit that clears the watch timer counter.

12.7 8/16-bit PPG Timer Outline

The 8/16-bit PPG timer is a 2-channel reload timer module (PPG0 and PPG1) that allows outputting pulses of arbitrary cycle and duty cycle. Combination of the two channels allows selection among the following operations:

- 8-bit PPG output 2-channel independent operation mode
- 16-bit PPG output operation mode
- 8-bit and 8-bit PPG output operation mode

MB90385 series device has two 8/16-bit built-in PPG timers. This section describes functions of PPG0/1. PPG2/3 have the same functions as those of PPG0/1.

Functions of 8/16-bit PPG Timer

The 8/16-bit PPG timer is composed of four 8-bit reload register (PRLH0/PRLL0, PRLH1/PRLL1) and two PPG down counters (PCNT0, PCNT1).

- Widths of “H” and “L” in output pulse are specifiable independently. Cycle and duty factor of output pulse is specifiable arbitrarily.
- Count clock is selectable among 6 internal clocks.
- The timer is usable as an interval timer, by generating interrupt requests for each interval.
- The time is usable as a D/A converter, with an external circuit.

12.9 DTP/External Interrupt and CAN Wakeup Outline

DTP/external interrupt transfers an interrupt request generated by an external peripheral device or a data transmission request to CPU, generating external interrupt request and activating expanded intelligent I/O service. Input RX of CAN controller is used as external interrupt input.

DTP/External Interrupt and CAN Wakeup Function

An interrupt request input from external peripheral device to external input pins (INT7 to INT4) and RX pin, just as interrupt request of peripheral device, generates an interrupt request. The interrupt request generates an external interrupt and activates expanded intelligent I/O service (EI^2OS).

If the expanded intelligent I/O service (EI^2OS) has been disabled by interrupt control register (ICR: ISE=0), external interrupt function is enabled and branches to interrupt processing.

If the EI^2OS has been enabled, (ICR: ISE=1), DTP function is enabled and automatic data transmission is performed by EI^2OS. After performing specified number of data transmission processes, the process branches to interrupt processing.

Table 12-2. DTP/External Interrupt and CAN Wakeup Outline

	External Interrupt	DTP Function
Input pin	5 pins (RX, and INT4 to INT7)	
Interrupt cause	Specify for each pin with detection level setting register (ELVR).	
	Input of “H” level/“L” level/rising edge/falling edge.	Input of “H” level/ “L” level
Interrupt number	#15 ($0F_H$), #24 (18_H), #27 ($1B_H$)	
Interrupt control	Enabling or disabling output of interrupt request, using DTP/external interrupt permission register (ENIR).	
Interrupt flag	Retaining interrupt cause with DTP/external interrupt cause register (EIRR).	
Process selection	Disable EI^2OS (ICR: ISE=0)	Enable EI^2OS (ICR: ISE=1)
Process	Branch to external interrupt process	After automatic data transmission by EI^2OS for specified number of times, branch to interrupt process.

12.10 8/10-bit A/D Converter

The 8/10-bit A/D converter converts an analog input voltage into 8-bit or 10/bit digital value, using the RC-type successive approximation conversion method.

- Input signal is selected among 8 channels of analog input pins.
- Activation trigger is selected among software trigger, internal timer output, and external trigger.

Functions of 8/10-bit A/D Converter

The 8/10-bit A/D converter converts an analog voltage (input voltage) input to analog input pin into an 8-bit or 10-bit digital value (A/D conversion).

The 8/10-bit A/D converter has the following functions:

- A/D conversion takes a minimum of 6.12 μs* for 1 channel, including sampling time. (A/D conversion)
- Sampling of one channel takes a minimum of 2.0 μs*.
- RC-type successive approximation conversion method, with sample & hold circuit is used for conversion.
- Resolution of either 8 bits or 10 bits is specifiable.
- A maximum of 8 channels of analog input pins are allowed for use.
- Generation of interrupt request is allowed, by storing A/D conversion result in A/D data register.
- Activation of EI^{2}OS is allowed upon occurrence of an interrupt request. With use of EI^{2}OS, data loss is avoided even if A/D conversion is performed successively.
- An activation trigger is selectable among software trigger, internal timer output, and external trigger (fall edge).

: When operating with 16 MHz machine clock

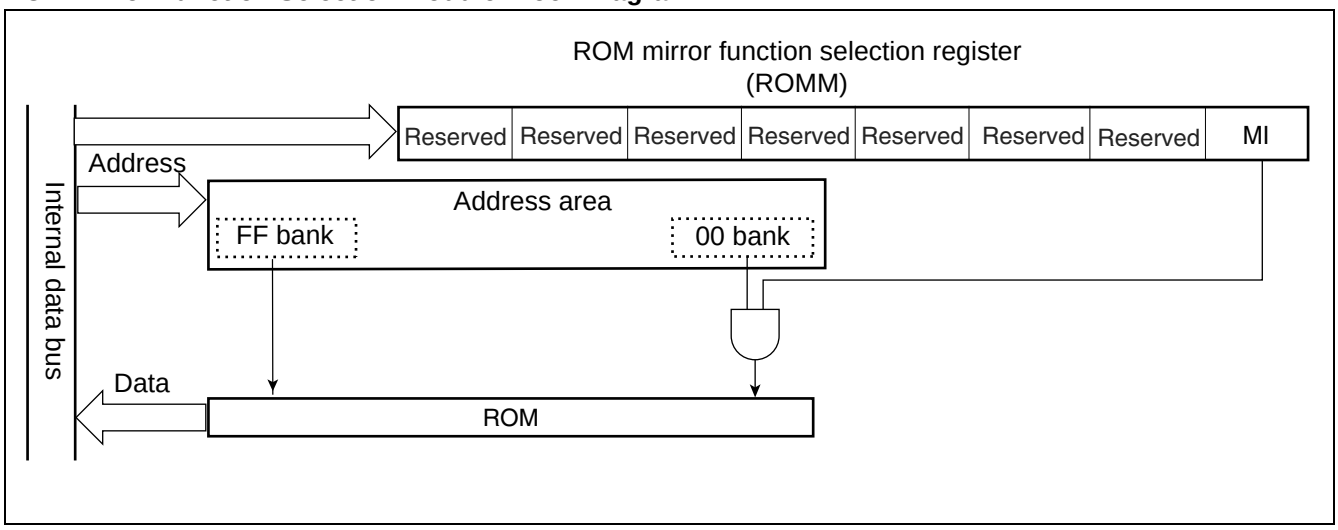
8/10-bit A/D Converter Conversion Mode

Conversion Mode	Description
Singular conversion mode	The A/D conversion is performed form a start channel to an end channel sequentially. Upon completion of A/D conversion on an end channel, A/D conversion function stops.
Sequential conversion mode	The A/D conversion is performed form a start channel to an end channel sequentially. Upon completion of A/D conversion on an end channel, A/D conversion function resumes from the start channel.
Pausing conversion mode	The A/D conversion is performed by pausing at each channel. Upon completion of A/D conversion on an end channel, A/D conversion and pause functions resume from the start channel.

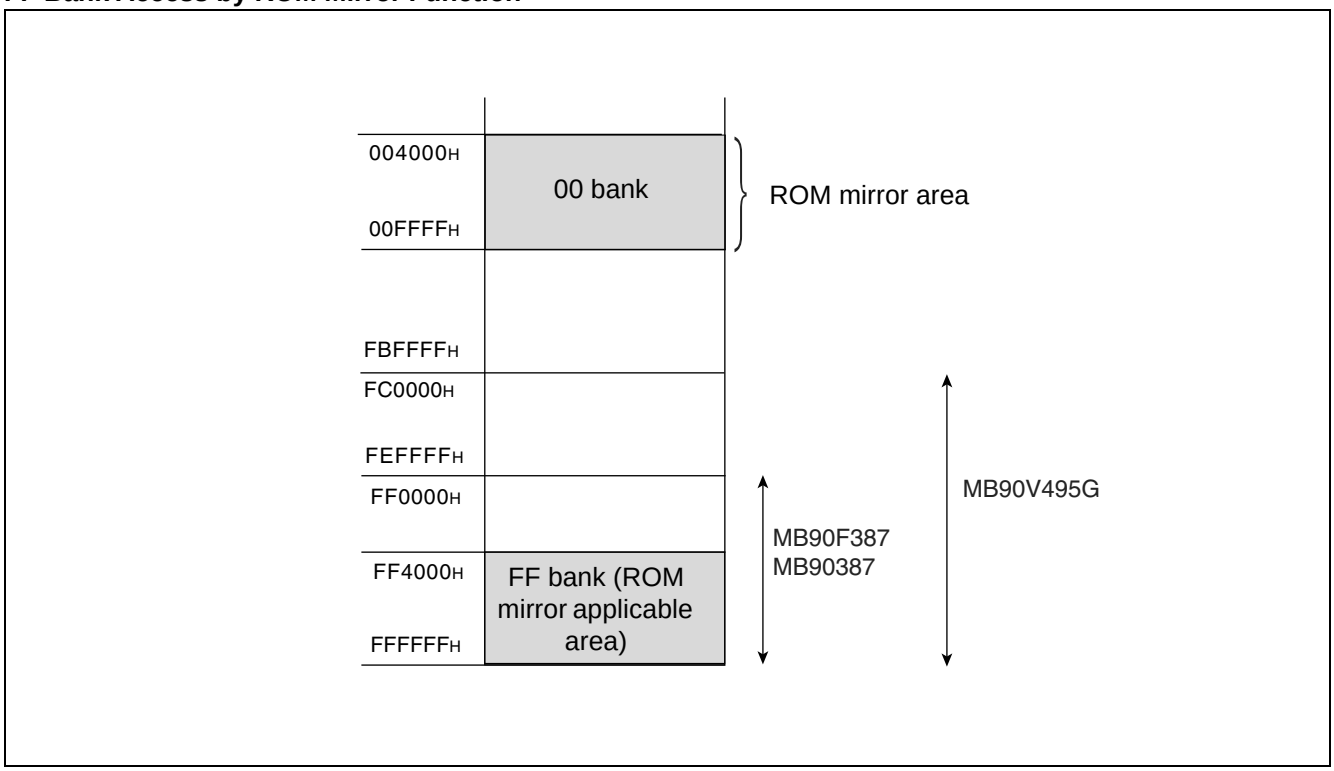
12.14 ROM Mirror Function Selection Module Outline

The ROM mirror function selection module sets the data in ROM assigned to FF bank so that the data is read by access to 00 bank.

ROM Mirror Function Selection Module Block Diagram



FF Bank Access by ROM Mirror Function



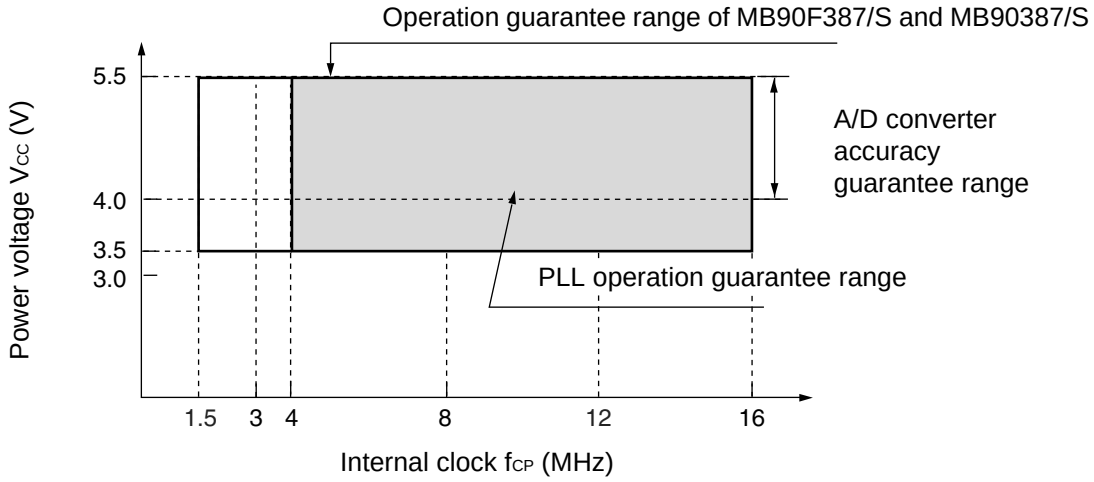
Sector Configuration of 512 Kbit Flash Memory

Flash memory	CPU address	Writer address*
SA0 (32 Kbytes)	FF0000H FF7FFFH	70000H 77FFFH
SA1 (8 Kbytes)	FF8000H FF9FFFH	78000H 79FFFH
SA2 (8 Kbytes)	FFA000H FFBFFFH	7A000H 7BFFFH
SA3 (16 Kbytes)	FFC000H FFFFFFH	7C000H 7FFFFH

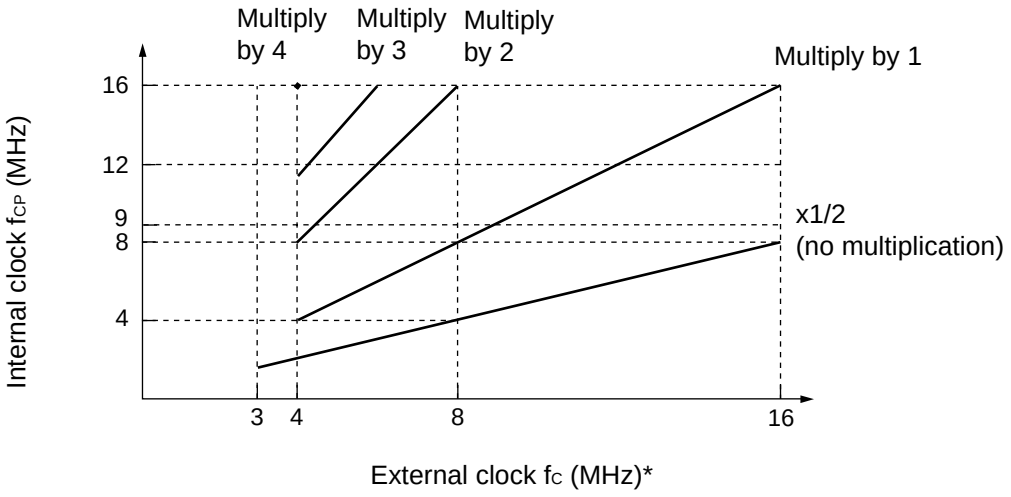
*: “Writer address” is an address equivalent to CPU address, which is used when data is written on Flash memory, using parallel writer. When writing/deleting data with general-purpose writer, the writer address is used for writing and deleting.

• PLL operation guarantee range

Relation between internal operation clock frequency and power supply voltage



Relation among external clock frequency and internal clock frequency



*: fc is 8 MHz at maximum when crystal or ceramic resonator circuit is used.