Infineon Technologies - MB90387SPMT-GS-138 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, SCI, UART/USART
Peripherals	POR, WDT
Number of I/O	36
Program Memory Size	64KB (64K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90387spmt-gs-138

MB90387/387S/F387/F387S
MB90V495G

16-bit Microcontrollers
F²MC-16LX MB90385 Series

MB90385 series devices are general-purpose high-performance 16-bit micro controllers designed for process control of consumer products, which require high-speed real-time processing. The devices of this series have the built-in full-CAN interface.
The system, inheriting the architecture of F²MC family, employs additional instruction ready for high-level languages, expanded addressing mode, enhanced multiply-divide instructions, and enriched bit-processing instructions. Furthermore, employment of 32-bit accumulator achieves processing of long-word data (32 bits).
The peripheral resources of MB90385 series include the following:
8/10-bit A/D converter, UART (SCI), 8/16-bit PPG timer, 16-bit input-output timer (16-bit free-run timer, input capture 0, 1, 2, 3 (ICU)), and CAN controller.

Features

Clock

- Built-in PLL clock frequency multiplication circuit
- Selection of machine clocks (PLL clocks) is allowed among frequency division by two on oscillation clock, and multiplication of 1 to 4 times of oscillation clock (for 4-MHz oscillation clock, 4 MHz to 16 MHz).
- Operation by sub-clock (8.192 kHz) is allowed. (MB90387, MB90F387)
- Minimum execution time of instruction: 62.5 ns (when operating with 4-MHz oscillation clock, and 4-time multiplied PLL clock).

16 Mbyte CPU memory Space

- 24-bit internal addressing

Instruction System Best Suited to Controller

- Wide choice of data types (bit, byte, word, and long word)
- Wide choice of addressing modes (23 types)
- Enhanced multiply-divide instructions and RETI instructions
- Enhanced high-precision computing with 32-bit accumulator

Instruction System Compatible with High-level Language (C language) and Multitask

- Employing system stack pointer
- Enhanced various pointer indirect instructions
- Barrel shift instructions

Increased Processing Speed

- 4-byte instruction queue

Powerful Interrupt Function with 8 Levels and 34 Factors

Automatic Data Transfer Function Independent of CPU

- Expanded intelligent I/O service function (EI² OS): Maximum of 16 channels

Low Power Consumption (standby) Mode

- Sleep mode (a mode that halts CPU operating clock)
- Time-base timer mode (a mode that operates oscillation clock, sub clock, time-base timer and watch timer only)
- Watch mode (a mode that operates sub clock and watch timer only)
- Stop mode (a mode that stops oscillation clock and sub clock)
- CPU blocking operation mode

Process

- CMOS technology

I/O Port

- General-purpose input/output port (CMOS output):

  MB90387, MB90F387: 34 ports (including 4 high-current output ports)
  MB90387S, MB90F387S: 36 ports (including 4 high-current output ports)

Timer

- Time-base timer, watch timer, watchdog timer: 1 channel
- 8/16-bit PPG timer: 8-bit x 4 channels, or 16-bit x 2 channels
- 16-bit reload timer: 2 channels
- 16-bit input/output timer
  - ❒ 16-bit free run timer: 1 channel
  - ❒ 16-bit input capture: (ICU): 4 channels

  Interrupt request is issued upon latching a count value of 16-bit free run timer by detection of an edge on pin input.

CAN Controller: 1 channel

- Compliant with Ver2.0A and Ver2.0B CAN specifications
- 8 built-in message buffers
- Transmission rate of 10 kbps to 1 Mbps (by 16 MHz machine clock)
- CAN wake-up

UART (SCI): 1 channel

- Equipped with full-duplex double buffer
- Clock-asynchronous or clock-synchronous serial transmission is available.

DTP/External Interrupt: 4 channels, CAN wakeup: 1channel

- Module for activation of expanded intelligent I/O service (EI^2OS), and generation of external interrupt.

Delay Interrupt Generator Module

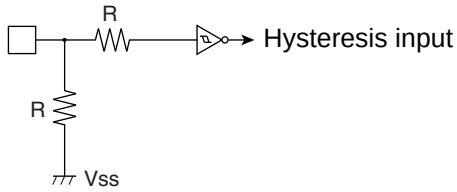
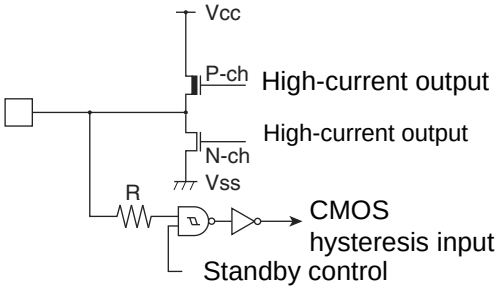
- Generates interrupt request for task switching.

8/10-bit A/D Converter: 8 channels

- Resolution is selectable between 8-bit and 10-bit.
- Activation by external trigger input is allowed.
- Conversion time: 6.125 μs (at 16 MHz machine clock, including sampling time)

Program Patch Function

- Address matching detection for 2 address pointers.

Type	Circuit	Remarks
F		■ Hysteresis input with pull-down resistor ■ Pull-down resistor, approx. 50 kΩ ■ Flash product is not provided with pull-down resistor.
G		■ CMOS hysteresis input ■ CMOS level output (high-current output) ■ Standby control provided

7. Handling Devices

Do Not Exceed Maximum Rating (preventing “latch up”)

■ On a CMOS IC, latch-up may occur when applying a voltage higher than Vcc or a voltage lower than Vss to input or output pin, which has no middle or high withstand voltage. Latch-up may also occur when a voltage exceeding maximum rating is applied across Vcc pin and Vss pin.

■ Latch-up causes drastic increase of power current, which may lead to destruction of elements by heat. Extreme caution must be taken not to exceed maximum rating.

■ When turning on and off analog power source, take extra care not to apply an analog power voltages (AVcc and AVR) and analog input voltage that are higher than digital power voltage (Vcc).

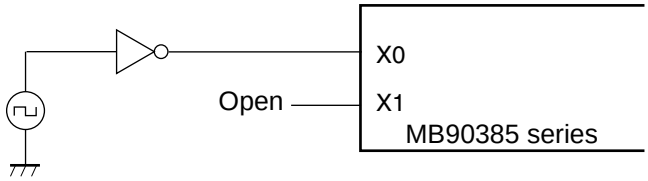
Handling Unused Pins

■ Leaving unused input pins open may cause permanent destruction by malfunction or latch-up. Apply pull-up or pull-down process to the unused pins using resistors of 2 kΩ or higher. Leave unused input/output pins open under output status, or process as input pins if they are under input status.

Using External Clock

■ When using an external clock, drive only X0 pin and leave X1 pin open. An example of using an external clock is shown below.

• Using external clock



Address	Register Abbreviation	Register	Read/ Write	Resource	Initial Value
000038H to 00003FH	(Reserved area) *				
000040H	PPGC0	PPG0 operation mode control register	R/W, W	8/16-bit PPG timer 0/1	0X000XX1B
000041H	PPGC1	PPG1 operation mode control register	R/W, W		0X000001B
000042H	PPG01	PPG0/1 count clock selection register	R/W		000000XXB
000043H	(Reserved area) *				
000044H	PPGC2	PPG2 operation mode control register	R/W, W	8/16-bit PPG timer 2/3	0X000XX1B
000045H	PPGC3	PPG3 operation mode control register	R/W, W		0X000001B
000046H	PPG23	PPG2/3 count clock selection register	R/W		000000XXB
000047H to 00004FH	(Reserved area) *				
000050H	IPCP0	Input capture data register 0	R	16-bit input/output timer	XXXXXXXXB
000051H					XXXXXXXXB
000052H	IPCP1	Input capture data register 1	R		XXXXXXXXB
000053H					XXXXXXXXB
000054H	ICS01	Input capture control status register	R/W		00000000B
000055H	ICS23				00000000B
000056H	TCDT	Timer counter data register	R/W		00000000B
000057H					00000000B
000058H	TCCS	Timer counter control status register	R/W		00000000B
000059H	(Reserved area) *				
00005AH	IPCP2	Input capture data register 2	R	16-bit input/output timer	XXXXXXXXB
00005BH					XXXXXXXXB
00005CH	IPCP3	Input capture data register 3	R		XXXXXXXXB
00005DH					XXXXXXXXB
00005EH to 000065H	(Reserved area) *				
000066H	TMCSR0	Timer control status register	R/W	16-bit reload timer 0	00000000B
000067H			R/W		XXXX0000B
000068H	TMCSR1		R/W	16-bit reload timer 1	00000000B
000069H			R/W		XXXX0000B
00006AH to 00006EH	(Reserved area) *				
00006FH	ROMM	ROM mirroring function selection register	W	ROM mirroring function selection module	XXXXXXX1B
000070H to 00007FH	(Reserved area) *				
000080H	BVALR	Message buffer enabling register	R/W	CAN controller	00000000B
000081H	(Reserved area) *				
000082H	TREQR	Send request register	R/W	CAN controller	00000000B

Address	Register Abbreviation	Register	Read/ Write	Resource	Initial Value
003910H	PRLL0	PPG0 reload register L	R/W	8/16-bit PPG timer	XXXXXXXXB
003911H	PRLH0	PPG0 reload register H	R/W		XXXXXXXXB
003912H	PRLL1	PPG1 reload register L	R/W		XXXXXXXXB
003913H	PRLH1	PPG1 reload register H	R/W		XXXXXXXXB
003914H	PRLL2	PPG2 reload register L	R/W		XXXXXXXXB
003915H	PRLH2	PPG2 reload register H	R/W		XXXXXXXXB
003916H	PRLL3	PPG3 reload register L	R/W		XXXXXXXXB
003917H	PRLH3	PPG3 reload register H	R/W		XXXXXXXXB
003918H to 00392FH	(Reserved area) *				
003930H to 003BFFH	(Reserved area) *				
003C00H to 003C0FH	RAM (General-purpose RAM)				
003C10H to 003C13H	IDR0	ID register 0	R/W	CAN controller	XXXXXXXXB to XXXXXXXXB
003C14H to 003C17H	IDR1	ID register 1	R/W		XXXXXXXXB to XXXXXXXXB
003C18H to 003C1BH	IDR2	ID register 2	R/W		XXXXXXXXB to XXXXXXXXB
003C1CH to 003C1FH	IDR3	ID register 3	R/W		XXXXXXXXB to XXXXXXXXB
003C20H to 003C23H	IDR4	ID register 4	R/W		XXXXXXXXB to XXXXXXXXB
003C24H to 003C27H	IDR5	ID register 5	R/W		XXXXXXXXB to XXXXXXXXB
003C28H to 003C2BH	IDR6	ID register 6	R/W		XXXXXXXXB to XXXXXXXXB
003C2CH to 003C2FH	IDR7	ID register 7	R/W		XXXXXXXXB to XXXXXXXXB
003C30H, 003C31H	DLCR0	DLC register 0	R/W		XXXXXXXXB, XXXXXXXXB
003C32H, 003C33H	DLCR1	DLC register 1	R/W		XXXXXXXXB, XXXXXXXXB
003C34H, 003C35H	DLCR2	DLC register 2	R/W		XXXXXXXXB, XXXXXXXXB
003C36H, 003C37H	DLCR3	DLC register 3	R/W		XXXXXXXXB, XXXXXXXXB

Interrupt Source	EI²OS Readiness	Interrupt Vector			Interrupt Control Register		Priority*3
		Number		Address	ICR	Address	
UART1 reception completed	◎	#37	25H	FFFF68H	ICR13	0000BDH*1	High
UART1 transmission completed	Δ	#38	26H	FFFF64H			↑
Reserved	×	#39	27H	FFFF60H	ICR14	0000BEH*1	
Reserved	×	#40	28H	FFFF5CH			
Flash memory	×	#41	29H	FFFF58H	ICR15	0000BFH*1	↓
Delay interrupt generation module	×	#42	2AH	FFFF54H			Low

○ : Available

× : Unavailable

◎ : Available EI²OS function is provided.

Δ: Available when a cause of interrupt sharing a same ICR is not used.

*1:

- ❒ Peripheral functions sharing an ICR register have the same interrupt level.
- ❒ If peripheral functions share an ICR register, only one function is available when using expanded intelligent I/O service.
- ❒ If peripheral functions share an ICR register, a function using expanded intelligent I/O service does not allow interrupt by another function.

*2: Input capture 1 corresponds to EI²OS, however, PPG does not. When using EI²OS by input capture 1, interrupt should be disabled for PPG.

*3:Priority when two or more interrupts of a same level occur simultaneously.

12. Peripheral Resources

12.1 I/O Ports

The I/O ports are used as general-purpose input/output ports (parallel I/O ports). The MB60385 series model is provided with 5 ports (34 inputs). The ports function as input/output pins for peripheral functions also.

I/O Port Functions

An I/O port, using port data resister (PDR), outputs the output data to I/O pin and input a signal input to I/O port. The port direction register (DDR) specifies direction of input/output of I/O pins on a bit-by-bit basis.

The following summarizes functions of the ports and sharing peripheral functions:

■ Port 1: General-purpose input/output port, used also for PPG timer output and input capture inputs.

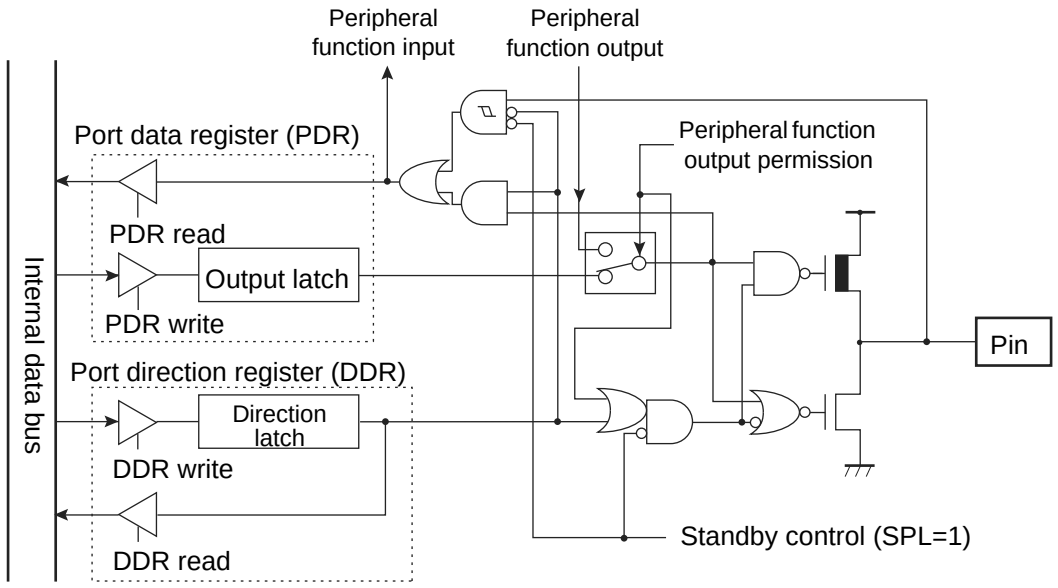
■ Port 2: General-purpose input/output port, used also for reload timer input/output and external interrupt input.

■ Port 3: General-purpose input/output port, used also for A/D converter activation trigger pin.

■ Port 4: General-purpose input/output port, used also for UART input/output and CAN controller send/receive pin.

■ Port 5: General-purpose input/output port, used also analog input pin.

Port 3 Pins Block Diagram (general-purpose input/output port)



Standby control: Control among Stop mode (SPL=1), Time-base timer mode (SPL=1), and watch mode (SPL=1).

Port 3 Registers

■ Port 3 registers include port 3 data register (PDR3) and port 3 direction register (DDR3).

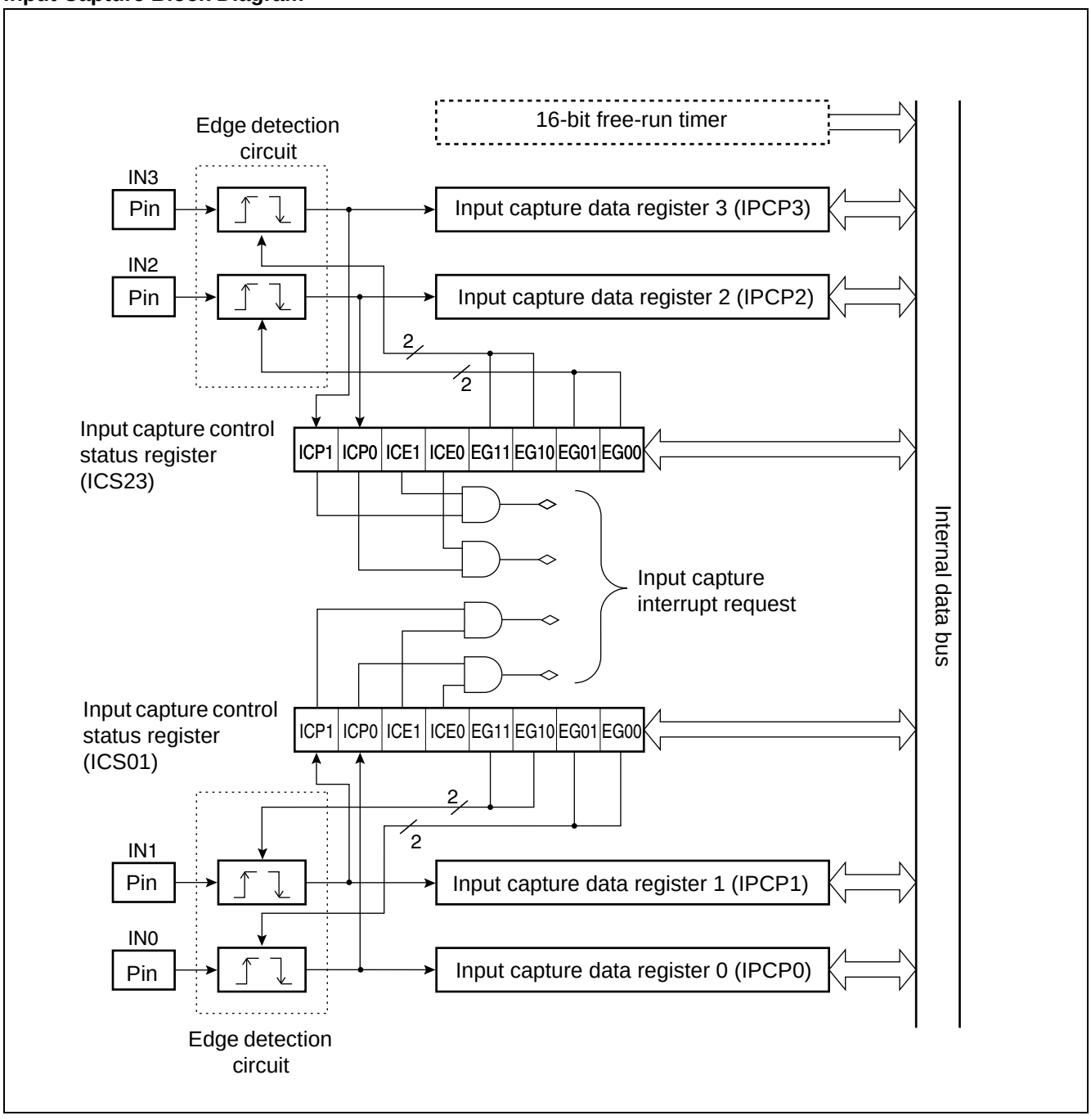
■ The bits configuring the register correspond to port 3 pins on a one-to-one basis.

Relation between Port 3 Registers and Pins

Port Name	Bits of Register and Corresponding Pins								
Port 3	PDR3, DDR3	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	Corresponding pins	P37	P36*	P35*	–	P33	P32	P31	P30

*: P35 and P36 do not exist on MB90387and MB90F387.

Input Capture Block Diagram



12.6 Watch Timer Outline

The watch timer is a 15-bit free-run counter that increments in synchronization with sub clock.

- Interval time is selectable among 7 choices, and generation of interrupt request is allowed for each interval.
- Provides operation clock to the subclock oscillation stabilizing wait timer and watchdog timer.
- Always uses subclock as a count clock regardless of settings of clock selection register (CKSCR).

Interval Timer Function

- In the watch timer, a bit corresponding to the interval time overflows (carry-over) when an interval time, which is specified by interval time selection bit, is reached. Then overflow flag bit is set (WTC: WTOF=1).
- If an interrupt by overflow is permitted (WTC: WTIE=1), an interrupt request is generated upon setting an overflow flag bit.
- Interval time of watch timer is selectable among the following seven choices:

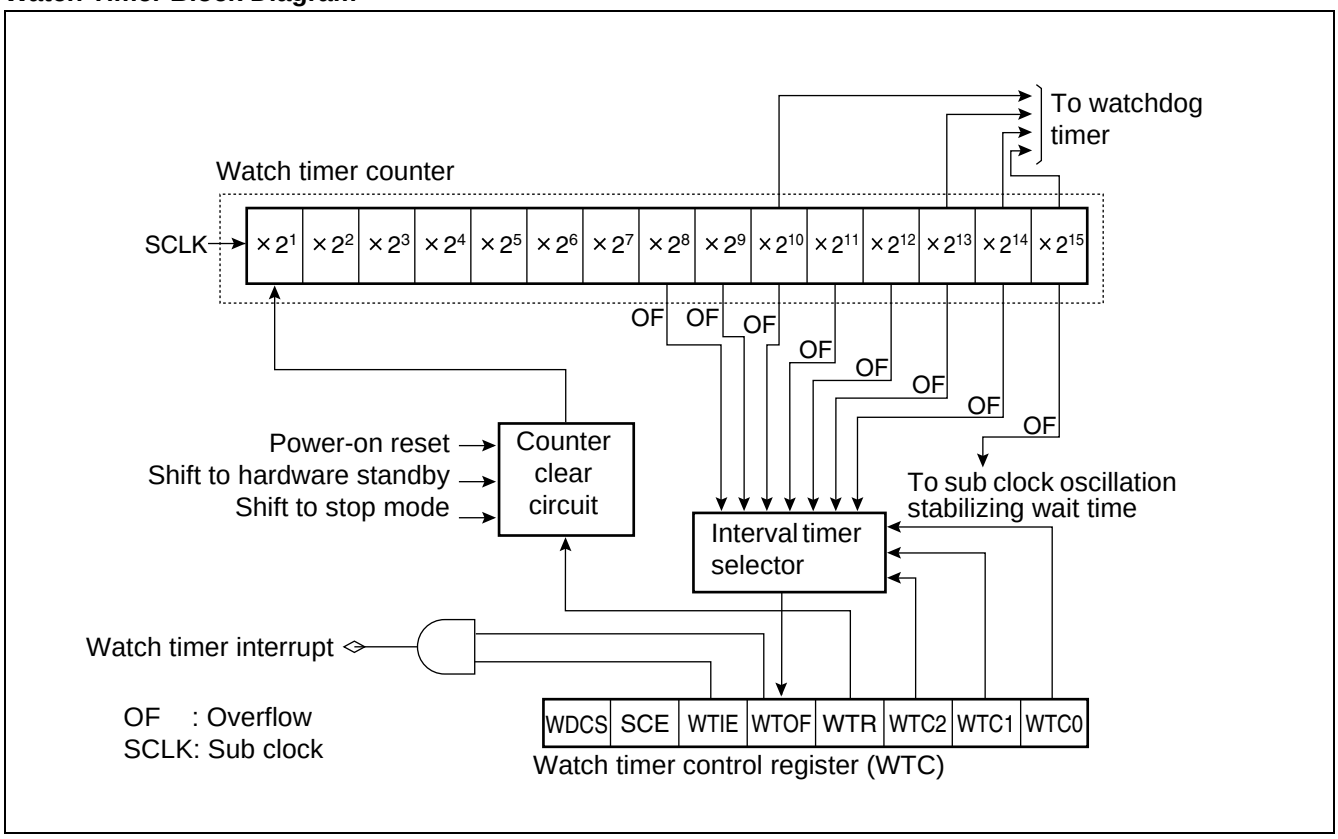
Interval Time of Watch Timer

Sub Clock Cycle	Interval Time
1/SCLK (122 μs)	2^8/SCLK (31.25 ms)
	2^9/SCLK (62.5 ms)
	2^{10}/SCLK (125 ms)
	2^{11}/SCLK (250 ms)
	2^{12}/SCLK (500 ms)
	2^{13}/SCLK (1.0 s)
	2^{14}/SCLK (2.0 s)

SCLK: Sub clock frequency

Values in parentheses “( )” are calculation when operating with 8.192 kHz clock.

Watch Timer Block Diagram



Actual interrupt request number of watch timer is as follows:
Interrupt request number: #28 ($1C_H$)

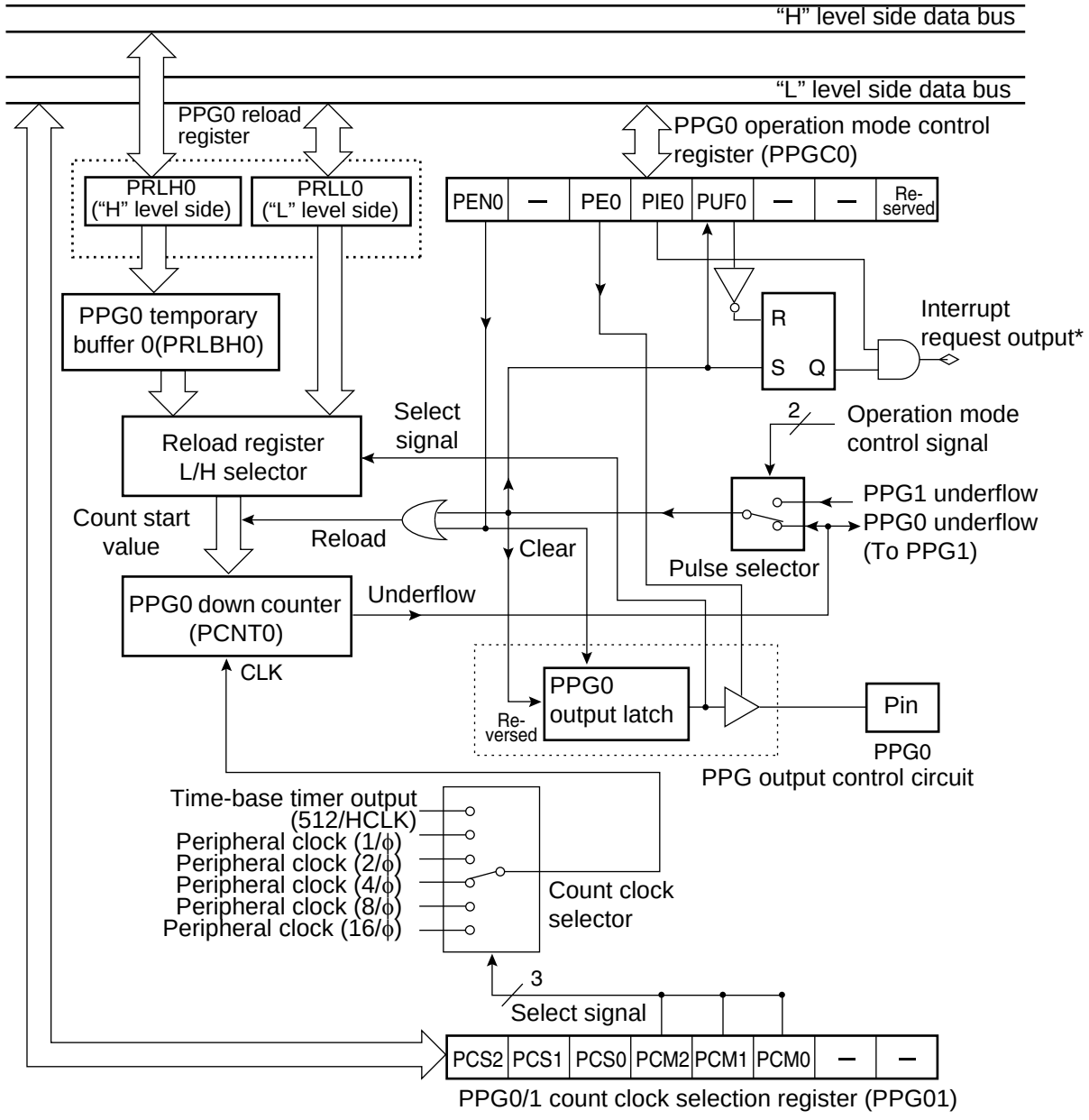
Watch Timer Counter

A 15-bit up counter that uses sub clock (SCLK) as a count clock.

Counter Clear Circuit

A circuit that clears the watch timer counter.

8/16-bit PPG Timer 0 Block Diagram



– : Undefined
Reserved: Reserved bit
HCLK : Oscillation clock frequency
ϕ : Machine clock frequency
* : Interrupt output of 8/16-bit PPG timer 0 is incorporated into one by the OR circuit against interrupt output of 8/16-bit PPG timer 1.

12.9 DTP/External Interrupt and CAN Wakeup Outline

DTP/external interrupt transfers an interrupt request generated by an external peripheral device or a data transmission request to CPU, generating external interrupt request and activating expanded intelligent I/O service. Input RX of CAN controller is used as external interrupt input.

DTP/External Interrupt and CAN Wakeup Function

An interrupt request input from external peripheral device to external input pins (INT7 to INT4) and RX pin, just as interrupt request of peripheral device, generates an interrupt request. The interrupt request generates an external interrupt and activates expanded intelligent I/O service (EI^2OS).

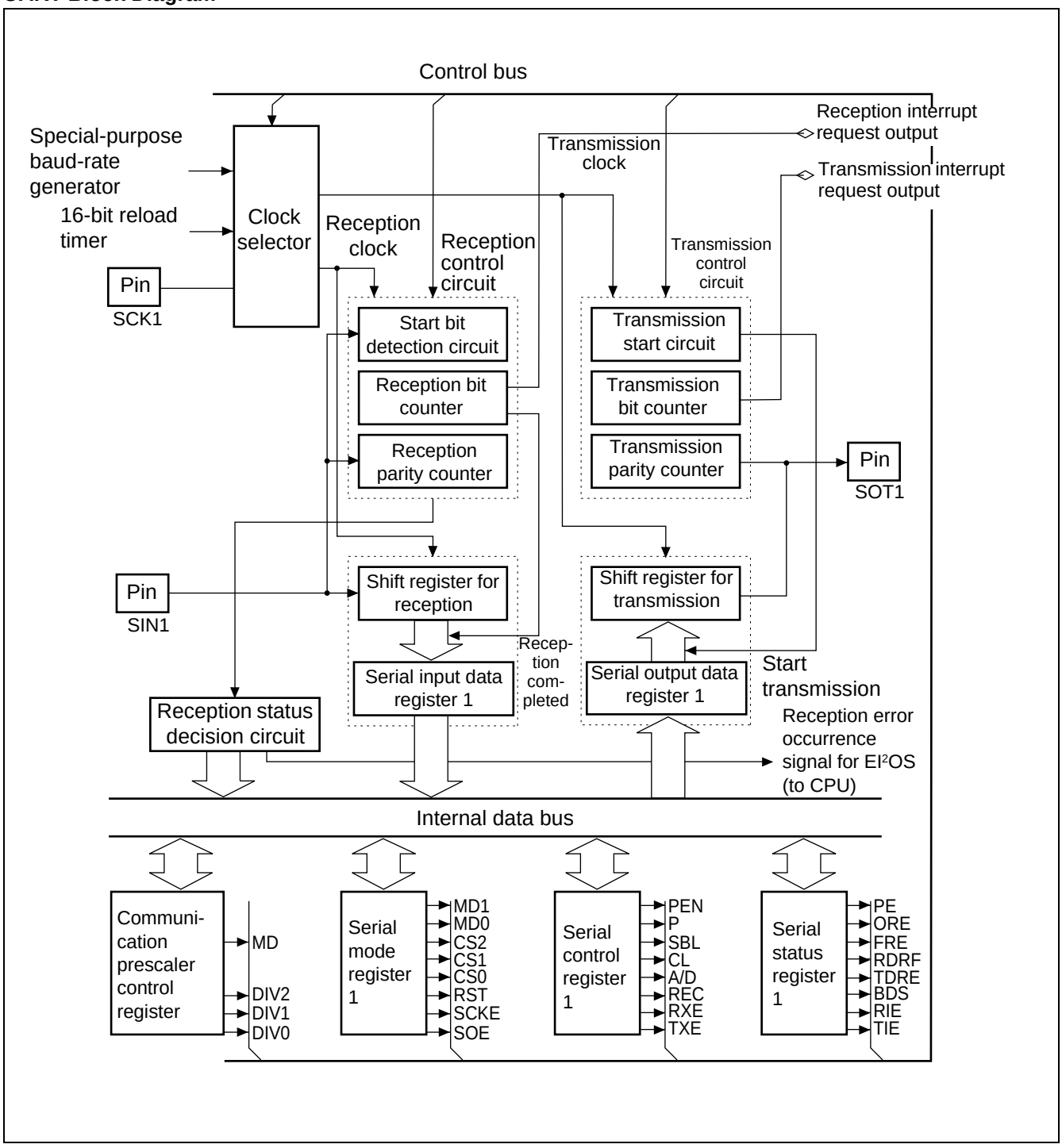
If the expanded intelligent I/O service (EI^2OS) has been disabled by interrupt control register (ICR: ISE=0), external interrupt function is enabled and branches to interrupt processing.

If the EI^2OS has been enabled, (ICR: ISE=1), DTP function is enabled and automatic data transmission is performed by EI^2OS. After performing specified number of data transmission processes, the process branches to interrupt processing.

Table 12-2. DTP/External Interrupt and CAN Wakeup Outline

	External Interrupt	DTP Function
Input pin	5 pins (RX, and INT4 to INT7)	
Interrupt cause	Specify for each pin with detection level setting register (ELVR).	
	Input of “H” level/“L” level/rising edge/falling edge.	Input of “H” level/ “L” level
Interrupt number	#15 ($0F_H$), #24 (18_H), #27 ($1B_H$)	
Interrupt control	Enabling or disabling output of interrupt request, using DTP/external interrupt permission register (ENIR).	
Interrupt flag	Retaining interrupt cause with DTP/external interrupt cause register (EIRR).	
Process selection	Disable EI^2OS (ICR: ISE=0)	Enable EI^2OS (ICR: ISE=1)
Process	Branch to external interrupt process	After automatic data transmission by EI^2OS for specified number of times, branch to interrupt process.

UART Block Diagram



12.12 CAN Controller

The Controller Area Network (CAN) is a serial communication protocol compliant with CANVer2.0A and Ver2.0B. The protocol allows data transmission and reception in both standard frame format and expanded frame format.

Features of CAN Controller

- CAN controller format is compliant with CANVer2.0A and Ver2.0B.
- The protocol allows data transmission and reception in standard frame format and expanded frame format.
- Automatic transmission of data frame by remote frame reception is allowed.
- Baud rate ranges from 10 kbps to 1 Mbps (with 16-MHz machine clock).

Table 12-5. Data Transmission Baud Rate

Machine Clock	Baud Rate (Max)
16 MHz	1 Mbps
12 MHz	1 Mbps
8 MHz	1 Mbps
4 MHz	500 kbps
2 MHz	250 kbps

- Provided with 8 transmission/reception message buffers.
- Transmission/reception is allowed at ID 11 bit in standard format, and at ID 29 bit in expanded frame format.
- Specifying 0 byte to 8 bytes is allowed in message data.
- Multi-level message buffer configuration is allowed.
- CAN controller has two built-in acceptance masks. Mask settings are independently allowed for the two acceptance masks on reception IDs.
- The two acceptance masks allow reception in standard frame format and expanded frame format.
- For types of masking, all-bit comparison, all-bit masking, and partial masking with acceptance mask register 0/1, are specifiable.

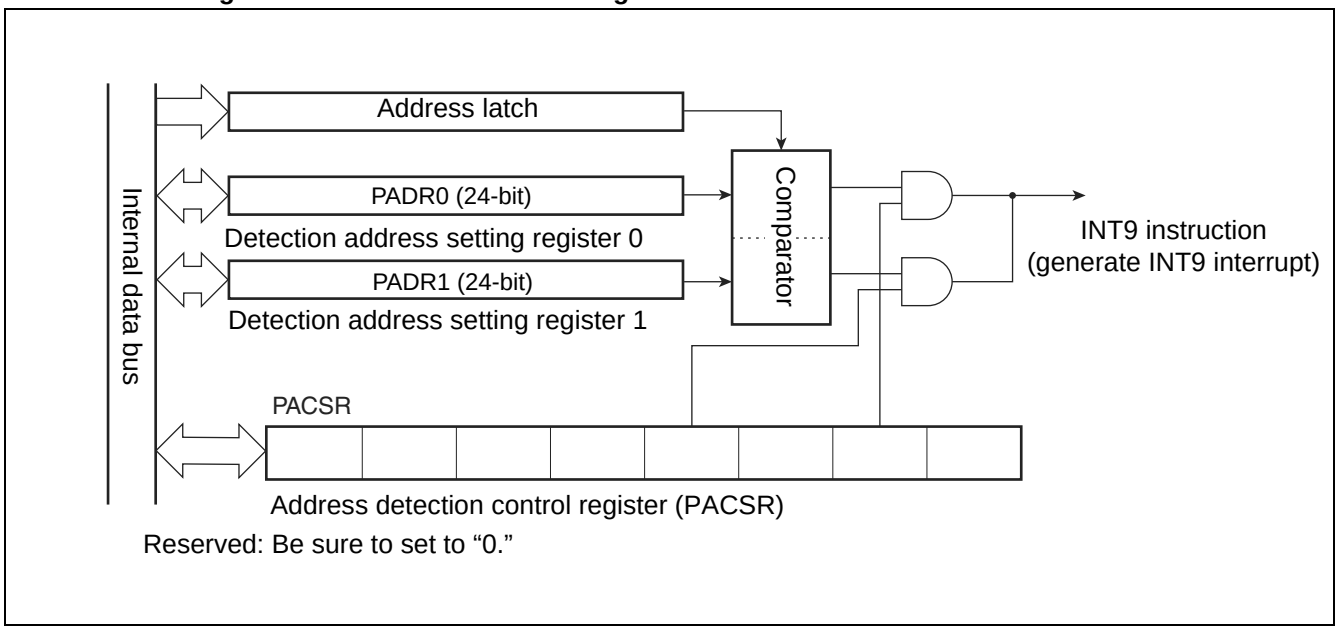
12.13 Address Matching Detection Function Outline

The address matching detection function checks if an address of an instruction to be processed next to a currently-processed instruction is identical with an address specified in the detection address register. If the addresses match with each other, an instruction to be processed next in program is forcibly replaced with INT9 instruction, and process branches to the interrupt process program. Using INT9 interrupt, this function is available for correcting program by batch processing.

Address Matching Detection Function Outline

- An address of an instruction to be processed next to a currently-processed instruction of the program is always retained in an address latch via internal data bus. By the address matching detection function, the address value retained in the address latch is always compared with an address specified in detection address setting register. If the compared address values match with each other, an instruction to be processed next by CPU is forcibly replaced with INT9 instruction, and an interrupt process program is executed.
- Two detection address setting registers are provided (PADR0 and PADR1), and each register is provided with interrupt permission bit. Generation of interrupt, which is caused by address matching between the address retained in address latch and the address specified in address setting register, is permitted and prohibited on a register-by-register basis.

Address Matching Detection Function Block Diagram



- Address latch

  Retains address value output to internal data bus.

- Address detection control register (PACSR)

  Specifies if interrupt is permitted or prohibited when addresses match with each other.

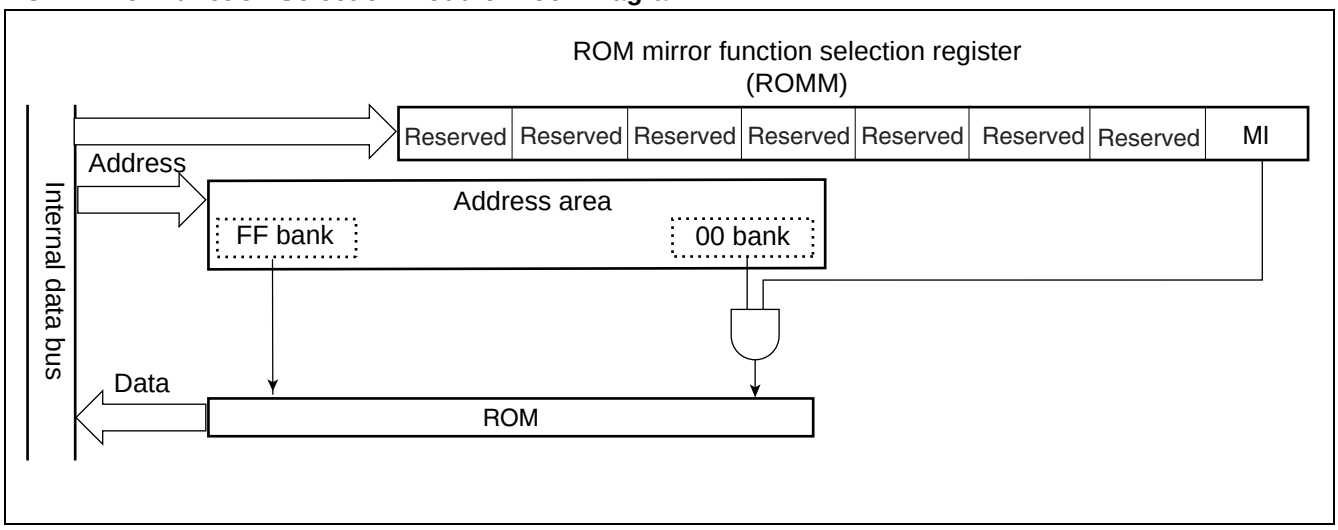
- Detection address setting (PADR0, PADR1)

  Specifies addresses to be compared with values in address latch.

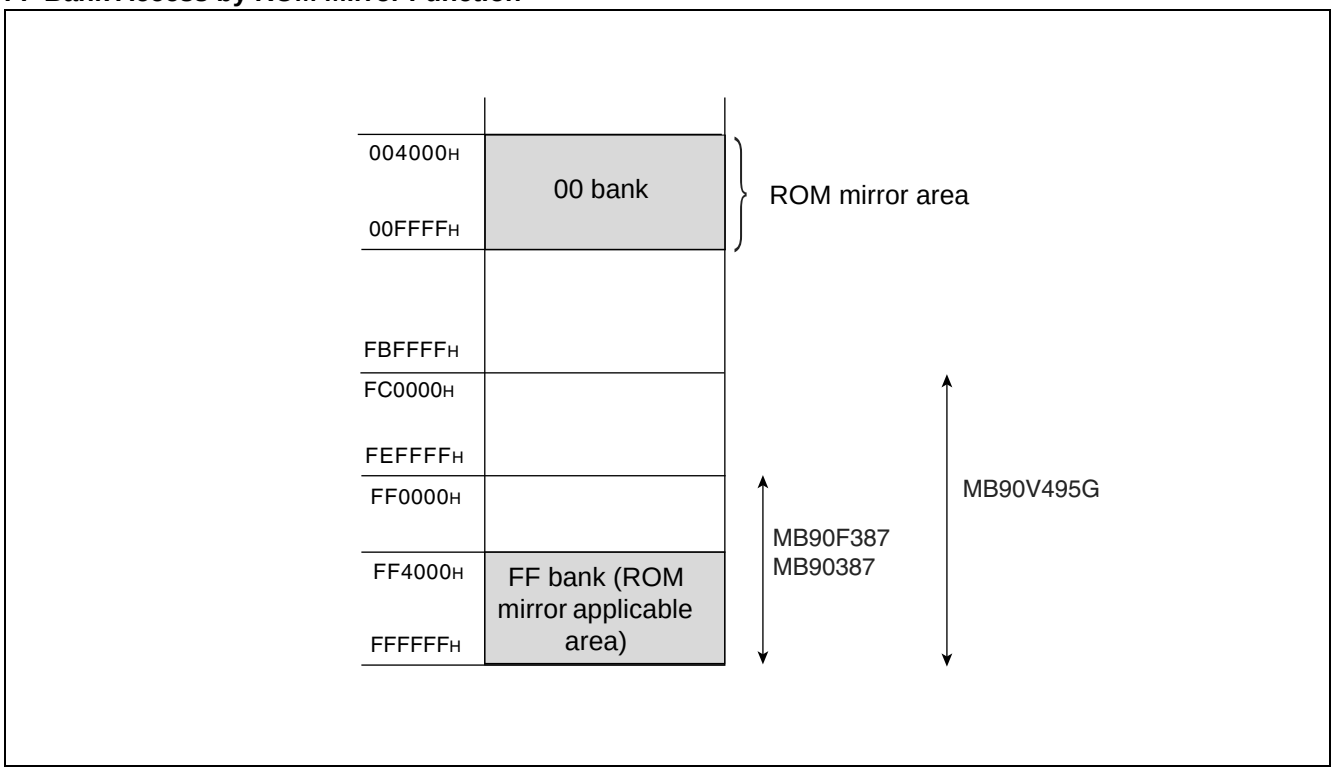
12.14 ROM Mirror Function Selection Module Outline

The ROM mirror function selection module sets the data in ROM assigned to FF bank so that the data is read by access to 00 bank.

ROM Mirror Function Selection Module Block Diagram



FF Bank Access by ROM Mirror Function



13. Electrical Characteristics

13.1 Absolute Maximum Rating

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	
	AV_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	$V_{CC} = AV_{CC}$*2
	AVR	V_{SS} – 0.3	V_{SS} + 6.0	V	$AV_{CC} \geq AVR$*2
Input voltage*1	V_I	V_{SS} – 0.3	V_{SS} + 6.0	V	*3
Output voltage*1	V_O	V_{SS} – 0.3	V_{SS} + 6.0	V	*3
Maximum clamp current	I_{CLAMP}	– 2.0	+ 2.0	mA	*7
Total maximum clamp current	$\Sigma \mid I_{CLAMP} \mid$	–	20	mA	*7
“L” level maximum output current	I_{OL1}	–	15	mA	Normal output*4
	I_{OL2}	–	40	mA	High-current output*4
“L” level average output current	I_{OLAV1}	–	4	mA	Normal output*5
	I_{OLAV2}	–	30	mA	High-current output*5
“L” level maximum total output current	ΣI_{OL1}	–	125	mA	Normal output
	ΣI_{OL2}	–	160	mA	High-current output
“L” level average total output current	ΣI_{OLAV1}	–	40	mA	Normal output*6
	ΣI_{OLAV2}	–	40	mA	High-current output*6
“H” level maximum output current	I_{OH1}	–	–15	mA	Normal output*4
	I_{OH2}	–	–40	mA	High-current output*4
“H” level average output current	I_{OHAV1}	–	–4	mA	Normal output*5
	I_{OHAV2}	–	–30	mA	High-current output*5
“H” level maximum total output current	ΣI_{OH1}	–	–125	mA	Normal output
	ΣI_{OH2}	–	–160	mA	High-current output
“H” level average total output current	ΣI_{OHAV1}	–	–40	mA	Normal output*6
	ΣI_{OHAV2}	–	–40	mA	High-current output*6
Power consumption	P_D	–	245	mW	
Operating temperature	T_A	–40	+105	°C	
Storage temperature	Tstg	–55	+150	°C	

*1: The parameter is based on $V_{SS} = AV_{SS} = 0.0$ V.

*2: AVcc and AVR should not exceed Vcc.

*3: V_I and V_O should not exceed Vcc + 0.3 V. However if the maximum current to/from an input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating.

*4: A peak value of an applicable one pin is specified as a maximum output current.

*5: An average current value of an applicable one pin within 100 ms is specified as an average output current. (Average value is found by multiplying operating current by operating rate.)

*6: An average current value of all pins within 100 ms is specified as an average total output current. (Average value is found by multiplying operating current by operating rate.)

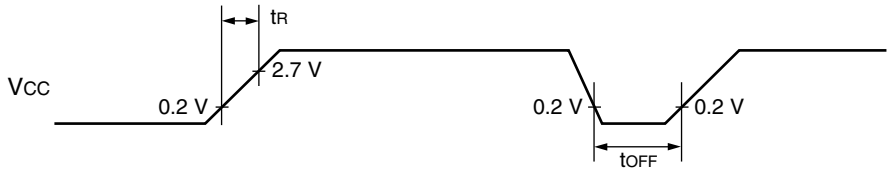
*7:

■ Applicable to pins: P10 to P17, P20 to P27, P30 to P33, P35*, P36*, P37, P40 to P44, P50 to P57
*: P35 and P36 are MB90387S and MB90F387S only.

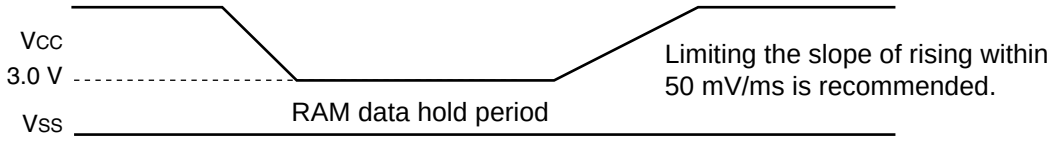
13.4.3 Power-on Reset

(V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Power supply rise time	t_R	V_{CC}	–	0.05	30	ms	
Power supply shutdown time	t_{OFF}	V_{CC}		1	–	ms	Waiting time until power-on



Sudden change of power supply voltage may activate the power-on reset function. When changing power supply voltages during operation, raise the power smoothly by suppressing variation of voltages as shown below. When raising the power, do not use PLL clock. However, if voltage drop is 1V/s or less, use of PLL clock is allowed during operation.



13.5 A/D Converter

(V_{CC} = AV_{CC} = 4.0 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, 3.0 V ≤ AVR − AV_{SS}, T_A = −40 °C to +105 °C)

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	–	–	–	–	10	bit	
Total error	–	–	–	–	± 3.0	LSB	
Nonlinear error	–	–	–	–	± 2.5	LSB	
Differential linear error	–	–	–	–	± 1.9	LSB	
Zero transition voltage	V_{OT}	AN0 to AN7	AV_{SS} − 1.5 LSB	AV_{SS} + 0.5 LSB	AV_{SS} + 2.5 LSB	V	1 LSB = (AVR − AV_{SS}) / 1024
Full-scale transition voltage	V_{FST}	AN0 to AN7	AVR − 3.5 LSB	AVR − 1.5 LSB	AVR + 0.5 LSB	V	
Compare time	–	–	66 t_{CP} *1	–	–	ns	With 16 MHz machine clock 5.5 V ≥ AV_{CC} ≥ 4.5 V
			88 t_{CP} *1	–	–	ns	With 16 MHz machine clock 4.5 V > AV_{CC} ≥ 4.0 V
Sampling time	–	–	32 t_{CP} *1	–	–	ns	With 16 MHz machine clock 5.5 V ≥ AV_{CC} ≥ 4.5 V
			128 t_{CP} *1	–	–	ns	With 16 MHz machine clock 4.5 V > AV_{CC} ≥ 4.0 V
Analog port input current	I_{AIN}	AN0 to AN7	–	–	10	µA	
Analog input voltage	V_{AIN}	AN0 to AN7	AV_{SS}	–	AVR	V	
Reference voltage	–	AVR	AV_{SS} + 2.7	–	AV_{CC}	V	
Power supply current	I_A	AV_{CC}	–	3.5	7.5	mA	
	I_{AH}	AV_{CC}	–	–	5	µA	*2
Reference voltage supplying current	I_R	AVR	–	165	250	µA	
	I_{RH}	AVR	–	–	5	µA	*2
Variation among channels	–	AN0 to AN7	–	–	4	LSB	

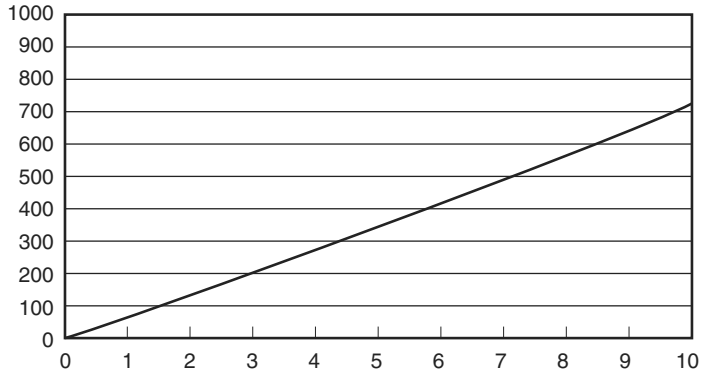
*1: Refer to Clock Timing on AC Characteristics.

*2: If A/D converter is not operating, a current when CPU is stopped is applicable (Vcc=AVcc=AVR=5.0 V).

(Continued)

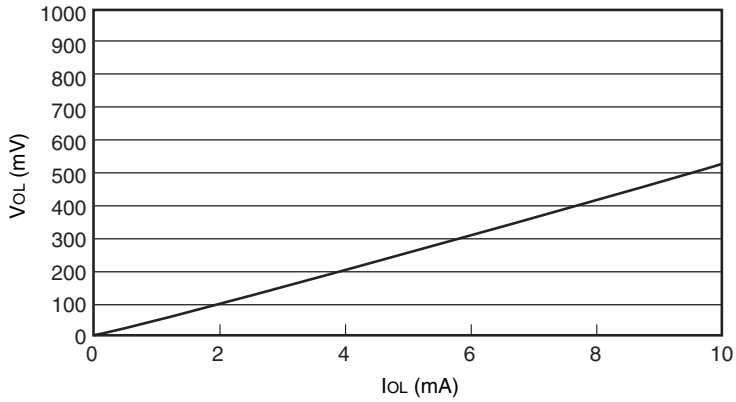
(V_{CC} - V_{OH}) – I_{OH}

T_A = +25 °C, V_{CC} = 4.5 V



V_{OL} – I_{OL}

T_A = +25 °C, V_{CC} = 4.5 V



H level input voltage/ L level input voltage
V_{IN} – V_{CC}

T_A = +25 °C