



Welcome to [E-XFL.COM](https://www.e-xfl.com)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	F ² MC-16LX
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, SCI, UART/USART
Peripherals	POR, WDT
Number of I/O	36
Program Memory Size	64KB (64K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90387sfmt-gs-245

10. I/O Map

Address	Register Abbreviation	Register	Read/Write	Resource	Initial Value
000000 _H	(Reserved area) *				
000001 _H	PDR1	Port 1 data register	R/W	Port 1	XXXXXXXX _B
000002 _H	PDR2	Port 2 data register	R/W	Port 2	XXXXXXXX _B
000003 _H	PDR3	Port 3 data register	R/W	Port 3	XXXXXXXX _B
000004 _H	PDR4	Port 4 data register	R/W	Port 4	XXXXXXXX _B
000005 _H	PDR5	Port 5 data register	R/W	Port 5	XXXXXXXX _B
000006 _H to 000010 _H	(Reserved area) *				
000011 _H	DDR1	Port 1 direction data register	R/W	Port 1	00000000 _B
000012 _H	DDR2	Port 2 direction data register	R/W	Port 2	00000000 _B
000013 _H	DDR3	Port 3 direction data register	R/W	Port 3	000X0000 _B
000014 _H	DDR4	Port 4 direction data register	R/W	Port 4	XXX00000 _B
000015 _H	DDR5	Port 5 direction data register	R/W	Port 5	00000000 _B
000016 _H to 00001A _H	(Reserved area) *				
00001B _H	ADER	Analog input permission register	R/W	8/10-bit A/D converter	11111111 _B
00001C _H to 000025 _H	(Reserved area) *				
000026 _H	SMR1	Serial mode register 1	R/W	UART1	00000000 _B
000027 _H	SCR1	Serial control register 1	R/W, W		00000100 _B
000028 _H	SIDR1/ SODR1	Serial input data register 1/ Serial output data register 1	R, W		XXXXXXXX _B
000029 _H	SSR1	Serial status data register 1	R, R/W		00001000 _B
00002A _H	(Reserved area) *				
00002B _H	CDCR1	Communication prescaler control register 1	R/W	UART1	0XXX0000 _B
00002C _H to 00002F _H	(Reserved area) *				
000030 _H	ENIR	DTP/External interrupt permission register	R/W	DTP/External interrupt	00000000 _B
000031 _H	EIRR	DTP/External interrupt permission register	R/W		XXXXXXXX _B
000032 _H	ELVR	Detection level setting register	R/W		00000000 _B
000033 _H			R/W		00000000 _B
000034 _H	ADCS	A/D control status register	R/W	8/10-bit A/D converter	00000000 _B
000035 _H			R/W, W		00000000 _B
000036 _H	ADCR	A/D data register	W, R		XXXXXXXX _B
000037 _H			R		00101XXX _B

Address	Register Abbreviation	Register	Read/Write	Resource	Initial Value
003C38 _H , 003C39 _H	DLCR4	DLC register 4	R/W	CAN controller	XXXXXXXX _B , XXXXXXXX _B
003C3A _H , 003C3B _H	DLCR5	DLC register 5	R/W		XXXXXXXX _B , XXXXXXXX _B
003C3C _H , 003C3D _H	DLCR6	DLC register 6	R/W		XXXXXXXX _B , XXXXXXXX _B
003C3E _H , 003C3F _H	DLCR7	DLC register 7	R/W		XXXXXXXX _B , XXXXXXXX _B
003C40 _H to 003C47 _H	DTR0	Data register 0	R/W		XXXXXXXX _B to XXXXXXXX _B
003C48 _H to 003C4F _H	DTR1	Data register 1	R/W		XXXXXXXX _B to XXXXXXXX _B
003C50 _H to 003C57 _H	DTR2	Data register 2	R/W		XXXXXXXX _B to XXXXXXXX _B
003C58 _H to 003C5F _H	DTR3	Data register 3	R/W		XXXXXXXX _B to XXXXXXXX _B
003C60 _H to 003C67 _H	DTR4	Data register 4	R/W		XXXXXXXX _B to XXXXXXXX _B
003C68 _H to 003C6F _H	DTR5	Data register 5	R/W		XXXXXXXX _B to XXXXXXXX _B
003C70 _H to 003C77 _H	DTR6	Data register 6	R/W		XXXXXXXX _B to XXXXXXXX _B
003C78 _H to 003C7F _H	DTR7	Data register 7	R/W		XXXXXXXX _B to XXXXXXXX _B
003C80 _H to 003CFF _H	(Reserved area) *				
003D00 _H , 003D01 _H	CSR	Control status register	R/W, R	CAN controller	0XXXX001 _B , 00XXX000 _B
003D02 _H	LEIR	Last event display register	R/W		000XX000 _B
003D03 _H	(Reserved area) *				
003D04 _H , 003D05 _H	RTEC	Send/receive error counter	R	CAN controller	00000000 _B , 00000000 _B
003D06 _H , 003D07 _H	BTR	Bit timing register	R/W		11111111 _B , X1111111 _B
003D08 _H	IDER	IDE register	R/W		XXXXXXXX _B
003D09 _H	(Reserved area) *				
003D0A _H	TRTRR	Send RTR register	R/W	CAN controller	00000000 _B
003D0B _H	(Reserved area) *				
003D0C _H	RFWTR	Remote frame receive wait register	R/W	CAN controller	XXXXXXXX _B

Address	Register Abbreviation	Register	Read/Write	Resource	Initial Value
003D0D _H	(Reserved area) *				
003D0E _H	TIER	Send completion interrupt permission register	R/W	CAN controller	00000000 _B
003D0F _H	(Reserved area) *				
003D10 _H , 003D11 _H	AMSR	Acceptance mask selection register	R/W	CAN controller	XXXXXXXX _B , XXXXXXXX _B
003D12 _H , 003D13 _H	(Reserved area) *				
003D14 _H to 003D17 _H	AMR0	Acceptance mask register 0	R/W	CAN controller	XXXXXXXX _B to XXXXXXXX _B
003D18 _H to 003D1B _H	AMR1	Acceptance mask register 1	R/W		XXXXXXXX _B to XXXXXXXX _B
003D1C _H to 003DFF _H	(Reserved area) *				
003E00 _H to 003EFF _H	(Reserved area) *				
003FF0 _H to 003FFF _H	(Reserved area) *				

Initial values:

0: Initial value of this bit is "0."

1: Initial value of this bit is "1."

X: Initial value of this bit is undefined.

*: "Reserved area" should not be written anything. Result of reading from "Reserved area" is undefined.

Interrupt Source	EI ² OS Readiness	Interrupt Vector		Interrupt Control Register		Priority* ³
		Number	Address	ICR	Address	
UART1 reception completed	◎	#37	25 _H	FFFF68 _H	ICR13	High ↑
UART1 transmission completed	△	#38	26 _H	FFFF64 _H		
Reserved	×	#39	27 _H	FFFF60 _H	ICR14	
Reserved	×	#40	28 _H	FFFF5C _H		
Flash memory	×	#41	29 _H	FFFF58 _H	ICR15	↓ Low
Delay interrupt generation module	×	#42	2A _H	FFFF54 _H		

○ : Available

× : Unavailable

◎ : Available EI²OS function is provided.

△: Available when a cause of interrupt sharing a same ICR is not used.

- *1:
- Peripheral functions sharing an ICR register have the same interrupt level.
 - If peripheral functions share an ICR register, only one function is available when using expanded intelligent I/O service.
 - If peripheral functions share an ICR register, a function using expanded intelligent I/O service does not allow interrupt by another function.

*2: Input capture 1 corresponds to EI²OS, however, PPG does not. When using EI²OS by input capture 1, interrupt should be disabled for PPG.

*3: Priority when two or more interrupts of a same level occur simultaneously.

12. Peripheral Resources

12.1 I/O Ports

The I/O ports are used as general-purpose input/output ports (parallel I/O ports). The MB60385 series model is provided with 5 ports (34 inputs). The ports function as input/output pins for peripheral functions also.

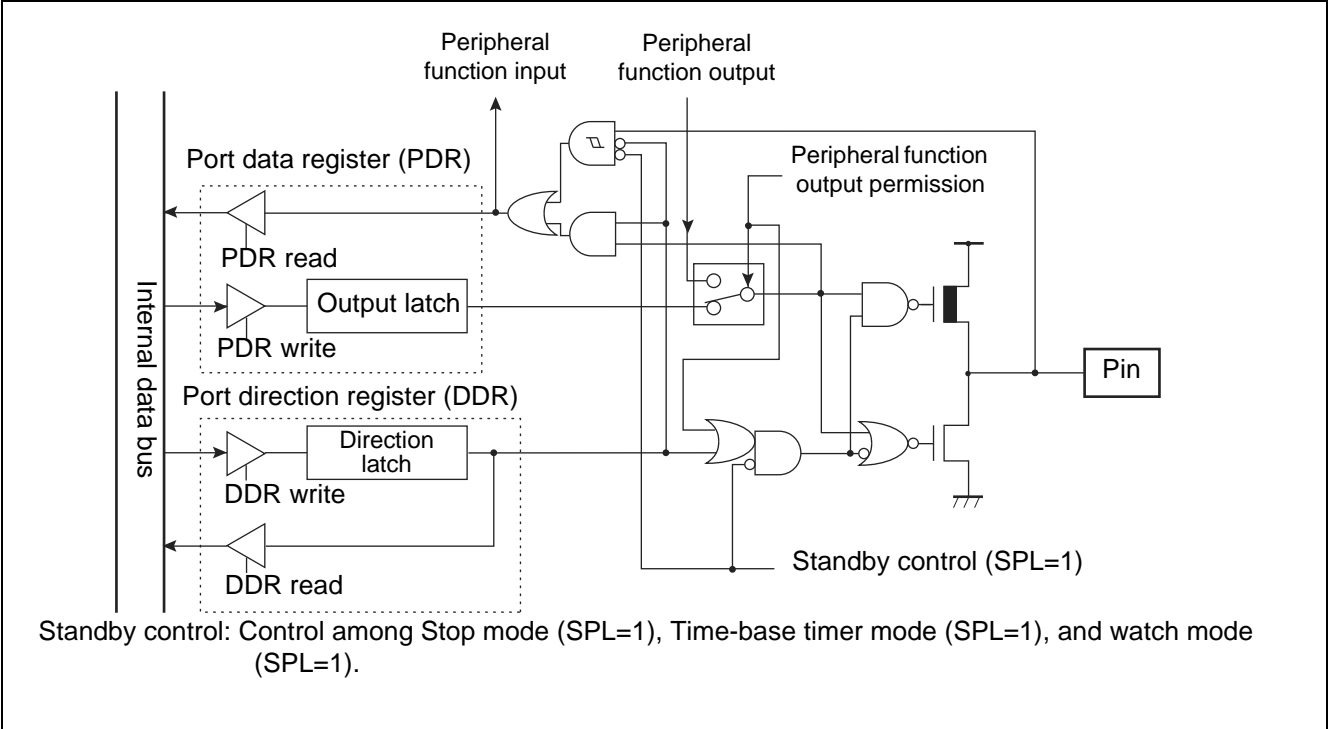
I/O Port Functions

An I/O port, using port data resistor (PDR), outputs the output data to I/O pin and input a signal input to I/O port. The port direction register (DDR) specifies direction of input/output of I/O pins on a bit-by-bit basis.

The following summarizes functions of the ports and sharing peripheral functions:

- Port 1: General-purpose input/output port, used also for PPG timer output and input capture inputs.
- Port 2: General-purpose input/output port, used also for reload timer input/output and external interrupt input.
- Port 3: General-purpose input/output port, used also for A/D converter activation trigger pin.
- Port 4: General-purpose input/output port, used also for UART input/output and CAN controller send/receive pin.
- Port 5: General-purpose input/output port, used also analog input pin.

Port 2 Pins Block Diagram (general-purpose input/output port)



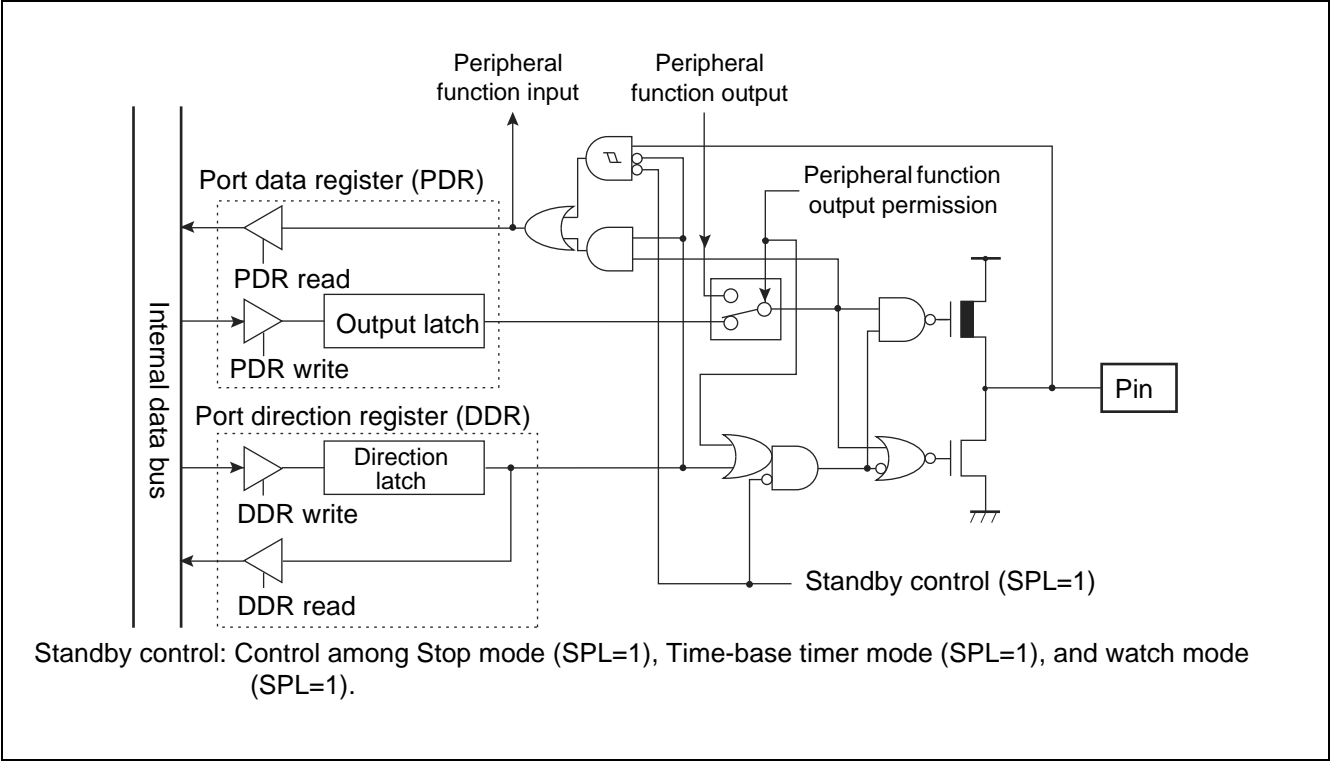
Port 2 Registers

- Port 2 registers include port 2 data register (PDR2) and port 2 direction register (DDR2).
- The bits configuring the register correspond to port 2 pins on a one-to-one basis.

Relation between Port 2 Registers and Pins

Port Name	Bits of Register and Corresponding Pins								
Port 2	PDR2,DDR2	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	Corresponding pins	P27	P26	P25	P24	P23	P22	P21	P20

Port 4 Pins Block Diagram



Port 4 Registers

- Port 4 registers include port 4 data register (PDR4) and port 4 direction register (DDR4).
- The bits configuring the register correspond to port 4 pins on a one-to-one basis.

Relation between Port 4 Registers and Pins

Port Name	Bits of Register and Corresponding Pins								
Port 4	PDR4, DDR4	–	–	–	bit4	bit3	bit2	bit1	bit0
	Corresponding pins	–	–	–	P44	P43	P42	P41	P40

12.5 16-bit Reload Timer

The 16-bit reload timer has the following functions:

- Count clock is selectable among 3 internal clocks and external event clock.
- Activation trigger is selectable between software trigger and external trigger.
- Generation of CPU interrupt is allowed upon occurrence of underflow on 16-bit timer register. Available as an interval timer using the interrupt function.
- When underflow of 16-bit timer register (TMR) occurs, one of two reload modes is selectable between one-shot mode that halts counting operation of TMR, and reload mode that reloads 16-bit reload register value to TMR, continuing TMR counting operation.
- The 16-bit reload timer is ready for expanded intelligent I/O service (EI²OS).
- MB90385 series device has 2 channels of built-in 16-bit reload timer.

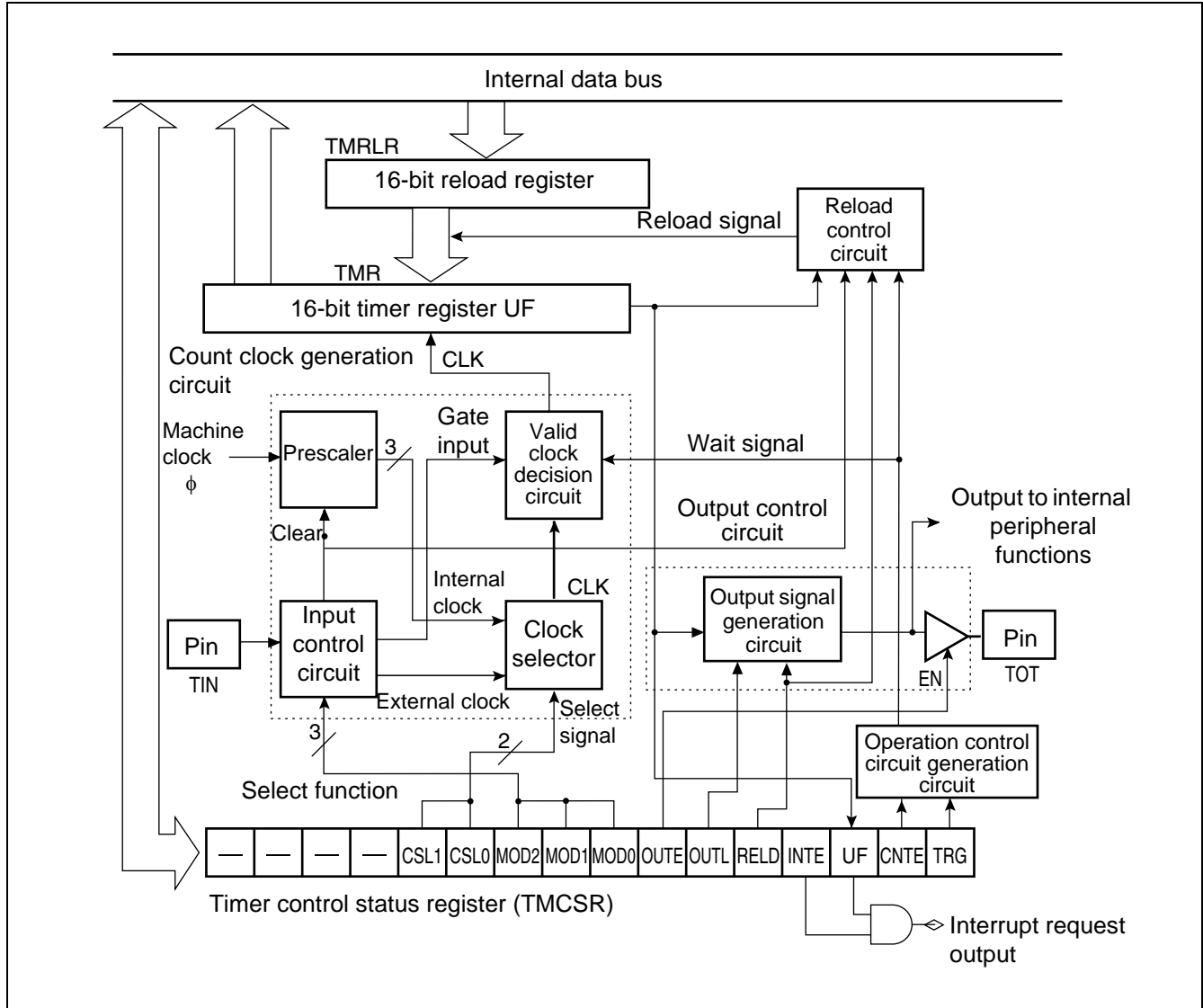
Operation Mode of 16-bit Reload Timer

Count Clock	Activation Trigger	Operation upon Underflow
Internal clock mode	Software trigger, external trigger	One-shot mode, reload mode
Event count mode	Software trigger	One-shot mode, reload mode

Internal Clock Mode

- The 16-bit reload timer is set to internal clock mode, by setting count clock selection bit (TMCSR: CSL1, CSL0) to "00_b", "01_b", "10_b".
- In the internal clock mode, the counter decrements in synchronization with the internal clock.
- Three types of count clock cycles are selectable by count clock selection bit (TMCSR: CSL1, CSL0) in timer control status register.
- Edge detection of software trigger or external trigger is specified as an activation trigger.

16-bit Reload Timer Block Diagram



The diagram illustrates the internal structure and control of the Watch timer. At the top, the **Watch timer counter** is shown as a 16-bit shift register, with bits labeled from $\times 2^1$ to $\times 2^{15}$. The **SCLK** (Sub clock) input is connected to the $\times 2^1$ bit. The counter's output is connected to the **To watchdog timer** block. Below the counter, the **Counter clear circuit** is shown, which is triggered by **Power-on reset**, **Shift to hardware standby**, and **Shift to stop mode**. The **Interval timer selector** block receives overflow (**OF**) signals from bits $\times 2^4$ through $\times 2^{15}$ and provides control signals to the **Watch timer control register (WTC)** and the **To sub clock oscillation stabilizing wait time** block. The **Watch timer interrupt** is generated by an AND gate combining the **WTIE** bit from the WTC and the **WTOF** overflow signal. The **WTC** register itself contains bits **WDCS**, **SCE**, **WTIE**, **WTOF**, **WTR**, **WTC2**, **WTC1**, and **WTC0**.

OF : Overflow
SCLK: Sub clock

Interrupt request number: #28 (1C_H)

A 15-bit up counter that uses sub clock (SCLK) as a count clock.

A circuit that clears the watch timer counter.

12.7 8/16-bit PPG Timer Outline

The 8/16-bit PPG timer is a 2-channel reload timer module (PPG0 and PPG1) that allows outputting pulses of arbitrary cycle and duty cycle. Combination of the two channels allows selection among the following operations:

- 8-bit PPG output 2-channel independent operation mode
- 16-bit PPG output operation mode
- 8-bit and 8-bit PPG output operation mode

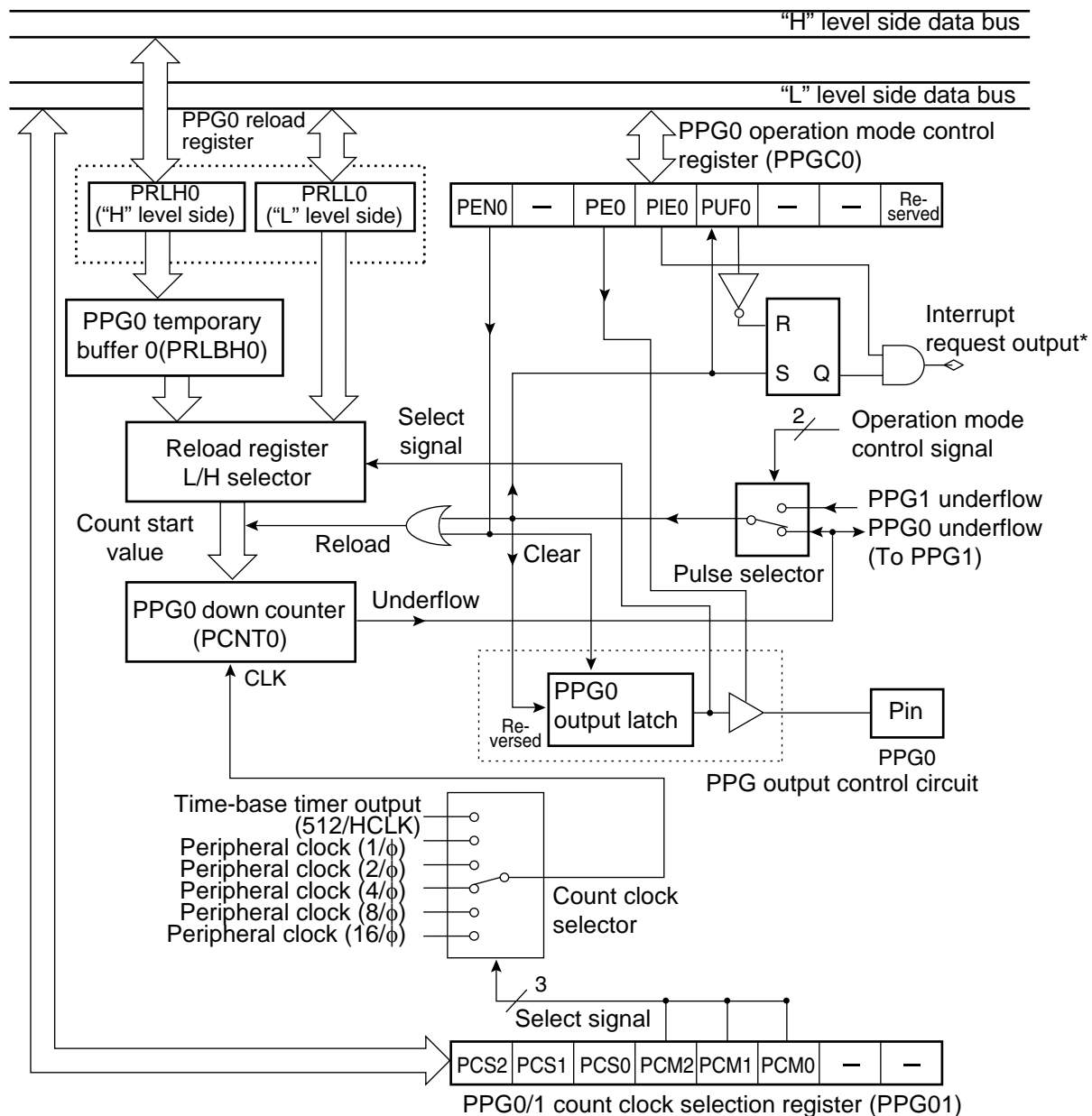
MB90385 series device has two 8/16-bit built-in PPG timers. This section describes functions of PPG0/1. PPG2/3 have the same functions as those of PPG0/1.

Functions of 8/16-bit PPG Timer

The 8/16-bit PPG timer is composed of four 8-bit reload register (PRLH0/PRLL0, PRLH1/PRLL1) and two PPG down counters (PCNT0, PCNT1).

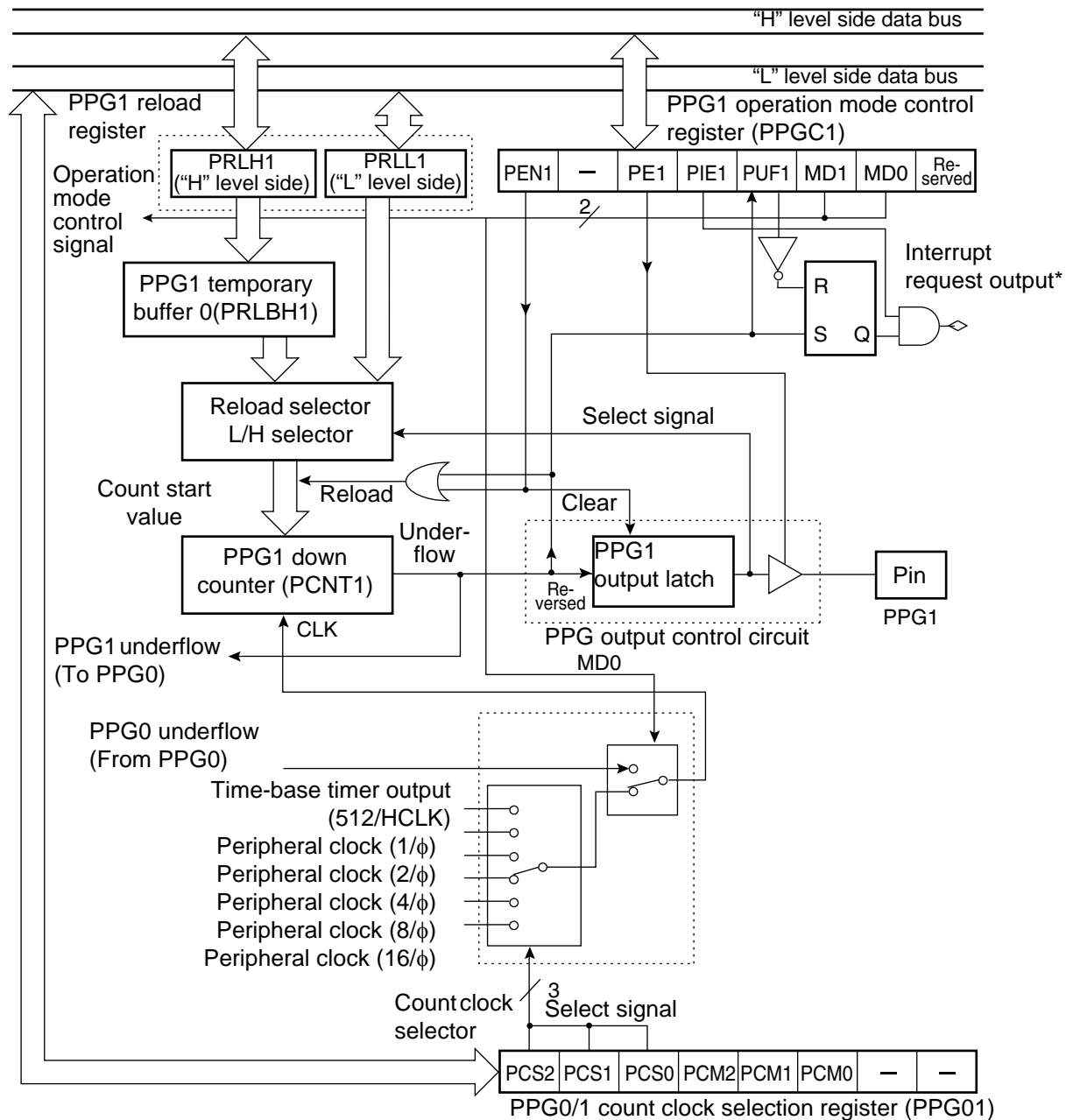
- Widths of “H” and “L” in output pulse are specifiable independently. Cycle and duty factor of output pulse is specifiable arbitrarily.
- Count clock is selectable among 6 internal clocks.
- The timer is usable as an interval timer, by generating interrupt requests for each interval.
- The time is usable as a D/A converter, with an external circuit.

8/16-bit PPG Timer 0 Block Diagram



— : Undefined
Reserved: Reserved bit
HCLK : Oscillation clock frequency
 ϕ : Machine clock frequency
* : Interrupt output of 8/16-bit PPG timer 0 is incorporated into one by the OR circuit against interrupt output of 8/16-bit PPG timer 1.

8/16-bit PPG Timer 1 Block Diagram



— : Undefined
Reserved: Reserved bit
HCLK : Oscillation clock frequency
φ : Machine clock frequency
* : Interrupt output of 8/16-bit PPG timer 1 is incorporated into one by the OR circuit against interrupt output of 8/16-bit PPG timer 0.

12.9 DTP/External Interrupt and CAN Wakeup Outline

DTP/external interrupt transfers an interrupt request generated by an external peripheral device or a data transmission request to CPU, generating external interrupt request and activating expanded intelligent I/O service. Input RX of CAN controller is used as external interrupt input.

DTP/External Interrupt and CAN Wakeup Function

An interrupt request input from external peripheral device to external input pins (INT7 to INT4) and RX pin, just as interrupt request of peripheral device, generates an interrupt request. The interrupt request generates an external interrupt and activates expanded intelligent I/O service (EI²OS).

If the expanded intelligent I/O service (EI²OS) has been disabled by interrupt control register (ICR: ISE=0), external interrupt function is enabled and branches to interrupt processing.

If the EI²OS has been enabled, (ICR: ISE=1), DTP function is enabled and automatic data transmission is performed by EI²OS. After performing specified number of data transmission processes, the process branches to interrupt processing.

Table 12-2. DTP/External Interrupt and CAN Wakeup Outline

	External Interrupt	DTP Function
Input pin	5 pins (RX, and INT4 to INT7)	
Interrupt cause	Specify for each pin with detection level setting register (ELVR).	
	Input of "H" level/"L" level/rising edge/falling edge.	Input of "H" level/ "L" level
Interrupt number	#15 (0FH), #24 (18H), #27 (1BH)	
Interrupt control	Enabling or disabling output of interrupt request, using DTP/external interrupt permission register (ENIR).	
Interrupt flag	Retaining interrupt cause with DTP/external interrupt cause register (EIRR).	
Process selection	Disable EI ² OS (ICR: ISE=0)	Enable EI ² OS (ICR: ISE=1)
Process	Branch to external interrupt process	After automatic data transmission by EI ² OS for specified number of times, branch to interrupt process.

12.11 UART Outline

UART is a general-purpose serial data communication interface for synchronous and asynchronous communication using external devices.

- Provided with bi-directional communication function for both clock-synchronous and clock-asynchronous modes.
- Provided with master/slave communication function (multi-processor mode). (Only master side is available.)
- Interrupt request is generated upon completion of reception, completion of transmission and detection of reception error.
- Ready for expanded intelligent service, EI²OS.

Table 12-3. UART Functions

	Description
Data buffer	Full-duplex double buffer
Transmission mode	Clock synchronous (No start/stop bit, no parity bit) Clock asynchronous (start-stop synchronous)
Baud rate	Built-in special-purpose baud-rate generator. Setting is selectable among 8 values. Input of external values is allowed. Use of clock from external timer (16-bit reload timer 0) is allowed.
Data length	7 bits (only asynchronous normal mode) 8 bits
Signaling system	Non Return to Zero (NRZ) system
Reception error detection	Framing error Overrun error Parity error (not detectable in operation mode 1 (multi-processor mode))
Interrupt request	Receive interrupt (reception completed, reception error detected) Transmission interrupt (transmission completed) Ready for expanded intelligent I/O service (EI ² OS) in both transmission and reception
Master/slave communication function (asynchronous, multi-processor mode)	Communication between 1 (master) and n (slaves) are available (usable as master only).

Note: Start/stop bit is not added upon clock-synchronous transmission. Data only is transmitted.

Table 12-4. UART Operation Modes

Operation Mode		Data Length		Synchronization	Stop Bit Length
		With Parity	Without Parity		
0	Asynchronous mode (normal mode)	7-bit or 8-bit		Asynchronous	1- bit or 2-bit *2
1	Multi processor mode	8+1 *1	—	Asynchronous	
2	Synchronous mode	8	—	Synchronous	No

—: Disallowed

1: “+1” is an address/data selection bit used for communication control (bit 11 of SCR1 register: A/D).

2: Only 1 bit is detected as a stop bit on data reception.

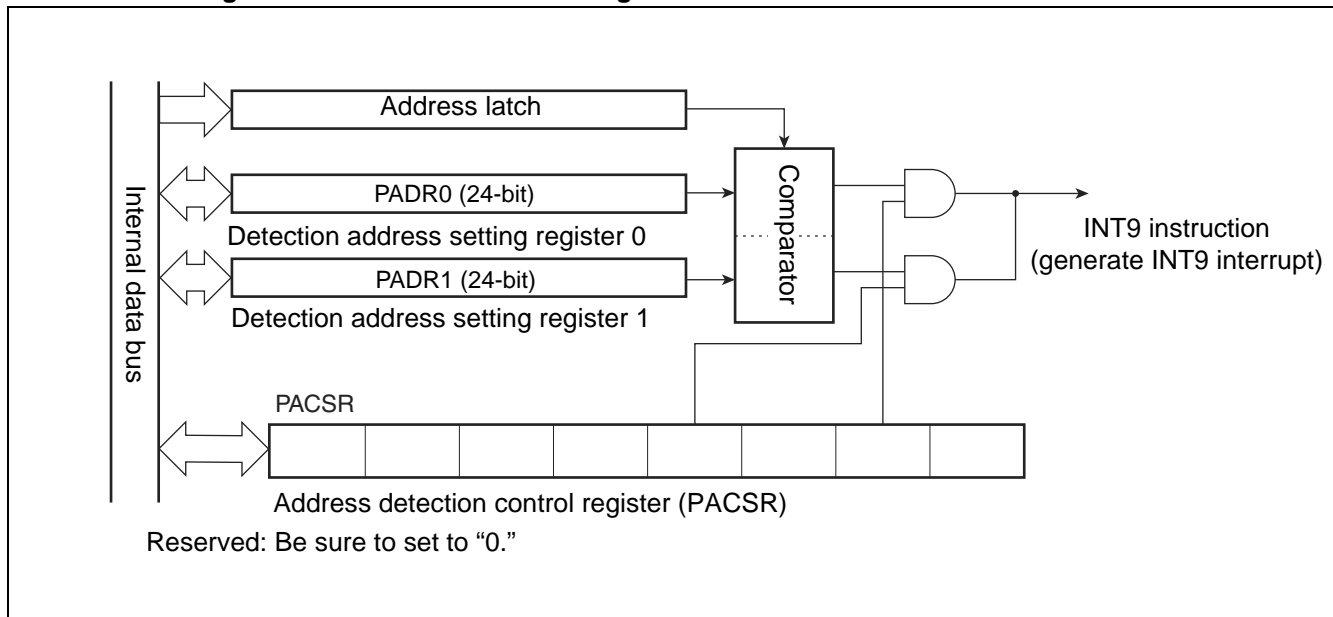
12.13 Address Matching Detection Function Outline

The address matching detection function checks if an address of an instruction to be processed next to a currently-processed instruction is identical with an address specified in the detection address register. If the addresses match with each other, an instruction to be processed next in program is forcibly replaced with INT9 instruction, and process branches to the interrupt process program. Using INT9 interrupt, this function is available for correcting program by batch processing.

Address Matching Detection Function Outline

- An address of an instruction to be processed next to a currently-processed instruction of the program is always retained in an address latch via internal data bus. By the address matching detection function, the address value retained in the address latch is always compared with an address specified in detection address setting register. If the compared address values match with each other, an instruction to be processed next by CPU is forcibly replaced with INT9 instruction, and an interrupt process program is executed.
- Two detection address setting registers are provided (PADR0 and PADR1), and each register is provided with interrupt permission bit. Generation of interrupt, which is caused by address matching between the address retained in address latch and the address specified in address setting register, is permitted and prohibited on a register-by-register basis.

Address Matching Detection Function Block Diagram



- Address latch
Retains address value output to internal data bus.
- Address detection control register (PACSR)
Specifies if interrupt is permitted or prohibited when addresses match with each other.
- Detection address setting (PADR0, PADR1)
Specifies addresses to be compared with values in address latch.

13. Electrical Characteristics

13.1 Absolute Maximum Rating

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V _{CC}	V _{SS} – 0.3	V _{SS} + 6.0	V	
	AV _{CC}	V _{SS} – 0.3	V _{SS} + 6.0	V	V _{CC} = AV _{CC} *2
	AVR	V _{SS} – 0.3	V _{SS} + 6.0	V	AV _{CC} ≥ AVR*2
Input voltage*1	V _I	V _{SS} – 0.3	V _{SS} + 6.0	V	*3
Output voltage*1	V _O	V _{SS} – 0.3	V _{SS} + 6.0	V	*3
Maximum clamp current	I _{CLAMP}	– 2.0	+ 2.0	mA	*7
Total maximum clamp current	Σ I _{CLAMP}	–	20	mA	*7
“L” level maximum output current	I _{OL1}	–	15	mA	Normal output*4
	I _{OL2}	–	40	mA	High-current output*4
“L” level average output current	I _{OLAV1}	–	4	mA	Normal output*5
	I _{OLAV2}	–	30	mA	High-current output*5
“L” level maximum total output current	Σ I _{OL1}	–	125	mA	Normal output
	Σ I _{OL2}	–	160	mA	High-current output
“L” level average total output current	Σ I _{OLAV1}	–	40	mA	Normal output*6
	Σ I _{OLAV2}	–	40	mA	High-current output*6
“H” level maximum output current	I _{OH1}	–	–15	mA	Normal output*4
	I _{OH2}	–	–40	mA	High-current output*4
“H” level average output current	I _{OHAV1}	–	–4	mA	Normal output*5
	I _{OHAV2}	–	–30	mA	High-current output*5
“H” level maximum total output current	Σ I _{OH1}	–	–125	mA	Normal output
	Σ I _{OH2}	–	–160	mA	High-current output
“H” level average total output current	Σ I _{OHAV1}	–	–40	mA	Normal output*6
	Σ I _{OHAV2}	–	–40	mA	High-current output*6
Power consumption	P _D	–	245	mW	
Operating temperature	T _A	–40	+105	°C	
Storage temperature	T _{stg}	–55	+150	°C	

*1: The parameter is based on V_{SS} = AV_{SS} = 0.0 V.

*2: AV_{CC} and AVR should not exceed V_{CC}.

*3: V_I and V_O should not exceed V_{CC} + 0.3 V. However if the maximum current to/from an input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating.

*4: A peak value of an applicable one pin is specified as a maximum output current.

*5: An average current value of an applicable one pin within 100 ms is specified as an average output current. (Average value is found by multiplying operating current by operating rate.)

*6: An average current value of all pins within 100 ms is specified as an average total output current. (Average value is found by multiplying operating current by operating rate.)

*7:

■ Applicable to pins: P10 to P17, P20 to P27, P30 to P33, P35*, P36*, P37, P40 to P44, P50 to P57

*: P35 and P36 are MB90387S and MB90F387S only.

13.2 Recommended Operating Conditions

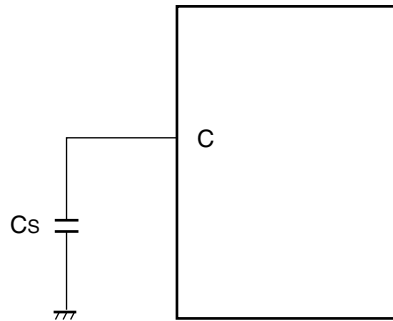
($V_{SS} = AV_{SS} = 0.0V$)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	V _{CC}	3.5	5.0	5.5	V	Under normal operation
		3.0	–	5.5	V	Retain status of stop operation
	AV _{CC}	4.0	–	5.5	V	*2
Smoothing capacitor	C _S	0.1	–	1.0	μF	*1
Operating temperature	T _A	–40	–	+105	°C	

*1: Use a ceramic capacitor, or a capacitor of similar frequency characteristics. On the V_{CC} pin, use a bypass capacitor that has a larger capacity than that of C_S.
Refer to the following figure for connection of smoothing capacitor C_S.

*2: AV_{CC} is a voltage at which accuracy is guaranteed. AV_{CC} should not exceed V_{CC}.

- C pin connection diagram



WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

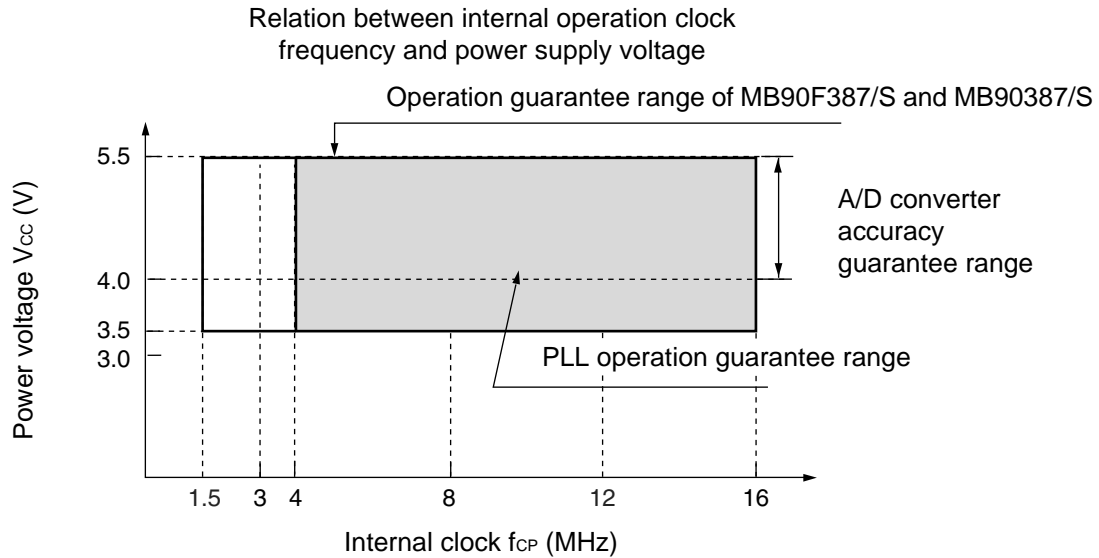
No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

(V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = -40 °C to +105 °C)

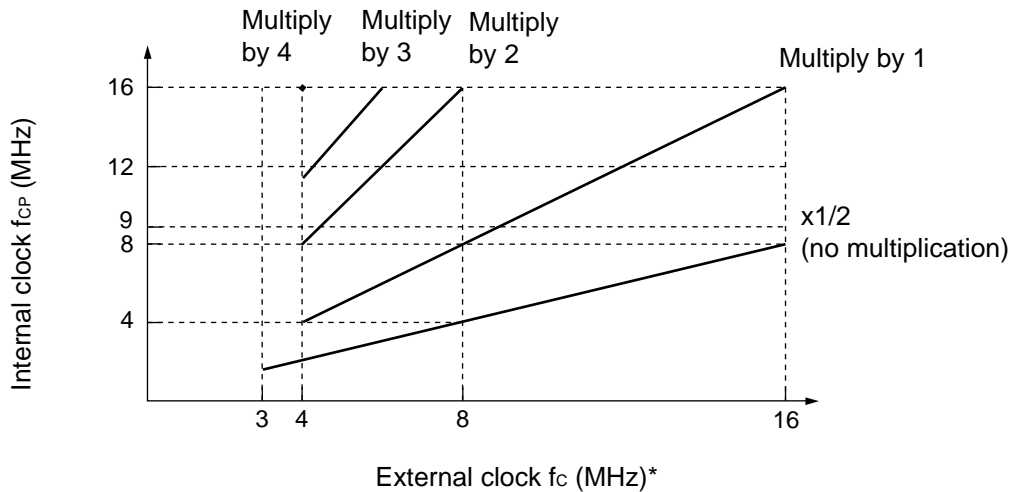
Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current*	I _{CC} L	V _{CC}	V _{CC} = 5.0 V, Internally operating at 8 kHz, subclock operation, T _A = + 25°C	—	0.3	1.2	mA	MB90F387/S
				—	40	100	μA	MB90387/S
	I _{CC} LS		V _{CC} = 5.0 V, Internally operating at 8 kHz, subclock, sleep mode, T _A = + 25°C	—	10	30	μA	
	I _{CC} T		V _{CC} = 5.0 V, Internally operating at 8 kHz, watch mode, T _A = + 25°C	—	8	25	μA	
	I _{CC} H		Stopping, T _A = + 25°C	—	5	20	μA	
Input capacity	C _{IN}	Other than AV _{CC} , AV _{SS} , AVR, C, V _{CC} , V _{SS}	—	—	5	15	pF	
Pull-up resistor	R _{UP}	RST	—	25	50	100	kΩ	
Pull-down resistor	R _{DOWN}	MD2	—	25	50	100	kΩ	Flash product is not provided with pull-down resistor.

*: Test conditions of power supply current are based on a device using external clock.

• PLL operation guarantee range

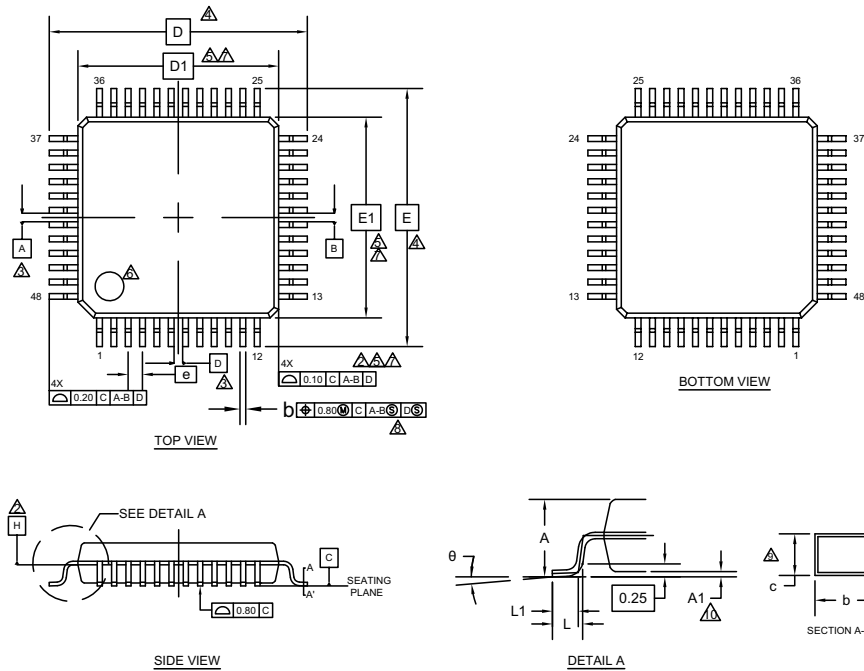


Relation among external clock frequency and internal clock frequency



*: f_c is 8 MHz at maximum when crystal or ceramic resonator circuit is used.

16. Package Dimension



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.00	—	0.20
b	0.15	—	0.27
c	0.09	—	0.20
D	9.00 BSC		
D1	7.00 BSC		
e	0.50 BSC		
E	9.00 BSC		
E1	7.00 BSC		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
θ	0°	—	8°

NOTES

- ALL DIMENSIONS ARE IN MILLIMETERS.
- DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
- DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
- TO BE DETERMINED AT SEATING PLANE C.
- DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
- DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
- REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS, DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
- DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBER PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
- THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
- A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-13731 **

PACKAGE OUTLINE, 48 LEAD LQFP
7.0X7.0X1.7 MM LQA048 REV**