# Infineon Technologies - MB90387SPMT-GS-249E1 Datasheet

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | F²MC-16LX |
| Core Size | 16-Bit |
| Speed | 16MHz |
| Connectivity | CANbus, SCI, UART/USART |
| Peripherals | POR, WDT |
| Number of I/O | 36 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | Mask ROM |
| EEPROM Size | - |
| RAM Size | 2K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3.5V ~ 5.5V |
| Data Converters | A/D 8x8/10b |
| Oscillator Type | External |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 48-LQFP |
| Supplier Device Package | 48-LQFP (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/mb90387spmt-gs-249e1 |

### DTP/External Interrupt: 4 channels, CAN wakeup: 1channel

- Module for activation of expanded intelligent I/O service ($EI^2OS$), and generation of external interrupt.

### Delay Interrupt Generator Module

- Generates interrupt request for task switching.

### 8/10-bit A/D Converter: 8 channels

- Resolution is selectable between 8-bit and 10-bit.
- Activation by external trigger input is allowed.
- Conversion time: 6.125 μs (at 16 MHz machine clock, including sampling time)

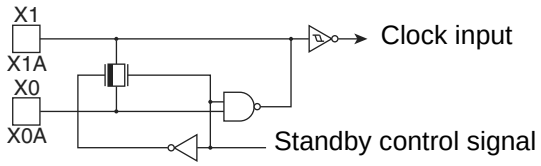
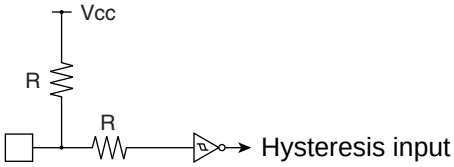
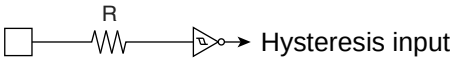
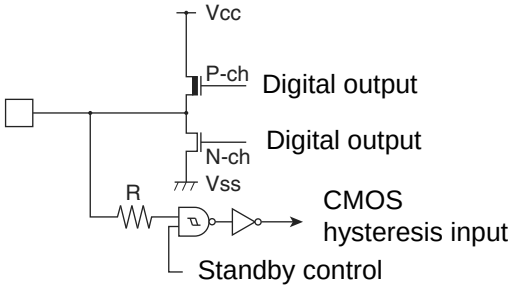
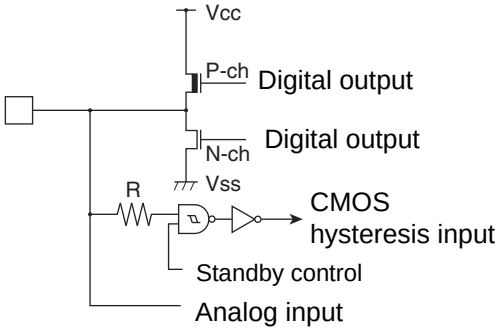
### Program Patch Function

- Address matching detection for 2 address pointers.

## 1. Product Lineup

| Parameter \ Part Number | | MB90F387<br>MB90F387S | MB90387<br>MB90387S | MB90V495G |
|---|---|---|---|---|
| Classification | | Flash ROM | Mask ROM | Evaluation product |
| ROM capacity | | 64 Kbytes | | – |
| RAM capacity | | 2 Kbytes | | 6 Kbytes |
| Process | | CMOS | | |
| Package | | LQFP-48 (pin pitch 0.50 mm) | | PGA-256 |
| Operating power supply voltage | | 3.5 V to 5.5 V | | 4.5 V to 5.5 V |
| Special power supply for emulator*1 | | – | | None |
| CPU functions | | Number of basic instructions : 351 instructions<br>Instruction bit length : 8 bits and 16 bits<br>Instruction length : 1 byte to 7 bytes<br>Data bit length : 1 bit, 8 bits, 16 bits | | |
| | | Minimum instruction execution time: 62.5 ns (at 16 MHz machine clock) | | |
| | | Interrupt processing time: 1.5 μs at minimum (at 16 MHz machine clock) | | |
| Low power consumption (standby) mode | | Sleep mode / Watch mode / Time-base timer mode / Stop mode / CPU intermittent | | |
| I/O port | | General-purpose input/output ports (CMOS output): 34 ports (36 ports*2)<br>including 4 high-current output ports (P14 to P17) | | |
| Time-base timer | | 18-bit free-run counter<br>Interrupt cycle: 1.024 ms, 4.096 ms, 16.834 ms, 131.072 ms<br>(with oscillation clock frequency at 4 MHz) | | |
| Watchdog timer | | Reset generation cycle: 3.58 ms, 14.33 ms, 57.23 ms, 458.75 ms<br>(with oscillation clock frequency at 4 MHz) | | |
| 16-bit input/ output timer | 16-bit free-run timer | Number of channels: 1<br>Interrupt upon occurrence of overflow | | |
| | Input capture | Number of channels: 4<br>Retaining free-run timer value set by pin input (rising edge, falling edge, and both edges) | | |
| 16-bit reload timer | | Number of channels: 2<br>16-bit reload timer operation<br>Count clock cycle: 0.25 μs, 0.5 μs, 2.0 μs<br>(at 16-MHz machine clock frequency)<br>External event count is allowed. | | |
| Watch timer | | 15-bit free-run counter<br>Interrupt cycle: 31.25 ms, 62.5 ms, 12 ms, 250 ms, 500 ms, 1.0 s, 2.0 s<br>(with 8.192 kHz sub clock) | | |
| 8/16-bit PPG timer | | Number of channels: 2 (four 8-bit channels are available also.)<br>PPG operation is allowed with four 8-bit channels or two 16-bit channels.<br>Outputting pulse wave of arbitrary cycle or arbitrary duty is allowed.<br>Count clock: 62.5 ns to 1 μs<br>(with 16 MHz machine clock) | | |
| Delay interrupt generator module | | Interrupt generator module for task switching. Used for realtime OS. | | |
| DTP/External interrupt | | Number of inputs: 4<br>Activated by rising edge, falling edge, “H” level or “L” level input.<br>External interrupt or expanded intelligent I/O service (EI$^2$OS) is available. | | |

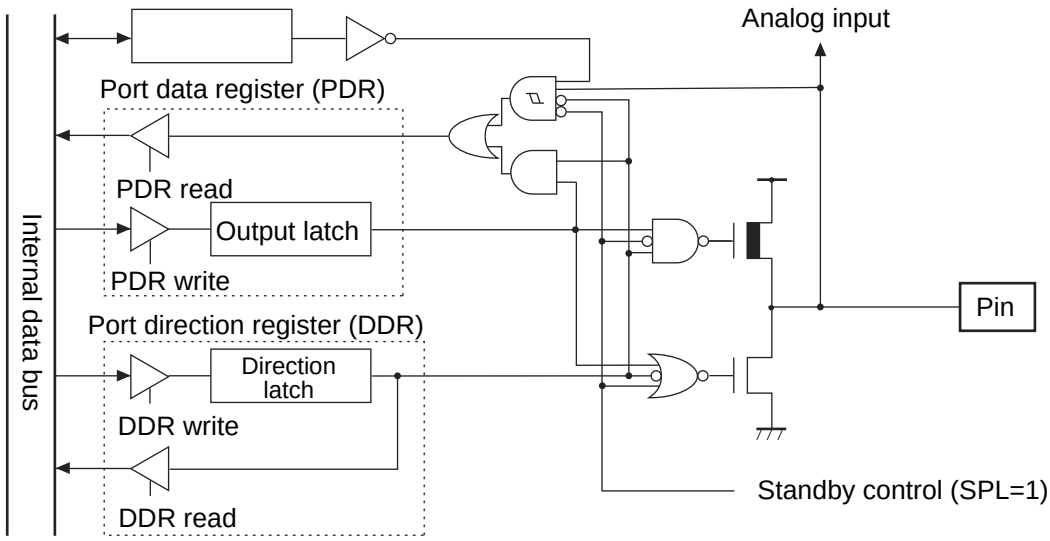
## 6. I/O Circuit Type

| Type | Circuit | Remarks |
|---|---|---|
| A |  | ■ High-rate oscillation feedback resistor, approx.1 MΩ<br>■ Low-rate oscillation feedback resistor, approx.10 MΩ |
| B |  | ■ Hysteresis input with pull-up resistor.<br>■ Pull-up resistor, approx.50 kΩ |
| C |  | ■ Hysteresis input |
| D |  | ■ CMOS hysteresis input<br>■ CMOS level output<br>■ Standby control provided |
| E |  | ■ CMOS hysteresis input<br>■ CMOS level output<br>■ Shared for analog input pin<br>■ Standby control provided |

| Address | Register Abbreviation | Register | Read/ Write | Resource | Initial Value |
|---|---|---|---|---|---|
| 000083H | (Reserved area) * | | | | |
| 000084H | TCANR | Send cancel register | W | CAN controller | 00000000B |
| 000085H | (Reserved area) * | | | | |
| 000086H | TCR | Send completion register | R/W | CAN controller | 00000000B |
| 000087H | (Reserved area) * | | | | |
| 000088H | RCR | Receive completion register | R/W | CAN controller | 00000000B |
| 000089H | (Reserved area) * | | | | |
| 00008AH | RRTRR | Receive RTR register | R/W | CAN controller | 00000000B |
| 00008BH | (Reserved area) * | | | | |
| 00008CH | ROVRR | Receive overrun register | R/W | CAN controller | 00000000B |
| 00008DH | (Reserved area) * | | | | |
| 00008EH | RIER | Receive completion interrupt permission register | R/W | CAN controller | 00000000B |
| 00008FH to 00009DH | (Reserved area) * | | | | |
| 00009EH | PACSR | Address detection control register | R/W | Address matching detection function | 00000000B |
| 00009FH | DIRR | Delay interrupt request generation/ release register | R/W | Delay interrupt generation module | XXXXXXX0B |
| 0000A0H | LPMCR | Lower power consumption mode control register | W,R/W | Lower power consumption mode | 00011000B |
| 0000A1H | CKSCR | Clock selection register | R,R/W | Clock | 11111100B |
| 0000A2H to 0000A7H | (Reserved area) * | | | | |
| 0000A8H | WDTC | Watchdog timer control register | R,W | Watchdog timer | XXXXX111B |
| 0000A9H | TBTC | Time-base timer control register | R/W,W | Time-base timer | 1XX00100B |
| 0000AAH | WTC | Watch timer control register | R,R/W | Watch timer | 1X001000B |
| 0000ABH to 0000ADH | (Reserved area) * | | | | |
| 0000AEH | FMCS | Flash memory control status register | R,W,R/W | 512k-bit Flash memory | 000X0000B |
| 0000AFH | (Reserved area) * | | | | |

| Address | Register Abbreviation | Register | Read/ Write | Resource | Initial Value |
|---|---|---|---|---|---|
| 0000B0H | ICR00 | Interrupt control register 00 | R/W | Interrupt controller | 00000111B |
| 0000B1H | ICR01 | Interrupt control register 01 | | | 00000111B |
| 0000B2H | ICR02 | Interrupt control register 02 | | | 00000111B |
| 0000B3H | ICR03 | Interrupt control register 03 | | | 00000111B |
| 0000B4H | ICR04 | Interrupt control register 04 | | | 00000111B |
| 0000B5H | ICR05 | Interrupt control register 05 | | | 00000111B |
| 0000B6H | ICR06 | Interrupt control register 06 | | | 00000111B |
| 0000B7H | ICR07 | Interrupt control register 07 | | | 00000111B |
| 0000B8H | ICR08 | Interrupt control register 08 | | | 00000111B |
| 0000B9H | ICR09 | Interrupt control register 09 | | | 00000111B |
| 0000BAH | ICR10 | Interrupt control register 10 | | | 00000111B |
| 0000BBH | ICR11 | Interrupt control register 11 | | | 00000111B |
| 0000BCH | ICR12 | Interrupt control register 12 | | | 00000111B |
| 0000BDH | ICR13 | Interrupt control register 13 | | | 00000111B |
| 0000BEH | ICR14 | Interrupt control register 14 | | | 00000111B |
| 0000BFH | ICR15 | Interrupt control register 15 | | | 00000111B |
| 0000C0H to 0000FFH | (Reserved area) * | | | | |
| 001FF0H | PADR0 | Detection address setting register 0 (low-order) | R/W | Address matching detection function | XXXXXXXXB |
| 001FF1H | | Detection address setting register 0 (middle-order) | | | XXXXXXXXB |
| 001FF2H | | Detection address setting register 0 (high-order) | | | XXXXXXXXB |
| 001FF3H | PADR1 | Detection address setting register 1 (low-order) | R/W | | XXXXXXXXB |
| 001FF4H | | Detection address setting register 1 (middle-order) | | | XXXXXXXXB |
| 001FF5H | | Detection address setting register 1 (high-order) | | | XXXXXXXXB |
| 003900H | TMR0/ TMRLR0 | 16-bit timer register 0/16-bit reload register | R,W | 16-bit reload timer 0 | XXXXXXXXB |
| 003901H | | | | | XXXXXXXXB |
| 003902H | TMR1/ TMRLR1 | 16-bit timer register 1/16-bit reload register | R,W | 16-bit reload timer 1 | XXXXXXXXB |
| 003903H | | | | | XXXXXXXXB |
| 003904H to 00390FH | (Reserved area) * | | | | |

**Port 5 Pins Block Diagram**




Standby control: Control among Stop mode (SPL=1), Time-base timer mode (SPL=1), and watch mode (SPL=1).

**Port 5 Registers**

- Port 5 registers include port 5 data register (PDR5), port 5 direction register (DDR5), and analog input permission register (ADER).
- Analog input permission register (ADER) allows or disallows input of analog signal to the analog input pin.
- The bits configuring the register correspond to port 5 pins on a one-to-one basis.

**Relation between Port 5 Registers and Pins**

| Port Name | Bits of Register and Corresponding Pins | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Port 5 | PDR5, DDR5 | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
| | ADER | ADE7 | ADE6 | ADE5 | ADE4 | ADE3 | ADE2 | ADE1 | ADE0 |
| | Corresponding pins | P57 | P56 | P55 | P54 | P53 | P52 | P51 | P50 |

## 12.2 Time-Base Timer

The time-base time is an 18-bit free-run counter (time-base timer counter) that counts up in synchronization with the main clock (dividing main oscillation clock by 2).

- Four choices of interval time are selectable, and generation of interrupt request is allowed for each interval time.
- Provides operation clock signal to oscillation stabilizing wait timer and peripheral functions.

### Interval Timer Function

- When the counter of time-base timer reaches an interval time specified by interval time selection bit (TBTC:TBC1, TBC0), an overflow (carrying-over) occurs (TBTC: TBOF=1) and interrupt request is generated.
- If an interrupt by overflow is permitted (TBTC: TBIE=1), an interrupt is generated when overflow occurs (TBTC: TBOF=1).
- The following four interval time settings are selectable:

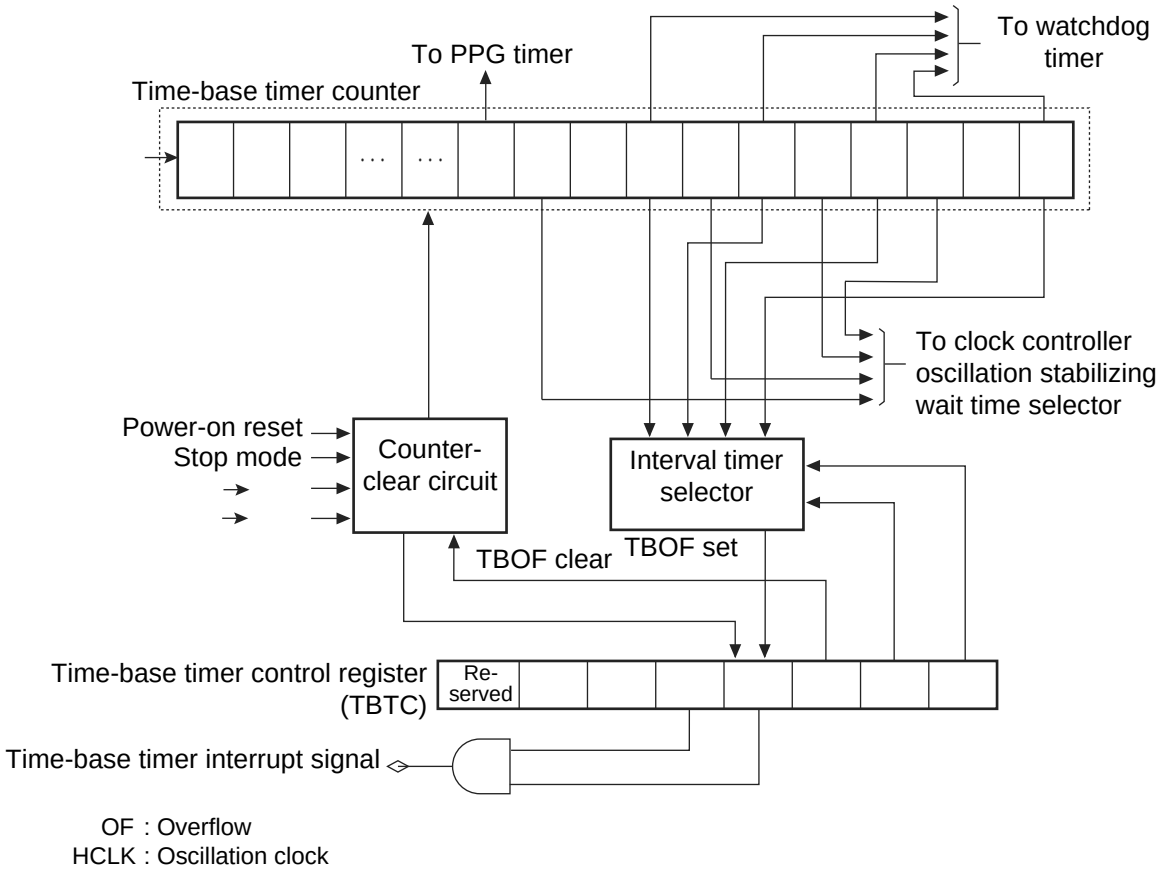
### Interval Time of Time-base Timer

| Count Clock | Interval Time |
|---|---|
| 2/HCLK (0.5 μs) | $2^{12}$/HCLK (Approx. 1.0 ms) |
| | $2^{14}$/HCLK (Approx. 4.1 ms) |
| | $2^{16}$/HCLK (Approx. 16.4 ms) |
| | $2^{19}$/HCLK (Approx. 131.1 ms) |

HCLK: Oscillation clock

Values in parentheses “( )” are those under operation of 4-MHz oscillation clock.

**Time-base Timer Block Diagram**




OF : Overflow
HCLK : Oscillation clock

*1: Switch machine clock from main clock to PLL clock.

*2: Switch machine clock from sub clock to main clock.

Actual interrupt request number of time-base timer is as follows:

Interrupt request number: #16 ($10_H$)

## 12.3 Watchdog Timer

The watchdog timer is a 2-bit counter that uses time-base timer or watch timer as count clock. If the counter is not cleared within an interval time, CPU is reset.

### Watchdog Timer Functions

- The watchdog timer is a timer counter that prevents runaway of a program. Once a watchdog timer is activated, the counter of watchdog timer must always be cleared within a specified time of interval. If specified interval time elapses without clearing the counter of a watchdog timer, CPU resetting occurs. This is the function of a watchdog timer.
- The interval time of a watchdog timer is determined by a clock cycle, which is input as a count clock. Watchdog resetting occurs between a minimum time and a maximum time specified.
- The output target of a clock source is specified by the watchdog clock selection bit (WTC: WDCS) in the watch timer control register.
- Interval time of a watchdog timer is specified by the time-base timer output selection bit / watch timer output selection bit (WDTC: WT1, WT0) in the watchdog timer control register.

### Interval Timer of Watchdog Timer

| Min | Max | Clock Cycle | Min | Max | Clock Cycle |
|---|---|---|---|---|---|
| Approx. 3.58 ms | Approx. 4.61 ms | $(2^{14}\pm2^{11})$ /HCLK | Approx. 0.457 s | Approx. 0.576 s | $(2^{12}\pm2^{9})$ /SCLK |
| Approx. 14.33 ms | Approx. 18.3 ms | $(2^{16}\pm2^{13})$ /HCLK | Approx. 3.584 s | Approx. 4.608 s | $(2^{15}\pm2^{12})$ /SCLK |
| Approx. 57.23 ms | Approx. 73.73 ms | $(2^{18}\pm2^{15})$ /HCLK | Approx. 7.168 s | Approx. 9.216 s | $(2^{16}\pm2^{13})$ /SCLK |
| Approx. 458.75 ms | Approx. 589.82 ms | $(2^{21}\pm2^{18})$ /HCLK | Approx. 14.336 s | Approx. 18.432 s | $(2^{17}\pm2^{14})$ /SCLK |

HCLK: Oscillation clock (4 MHz), CSCLK: Sub clock (8.192 kHz)

Notes:

- If the time-base timer is cleared when watchdog timer count clock is used as time base timer output (carry-over signal), watchdog reset time may become longer.
- When using the sub clock as machine clock, be sure to specify watchdog timer clock source selection bit (WDCS) in watch timer control register (WTC) at “0,” selecting output of watch timer.

## 12.4 16-bit Input/Output Timer

The 16-bit input/output timer is a compound module composed of 16-bit free-run timer, (1 unit) and input capture (2 units, 4 input pins). The timer, using the 16-bit free-run timer as a basis, enables measurement of clock cycle of an input signal and its pulse width.

### Configuration of 16-bit Input/Output Timer

The 16-bit input/output timer is composed of the following modules:

- 16-bit free-run timer (1 unit)
- Input capture (2 units, 2 input pins per unit)

### Functions of 16-bit Input/Output Timer

*Functions of 16-bit Free-run Timer*

The 16-bit free-run timer is composed of 16-bit up counter, timer counter control status register, and prescaler. The 16-bit up counter increments in synchronization with dividing ratio of machine clock.

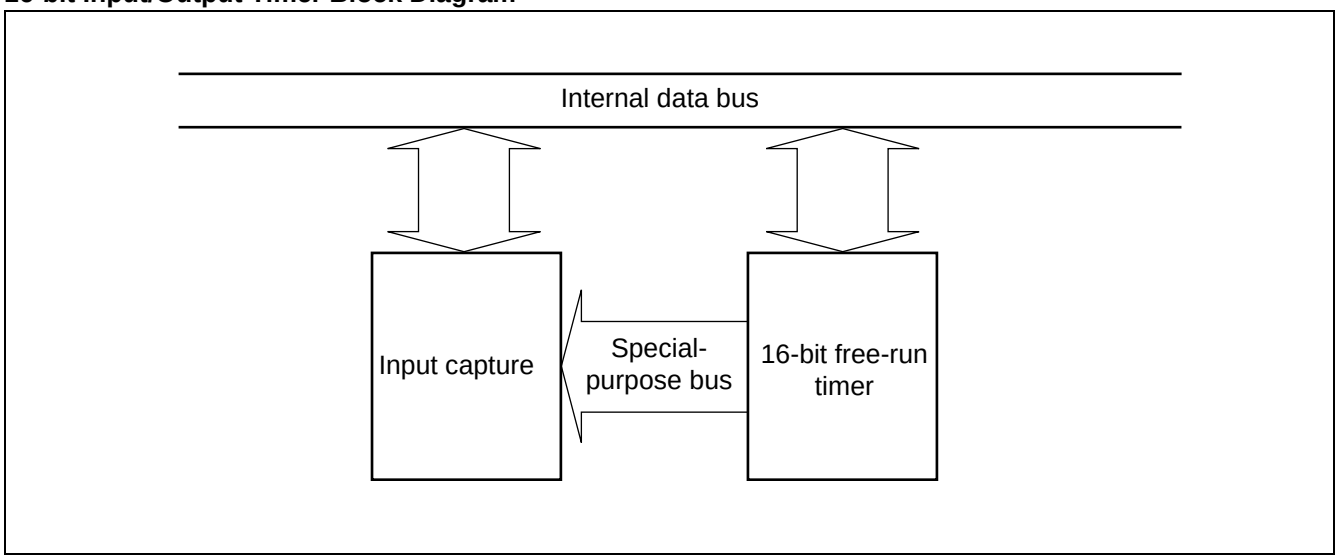
- Count clock is set among four types of machine clock dividing rates.
- Generation of interrupt is allowed by counter value overflow.
- Activation of expanded intelligent I/O service (EI$^2$OS) is allowed by interrupt generation.
- Counter value of 16-bit free-run timer is cleared to "0000$_H$" by either resetting or software-clearing with timer count clear bit (TCCS: CLR).
- Counter value of 16-bit free-run timer is output to input capture, which is available as base time for capture operation.

*Functions of Input Capture*

The input capture, upon detecting an edge of a signal input to the input pin from external device, stores a counter value of 16-bit free-run timer at the time of detection into the input capture data register. The function includes the input capture data registers corresponding to four input pins, input capture control status register, and edge detection circuit.

- Rising edge, falling edge, and both edges are selectable for detection.
- Generating interrupt on CPU is allowed by detecting an edge of input signal.
- Expanded intelligent I/O service (EI$^2$OS) is activated by interrupt generation.
- The four input capture input pins and input capture data registers allows monitoring of a maximum of four events.

### 16-bit Input/Output Timer Block Diagram



## 12.7 8/16-bit PPG Timer Outline

The 8/16-bit PPG timer is a 2-channel reload timer module (PPG0 and PPG1) that allows outputting pulses of arbitrary cycle and duty cycle. Combination of the two channels allows selection among the following operations:

- 8-bit PPG output 2-channel independent operation mode
- 16-bit PPG output operation mode
- 8-bit and 8-bit PPG output operation mode

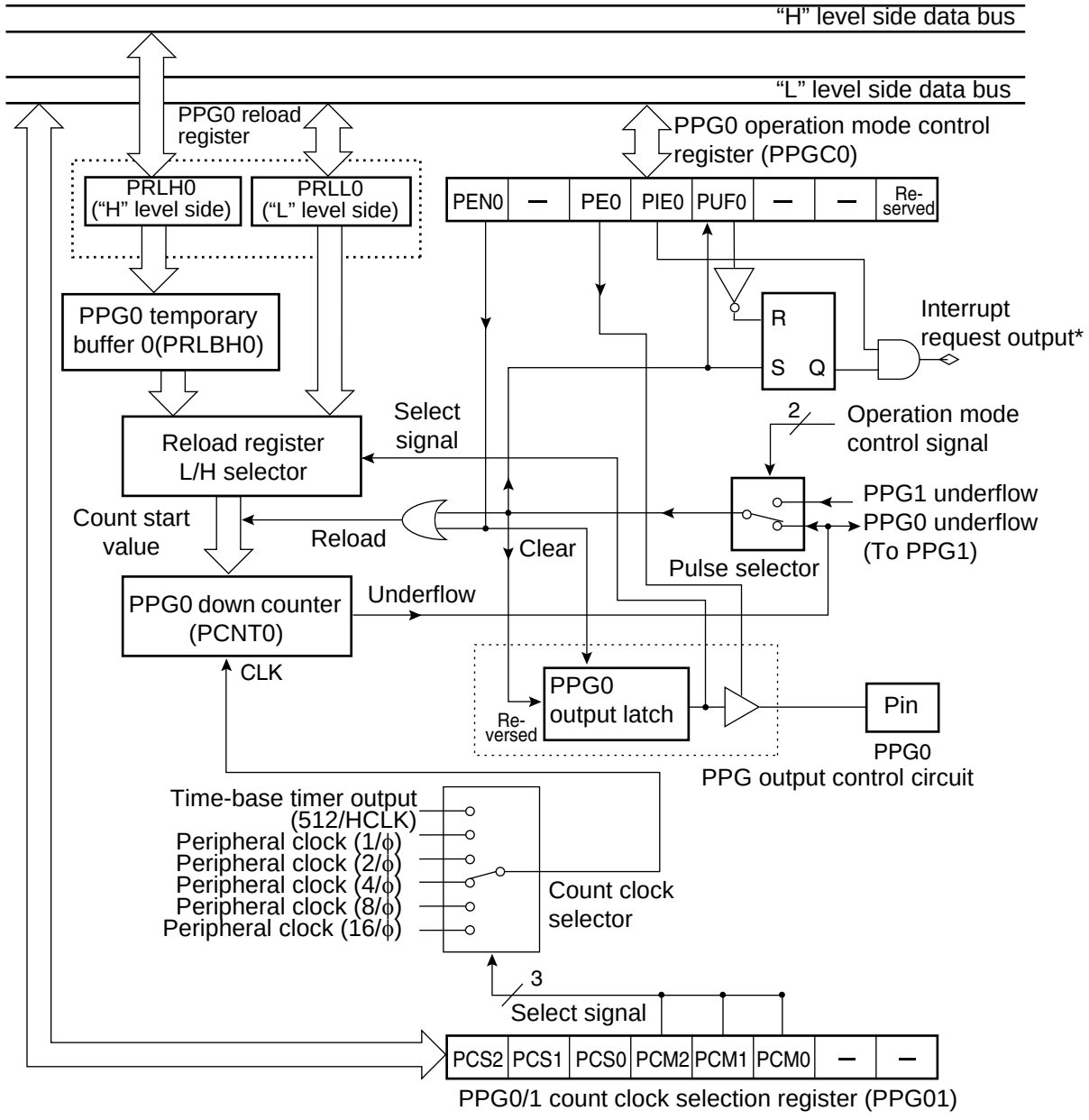
MB90385 series device has two 8/16-bit built-in PPG timers. This section describes functions of PPG0/1. PPG2/3 have the same functions as those of PPG0/1.

### Functions of 8/16-bit PPG Timer

The 8/16-bit PPG timer is composed of four 8-bit reload register (PRLH0/PRLL0, PRLH1/PRLL1) and two PPG down counters (PCNT0, PCNT1).

- Widths of “H” and “L” in output pulse are specifiable independently. Cycle and duty factor of output pulse is specifiable arbitrarily.
- Count clock is selectable among 6 internal clocks.
- The timer is usable as an interval timer, by generating interrupt requests for each interval.
- The time is usable as a D/A converter, with an external circuit.

**8/16-bit PPG Timer 0 Block Diagram**




– : Undefined
Reserved: Reserved bit
HCLK : Oscillation clock frequency
ϕ : Machine clock frequency
* : Interrupt output of 8/16-bit PPG timer 0 is incorporated into one by the OR circuit against interrupt output of 8/16-bit PPG timer 1.

### 13.2 Recommended Operating Conditions

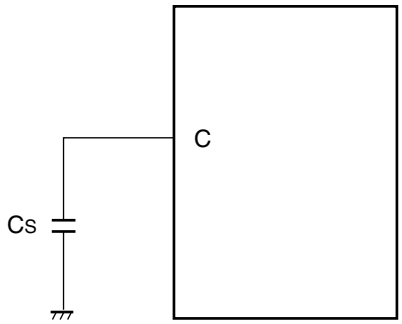
($V_{SS}$ = $AV_{SS}$ = 0.0V)

| Parameter | Symbol | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| Power supply voltage | $V_{CC}$ | 3.5 | 5.0 | 5.5 | V | Under normal operation |
| | | 3.0 | – | 5.5 | V | Retain status of stop operation |
| | $AV_{CC}$ | 4.0 | – | 5.5 | V | *2 |
| Smoothing capacitor | $C_S$ | 0.1 | – | 1.0 | μF | *1 |
| Operating temperature | $T_A$ | −40 | – | +105 | °C | |

*1: Use a ceramic capacitor, or a capacitor of similar frequency characteristics. On the Vcc pin, use a bypass capacitor that has a larger capacity than that of Cs.
Refer to the following figure for connection of smoothing capacitor Cs.

*2: AVcc is a voltage at which accuracy is guaranteed. AVcc should not exceed Vcc.

- C pin connection diagram




WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

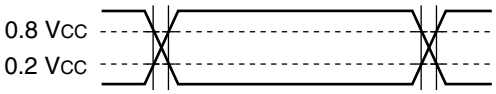
Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

Rating values of alternating current is defined by the measurement reference voltage values shown below:

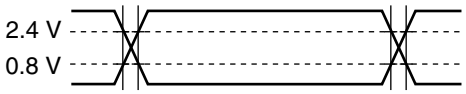
- Input signal waveform

Hysteresis input pin




- Output signal waveform

Output pin




*13.4.2 Reset Input Timing*

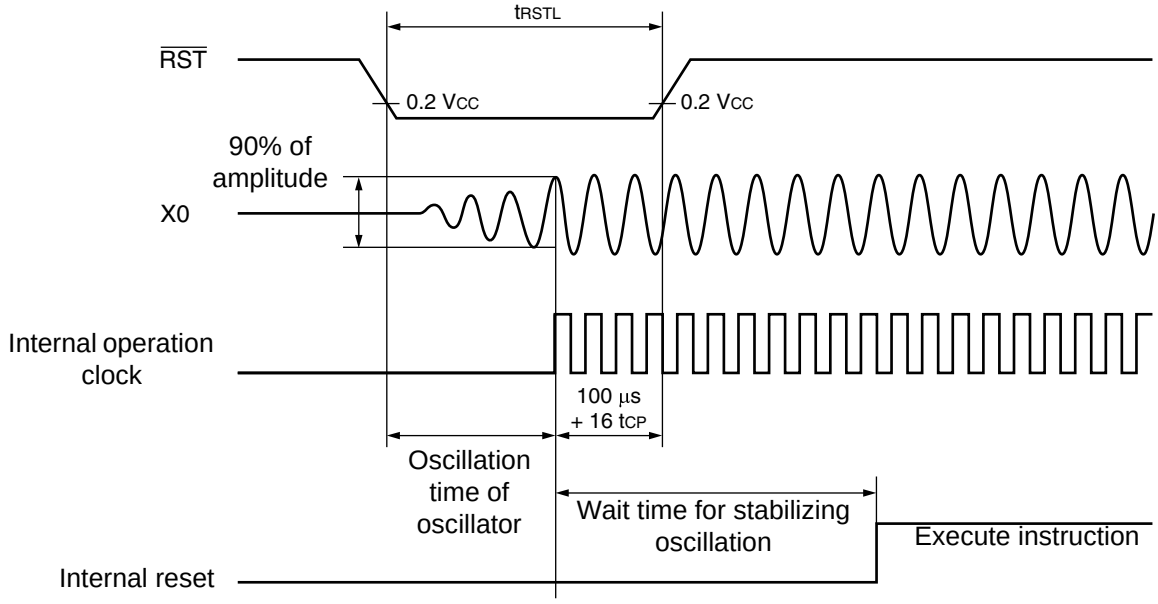
| Parameter | Symbol | Pin Name | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | | Min | Max | | |
| Reset input time | $t_{RSTL}$ | RST | 16 $t_{CP}$*3 | – | ns | Normal operation |
| | | | Oscillation time of oscillator*1 + 100 μs + 16 $t_{CP}$*3 | – | – | In sub clock*2, sub sleep*2, watch*2 and stop mode |
| | | | 100 | – | μs | In timebase timer |

*1: Oscillation time of oscillator is time that the amplitude reached the 90%. In the crystal oscillator, the oscillation time is between several ms to tens of ms. In ceramic oscillator, the oscillation time is between hundreds of μs to several ms. In the external clock, the oscillation time is 0 ms.

*2: Except for MB90F387S and MB90387S.

*3: Refer to "(1) Clock timing" ratings for $t_{CP}$ (internal operation clock cycle time).

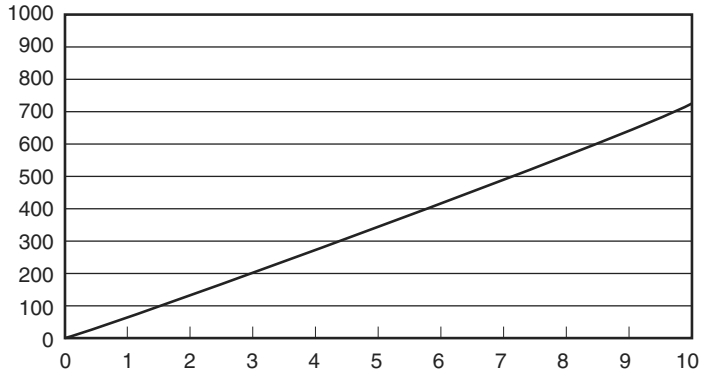
- In sub clock, sub sleep, watch and stop mode



*(Continued)*

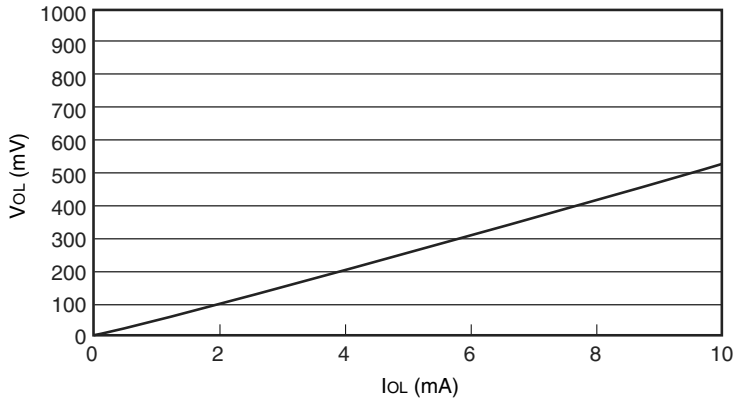
**($V_{CC}$ - $V_{OH}$) – $I_{OH}$**

$T_A$ = +25 °C, $V_{CC}$ = 4.5 V



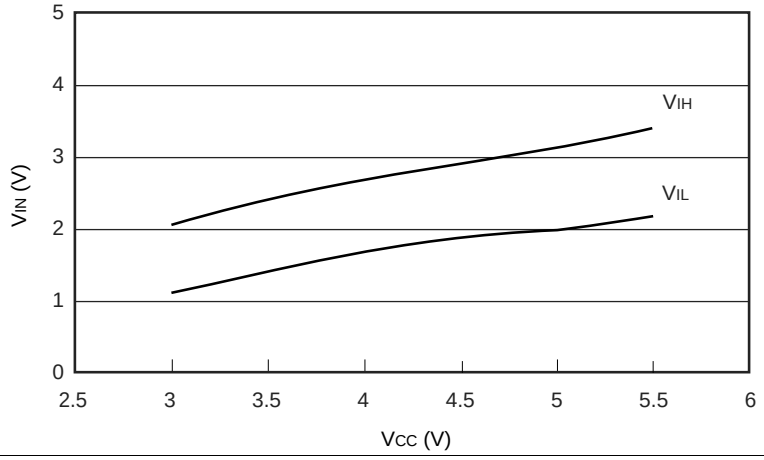

**$V_{OL}$ – $I_{OL}$**

$T_A$ = +25 °C, $V_{CC}$ = 4.5 V



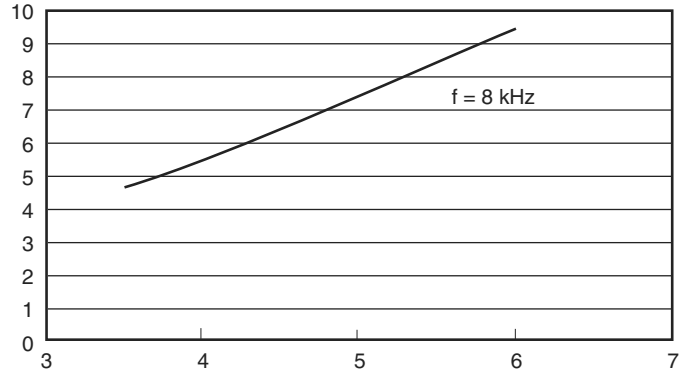

**H level input voltage/ L level input voltage**
**$V_{IN}$ – $V_{CC}$**

$T_A$ = +25 °C



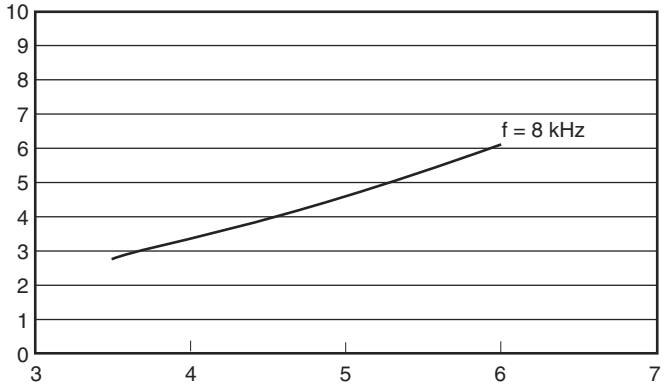
**$I_{CCLS}$ – $V_{CC}$**

$T_A$ = +25 °C, In external clock operation
f = Internal operating frequency



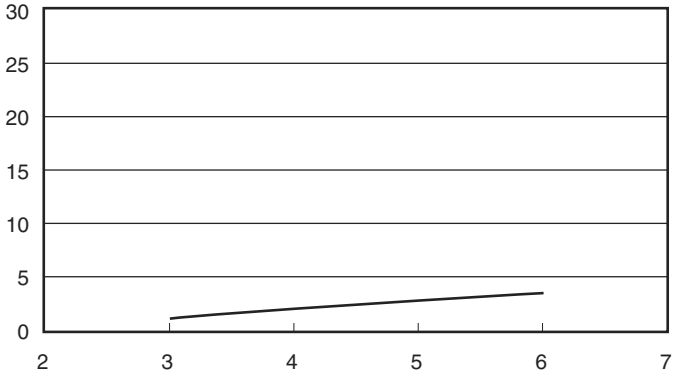

**$I_{CCT}$ – $V_{CC}$**

$T_A$ = +25 °C, In external clock operation
f = Internal operating frequency




**$I_{CCH}$ – $V_{CC}$**

Stopping, $T_A$ = +25 °C

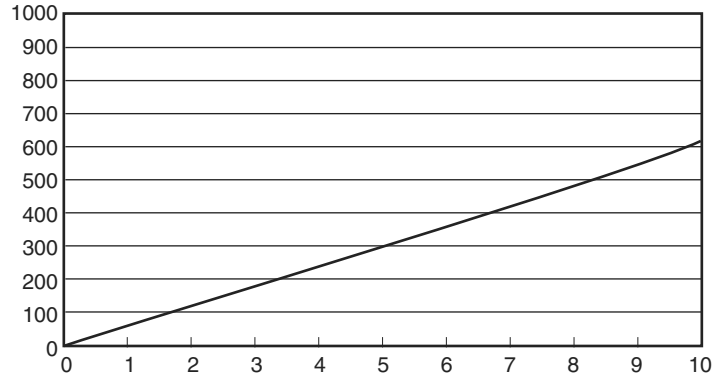



*(Continued)*

*(Continued)*

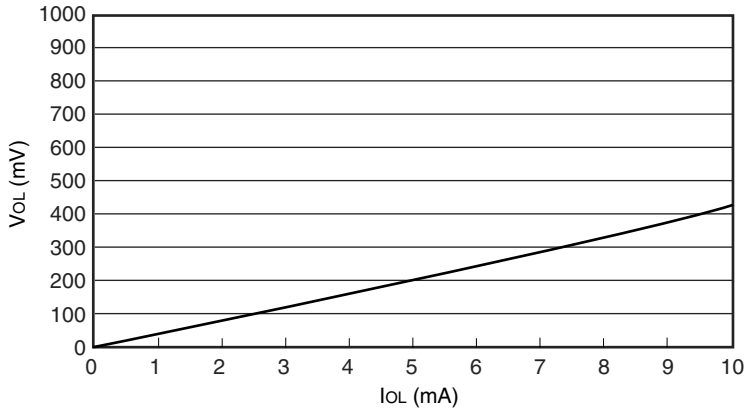
**($V_{CC}$ - $V_{OH}$) – $I_{OH}$**

$T_A$ = +25 °C, $V_{CC}$ = 4.5 V



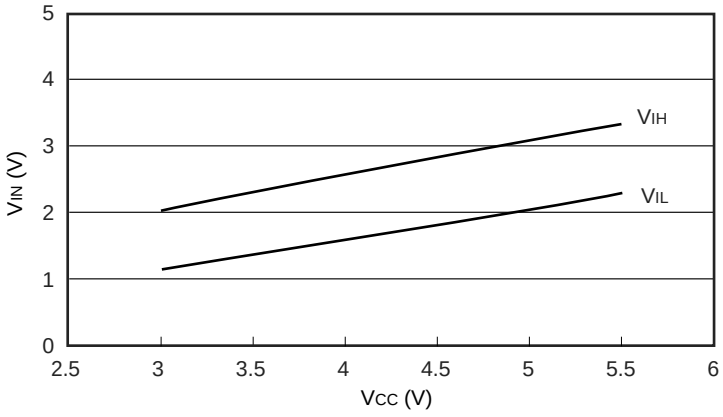

**$V_{OL}$ – $I_{OL}$**

$T_A$ = +25 °C, $V_{CC}$ = 4.5 V

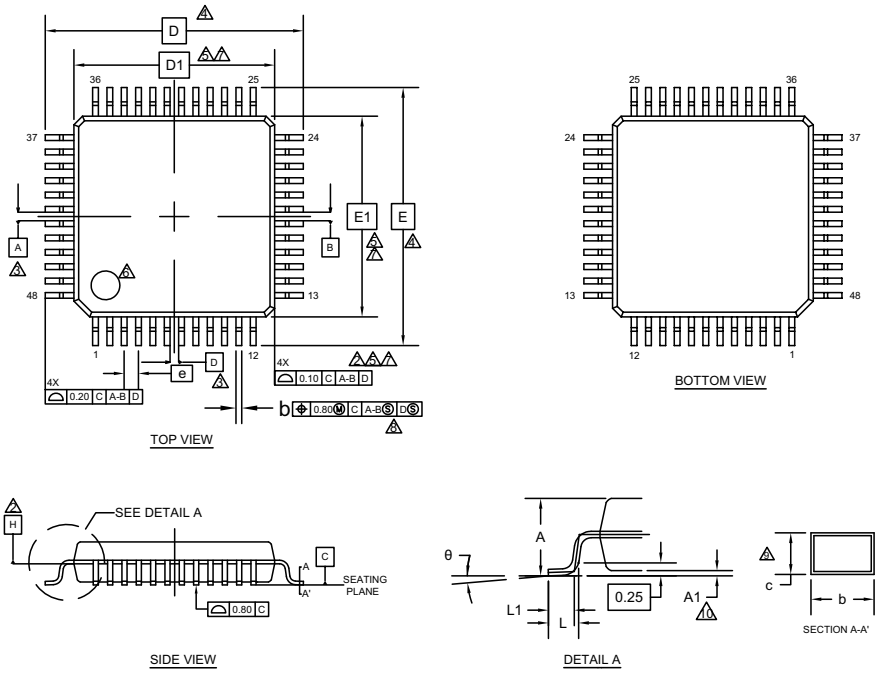



**H level input voltage/ L level input voltage**
**$V_{IN}$ – $V_{CC}$**

$T_A$ = +25 °C



## 16. Package Dimension




| SYMBOL | DIMENSIONS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | — | — | 1.70 |
| A1 | 0.00 | — | 0.20 |
| b | 0.15 | — | 0.27 |
| c | 0.09 | — | 0.20 |
| D | 9.00 BSC | | |
| D1 | 7.00 BSC | | |
| e | 0.50 BSC | | |
| E | 9.00 BSC | | |
| E1 | 7.00 BSC | | |
| L | 0.45 | 0.60 | 0.75 |
| L1 | 0.30 | 0.50 | 0.70 |
| θ | 0° | — | 8° |

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-13731 **

PACKAGE OUTLINE, 48 LEAD LQFP
7.0X7.0X1.7 MM LQA048 REV**

## 17. Major Changes

Spansion Publication Number: DS07-13717-5E

| Page | Section | Change Results |
|---|---|---|
| 4 | ■ PRODUCT LINEUP | Changed the number of channel of 8/16 bit PPG timer.<br>or one 16-bit channel → or two 16-bit channels |
| 13 | ■ BLOCK DIAGRAM | Changed the direction of arrow of TIN0, TIN1 signals of 16-bit reload timer.<br>right arrow (output) → left arrow (input) |
| 67 | ■ ELECTRIC CHARACTERISTICS<br>4. AC Characteristics<br>(4) UART timing | Changed the value of Serial clock.<br>Serial clock “H” pulse width: $4t_{CP} \rightarrow 2t_{CP}$<br>Serial clock “L” pulse width: $4t_{CP} \rightarrow 2t_{CP}$ |

**NOTE: Please see "Document History" about later revised information.**

## Document History

| Document Title: MB90387/387S/F387/F387S, MB90V495G, 16-bit Microcontrollers F²MC-16LX MB90385 Series<br>Document Number:002-07765 | | | | |
|---|---|---|---|---|
| **Revision** | **ECN** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| ** | — | AKIH | 12/19/2008 | Migrated to Cypress and assigned document number 002-07765.<br>No change to document contents or format. |
| *A | 6059071 | SSAS | 02/05/2018 | Updated to Cypress template<br>Package: FPT-48P-M26 --> LQA048 |