Infineon Technologies - MB90387SPMT-GS-255 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, SCI, UART/USART
Peripherals	POR, WDT
Number of I/O	36
Program Memory Size	64KB (64K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90387spmt-gs-255

MB90387/387S/F387/F387S
MB90V495G

16-bit Microcontrollers
F²MC-16LX MB90385 Series

MB90385 series devices are general-purpose high-performance 16-bit micro controllers designed for process control of consumer products, which require high-speed real-time processing. The devices of this series have the built-in full-CAN interface.
The system, inheriting the architecture of F²MC family, employs additional instruction ready for high-level languages, expanded addressing mode, enhanced multiply-divide instructions, and enriched bit-processing instructions. Furthermore, employment of 32-bit accumulator achieves processing of long-word data (32 bits).
The peripheral resources of MB90385 series include the following:
8/10-bit A/D converter, UART (SCI), 8/16-bit PPG timer, 16-bit input-output timer (16-bit free-run timer, input capture 0, 1, 2, 3 (ICU)), and CAN controller.

Features

Clock

- Built-in PLL clock frequency multiplication circuit
- Selection of machine clocks (PLL clocks) is allowed among frequency division by two on oscillation clock, and multiplication of 1 to 4 times of oscillation clock (for 4-MHz oscillation clock, 4 MHz to 16 MHz).
- Operation by sub-clock (8.192 kHz) is allowed. (MB90387, MB90F387)
- Minimum execution time of instruction: 62.5 ns (when operating with 4-MHz oscillation clock, and 4-time multiplied PLL clock).

16 Mbyte CPU memory Space

- 24-bit internal addressing

Instruction System Best Suited to Controller

- Wide choice of data types (bit, byte, word, and long word)
- Wide choice of addressing modes (23 types)
- Enhanced multiply-divide instructions and RETI instructions
- Enhanced high-precision computing with 32-bit accumulator

Instruction System Compatible with High-level Language (C language) and Multitask

- Employing system stack pointer
- Enhanced various pointer indirect instructions
- Barrel shift instructions

Increased Processing Speed

- 4-byte instruction queue

Powerful Interrupt Function with 8 Levels and 34 Factors

Automatic Data Transfer Function Independent of CPU

- Expanded intelligent I/O service function (EI² OS): Maximum of 16 channels

Low Power Consumption (standby) Mode

- Sleep mode (a mode that halts CPU operating clock)
- Time-base timer mode (a mode that operates oscillation clock, sub clock, time-base timer and watch timer only)
- Watch mode (a mode that operates sub clock and watch timer only)
- Stop mode (a mode that stops oscillation clock and sub clock)
- CPU blocking operation mode

Process

- CMOS technology

I/O Port

- General-purpose input/output port (CMOS output):

  MB90387, MB90F387: 34 ports (including 4 high-current output ports)
  MB90387S, MB90F387S: 36 ports (including 4 high-current output ports)

Timer

- Time-base timer, watch timer, watchdog timer: 1 channel
- 8/16-bit PPG timer: 8-bit x 4 channels, or 16-bit x 2 channels
- 16-bit reload timer: 2 channels
- 16-bit input/output timer
  - ❒ 16-bit free run timer: 1 channel
  - ❒ 16-bit input capture: (ICU): 4 channels

  Interrupt request is issued upon latching a count value of 16-bit free run timer by detection of an edge on pin input.

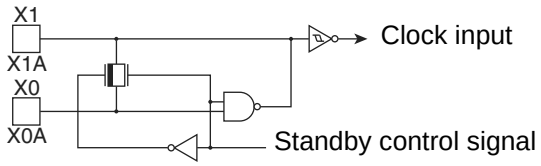
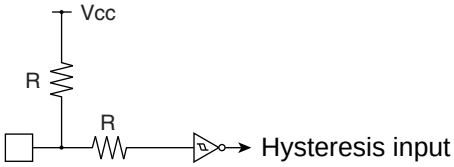
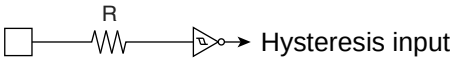
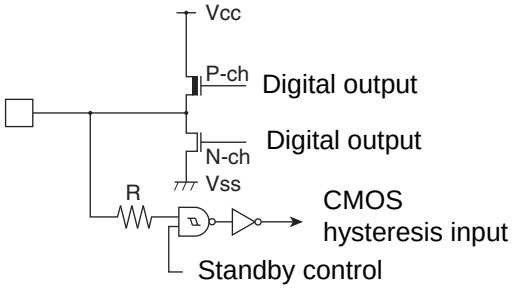
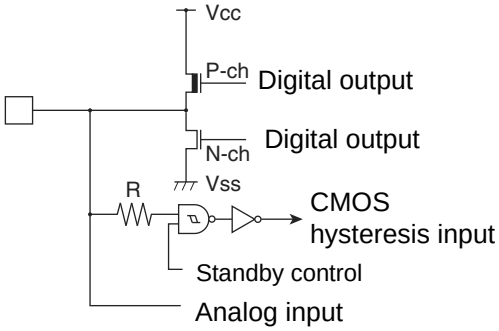
CAN Controller: 1 channel

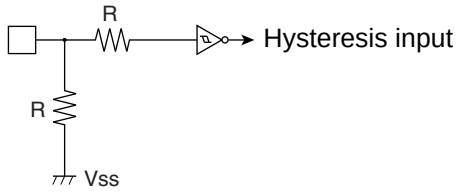
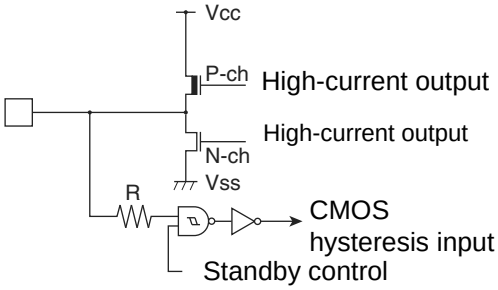
- Compliant with Ver2.0A and Ver2.0B CAN specifications
- 8 built-in message buffers
- Transmission rate of 10 kbps to 1 Mbps (by 16 MHz machine clock)
- CAN wake-up

UART (SCI): 1 channel

- Equipped with full-duplex double buffer
- Clock-asynchronous or clock-synchronous serial transmission is available.

6. I/O Circuit Type

Type	Circuit	Remarks
A		■ High-rate oscillation feedback resistor, approx.1 MΩ ■ Low-rate oscillation feedback resistor, approx.10 MΩ
B		■ Hysteresis input with pull-up resistor. ■ Pull-up resistor, approx.50 kΩ
C		■ Hysteresis input
D		■ CMOS hysteresis input ■ CMOS level output ■ Standby control provided
E		■ CMOS hysteresis input ■ CMOS level output ■ Shared for analog input pin ■ Standby control provided

Type	Circuit	Remarks
F		■ Hysteresis input with pull-down resistor ■ Pull-down resistor, approx. 50 kΩ ■ Flash product is not provided with pull-down resistor.
G		■ CMOS hysteresis input ■ CMOS level output (high-current output) ■ Standby control provided

7. Handling Devices

Do Not Exceed Maximum Rating (preventing “latch up”)

■ On a CMOS IC, latch-up may occur when applying a voltage higher than Vcc or a voltage lower than Vss to input or output pin, which has no middle or high withstand voltage. Latch-up may also occur when a voltage exceeding maximum rating is applied across Vcc pin and Vss pin.

■ Latch-up causes drastic increase of power current, which may lead to destruction of elements by heat. Extreme caution must be taken not to exceed maximum rating.

■ When turning on and off analog power source, take extra care not to apply an analog power voltages (AVcc and AVR) and analog input voltage that are higher than digital power voltage (Vcc).

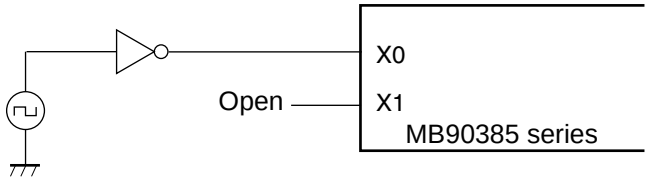
Handling Unused Pins

■ Leaving unused input pins open may cause permanent destruction by malfunction or latch-up. Apply pull-up or pull-down process to the unused pins using resistors of 2 kΩ or higher. Leave unused input/output pins open under output status, or process as input pins if they are under input status.

Using External Clock

■ When using an external clock, drive only X0 pin and leave X1 pin open. An example of using an external clock is shown below.

• Using external clock



Address	Register Abbreviation	Register	Read/ Write	Resource	Initial Value
000038H to 00003FH	(Reserved area) *				
000040H	PPGC0	PPG0 operation mode control register	R/W, W	8/16-bit PPG timer 0/1	0X000XX1B
000041H	PPGC1	PPG1 operation mode control register	R/W, W		0X000001B
000042H	PPG01	PPG0/1 count clock selection register	R/W		000000XXB
000043H	(Reserved area) *				
000044H	PPGC2	PPG2 operation mode control register	R/W, W	8/16-bit PPG timer 2/3	0X000XX1B
000045H	PPGC3	PPG3 operation mode control register	R/W, W		0X000001B
000046H	PPG23	PPG2/3 count clock selection register	R/W		000000XXB
000047H to 00004FH	(Reserved area) *				
000050H	IPCP0	Input capture data register 0	R	16-bit input/output timer	XXXXXXXXB
000051H					XXXXXXXXB
000052H	IPCP1	Input capture data register 1	R		XXXXXXXXB
000053H					XXXXXXXXB
000054H	ICS01	Input capture control status register	R/W		00000000B
000055H	ICS23				00000000B
000056H	TCDT	Timer counter data register	R/W		00000000B
000057H					00000000B
000058H	TCCS	Timer counter control status register	R/W		00000000B
000059H	(Reserved area) *				
00005AH	IPCP2	Input capture data register 2	R	16-bit input/output timer	XXXXXXXXB
00005BH					XXXXXXXXB
00005CH	IPCP3	Input capture data register 3	R		XXXXXXXXB
00005DH					XXXXXXXXB
00005EH to 000065H	(Reserved area) *				
000066H	TMCSR0	Timer control status register	R/W	16-bit reload timer 0	00000000B
000067H			R/W		XXXX0000B
000068H	TMCSR1		R/W	16-bit reload timer 1	00000000B
000069H			R/W		XXXX0000B
00006AH to 00006EH	(Reserved area) *				
00006FH	ROMM	ROM mirroring function selection register	W	ROM mirroring function selection module	XXXXXXX1B
000070H to 00007FH	(Reserved area) *				
000080H	BVALR	Message buffer enabling register	R/W	CAN controller	00000000B
000081H	(Reserved area) *				
000082H	TREQR	Send request register	R/W	CAN controller	00000000B

Interrupt Source	EI²OS Readiness	Interrupt Vector			Interrupt Control Register		Priority*3
		Number		Address	ICR	Address	
UART1 reception completed	◎	#37	25H	FFFF68H	ICR13	0000BDH*1	High
UART1 transmission completed	Δ	#38	26H	FFFF64H			↑
Reserved	×	#39	27H	FFFF60H	ICR14	0000BEH*1	
Reserved	×	#40	28H	FFFF5CH			
Flash memory	×	#41	29H	FFFF58H	ICR15	0000BFH*1	↓
Delay interrupt generation module	×	#42	2AH	FFFF54H			Low

○ : Available

× : Unavailable

◎ : Available EI²OS function is provided.

Δ: Available when a cause of interrupt sharing a same ICR is not used.

*1:

- ❒ Peripheral functions sharing an ICR register have the same interrupt level.
- ❒ If peripheral functions share an ICR register, only one function is available when using expanded intelligent I/O service.
- ❒ If peripheral functions share an ICR register, a function using expanded intelligent I/O service does not allow interrupt by another function.

*2: Input capture 1 corresponds to EI²OS, however, PPG does not. When using EI²OS by input capture 1, interrupt should be disabled for PPG.

*3:Priority when two or more interrupts of a same level occur simultaneously.

12. Peripheral Resources

12.1 I/O Ports

The I/O ports are used as general-purpose input/output ports (parallel I/O ports). The MB60385 series model is provided with 5 ports (34 inputs). The ports function as input/output pins for peripheral functions also.

I/O Port Functions

An I/O port, using port data resister (PDR), outputs the output data to I/O pin and input a signal input to I/O port. The port direction register (DDR) specifies direction of input/output of I/O pins on a bit-by-bit basis.

The following summarizes functions of the ports and sharing peripheral functions:

■ Port 1: General-purpose input/output port, used also for PPG timer output and input capture inputs.

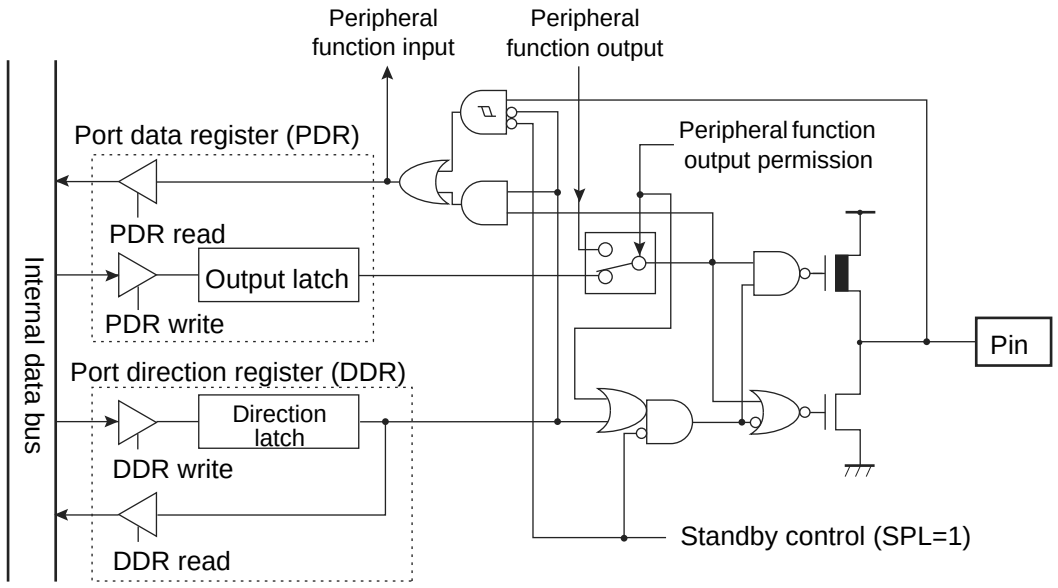
■ Port 2: General-purpose input/output port, used also for reload timer input/output and external interrupt input.

■ Port 3: General-purpose input/output port, used also for A/D converter activation trigger pin.

■ Port 4: General-purpose input/output port, used also for UART input/output and CAN controller send/receive pin.

■ Port 5: General-purpose input/output port, used also analog input pin.

Port 3 Pins Block Diagram (general-purpose input/output port)



Standby control: Control among Stop mode (SPL=1), Time-base timer mode (SPL=1), and watch mode (SPL=1).

Port 3 Registers

■ Port 3 registers include port 3 data register (PDR3) and port 3 direction register (DDR3).

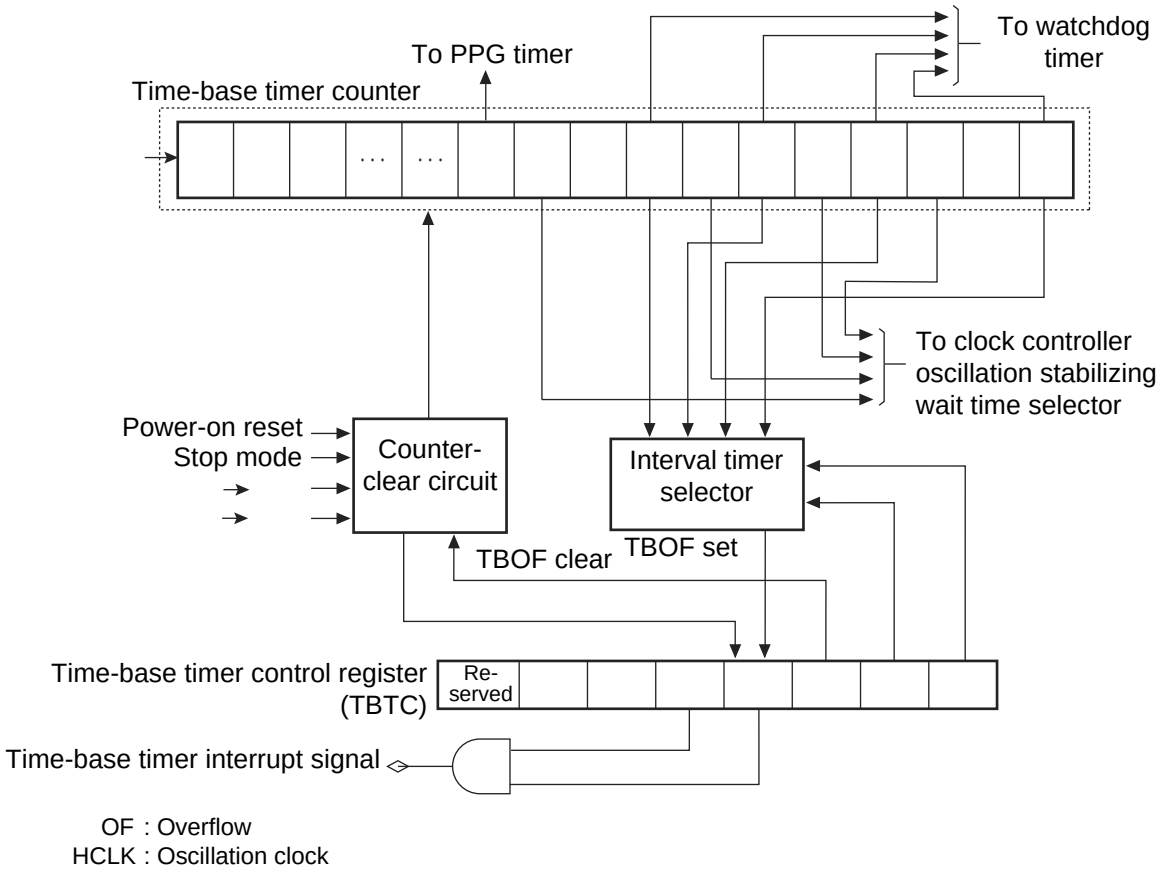
■ The bits configuring the register correspond to port 3 pins on a one-to-one basis.

Relation between Port 3 Registers and Pins

Port Name	Bits of Register and Corresponding Pins								
Port 3	PDR3, DDR3	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	Corresponding pins	P37	P36*	P35*	–	P33	P32	P31	P30

*: P35 and P36 do not exist on MB90387and MB90F387.

Time-base Timer Block Diagram



OF : Overflow
HCLK : Oscillation clock

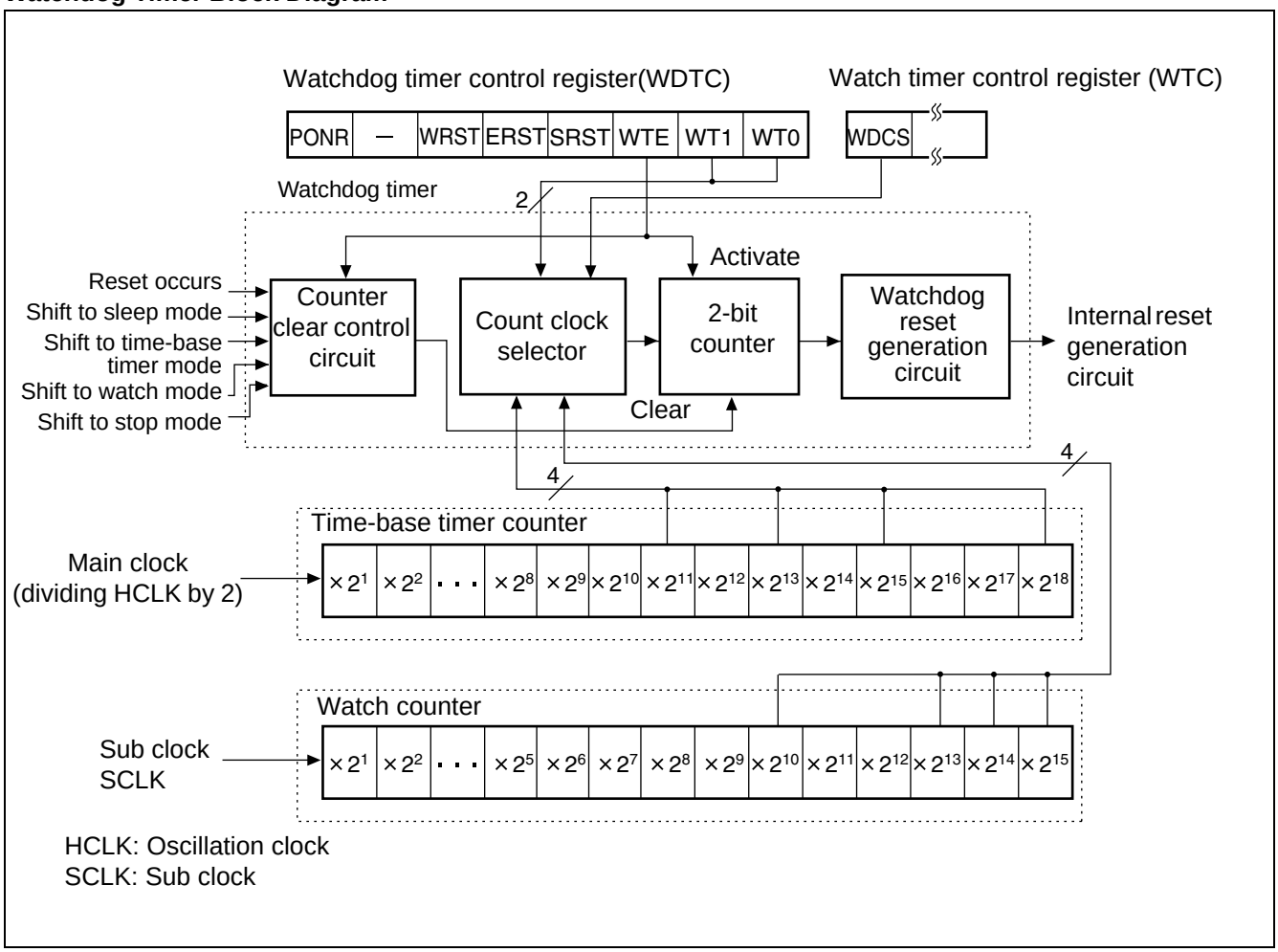
*1: Switch machine clock from main clock to PLL clock.

*2: Switch machine clock from sub clock to main clock.

Actual interrupt request number of time-base timer is as follows:

Interrupt request number: #16 (10_H)

Watchdog Timer Block Diagram



12.4 16-bit Input/Output Timer

The 16-bit input/output timer is a compound module composed of 16-bit free-run timer, (1 unit) and input capture (2 units, 4 input pins). The timer, using the 16-bit free-run timer as a basis, enables measurement of clock cycle of an input signal and its pulse width.

Configuration of 16-bit Input/Output Timer

The 16-bit input/output timer is composed of the following modules:

- 16-bit free-run timer (1 unit)
- Input capture (2 units, 2 input pins per unit)

Functions of 16-bit Input/Output Timer

Functions of 16-bit Free-run Timer

The 16-bit free-run timer is composed of 16-bit up counter, timer counter control status register, and prescaler. The 16-bit up counter increments in synchronization with dividing ratio of machine clock.

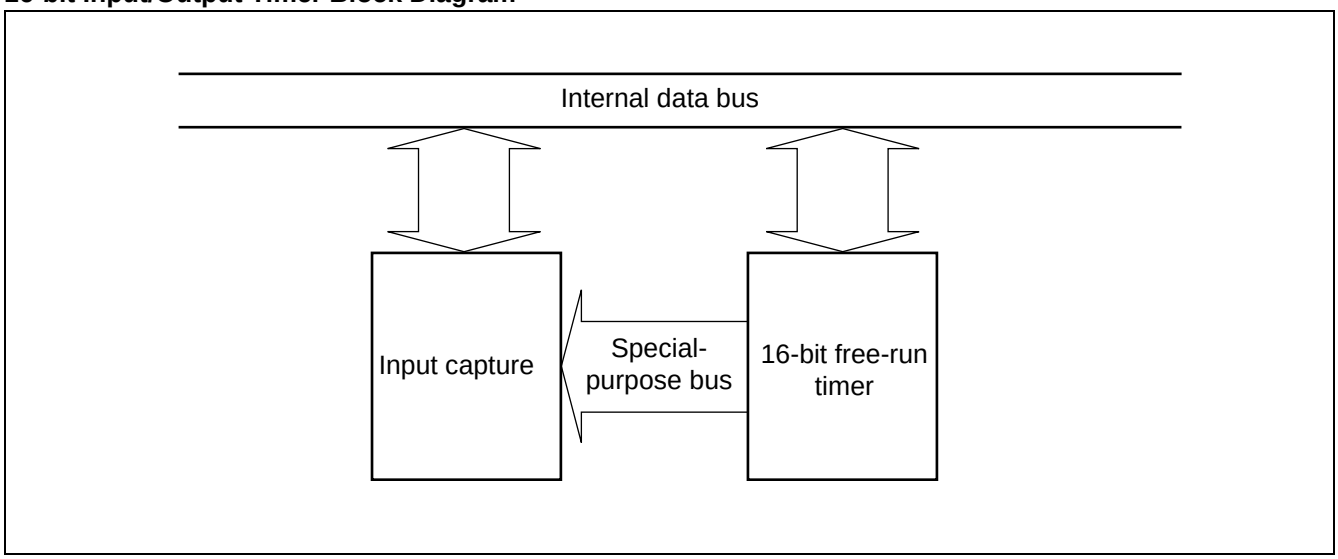
- Count clock is set among four types of machine clock dividing rates.
- Generation of interrupt is allowed by counter value overflow.
- Activation of expanded intelligent I/O service (EI^{2}OS) is allowed by interrupt generation.
- Counter value of 16-bit free-run timer is cleared to "0000$_H$" by either resetting or software-clearing with timer count clear bit (TCCS: CLR).
- Counter value of 16-bit free-run timer is output to input capture, which is available as base time for capture operation.

Functions of Input Capture

The input capture, upon detecting an edge of a signal input to the input pin from external device, stores a counter value of 16-bit free-run timer at the time of detection into the input capture data register. The function includes the input capture data registers corresponding to four input pins, input capture control status register, and edge detection circuit.

- Rising edge, falling edge, and both edges are selectable for detection.
- Generating interrupt on CPU is allowed by detecting an edge of input signal.
- Expanded intelligent I/O service (EI^{2}OS) is activated by interrupt generation.
- The four input capture input pins and input capture data registers allows monitoring of a maximum of four events.

16-bit Input/Output Timer Block Diagram



12.7 8/16-bit PPG Timer Outline

The 8/16-bit PPG timer is a 2-channel reload timer module (PPG0 and PPG1) that allows outputting pulses of arbitrary cycle and duty cycle. Combination of the two channels allows selection among the following operations:

- 8-bit PPG output 2-channel independent operation mode
- 16-bit PPG output operation mode
- 8-bit and 8-bit PPG output operation mode

MB90385 series device has two 8/16-bit built-in PPG timers. This section describes functions of PPG0/1. PPG2/3 have the same functions as those of PPG0/1.

Functions of 8/16-bit PPG Timer

The 8/16-bit PPG timer is composed of four 8-bit reload register (PRLH0/PRLL0, PRLH1/PRLL1) and two PPG down counters (PCNT0, PCNT1).

- Widths of “H” and “L” in output pulse are specifiable independently. Cycle and duty factor of output pulse is specifiable arbitrarily.
- Count clock is selectable among 6 internal clocks.
- The timer is usable as an interval timer, by generating interrupt requests for each interval.
- The time is usable as a D/A converter, with an external circuit.

12.9 DTP/External Interrupt and CAN Wakeup Outline

DTP/external interrupt transfers an interrupt request generated by an external peripheral device or a data transmission request to CPU, generating external interrupt request and activating expanded intelligent I/O service. Input RX of CAN controller is used as external interrupt input.

DTP/External Interrupt and CAN Wakeup Function

An interrupt request input from external peripheral device to external input pins (INT7 to INT4) and RX pin, just as interrupt request of peripheral device, generates an interrupt request. The interrupt request generates an external interrupt and activates expanded intelligent I/O service (EI^2OS).

If the expanded intelligent I/O service (EI^2OS) has been disabled by interrupt control register (ICR: ISE=0), external interrupt function is enabled and branches to interrupt processing.

If the EI^2OS has been enabled, (ICR: ISE=1), DTP function is enabled and automatic data transmission is performed by EI^2OS. After performing specified number of data transmission processes, the process branches to interrupt processing.

Table 12-2. DTP/External Interrupt and CAN Wakeup Outline

	External Interrupt	DTP Function
Input pin	5 pins (RX, and INT4 to INT7)	
Interrupt cause	Specify for each pin with detection level setting register (ELVR).	
	Input of “H” level/“L” level/rising edge/falling edge.	Input of “H” level/ “L” level
Interrupt number	#15 ($0F_H$), #24 (18_H), #27 ($1B_H$)	
Interrupt control	Enabling or disabling output of interrupt request, using DTP/external interrupt permission register (ENIR).	
Interrupt flag	Retaining interrupt cause with DTP/external interrupt cause register (EIRR).	
Process selection	Disable EI^2OS (ICR: ISE=0)	Enable EI^2OS (ICR: ISE=1)
Process	Branch to external interrupt process	After automatic data transmission by EI^2OS for specified number of times, branch to interrupt process.

12.11 UART Outline

UART is a general-purpose serial data communication interface for synchronous and asynchronous communication using external devices.

- Provided with bi-directional communication function for both clock-synchronous and clock-asynchronous modes.
- Provided with master/slave communication function (multi-processor mode). (Only master side is available.)
- Interrupt request is generated upon completion of reception, completion of transmission and detection of reception error.
- Ready for expanded intelligent service, EI^{2}OS.

Table 12-3. UART Functions

	Description
Data buffer	Full-duplex double buffer
Transmission mode	Clock synchronous (No start/stop bit, no parity bit) Clock asynchronous (start-stop synchronous)
Baud rate	Built-in special-purpose baud-rate generator. Setting is selectable among 8 values. Input of external values is allowed. Use of clock from external timer (16-bit reload timer 0) is allowed.
Data length	7 bits (only asynchronous normal mode) 8 bits
Signaling system	Non Return to Zero (NRZ) system
Reception error detection	Framing error Overrun error Parity error (not detectable in operation mode 1 (multi-processor mode))
Interrupt request	Receive interrupt (reception completed, reception error detected) Transmission interrupt (transmission completed) Ready for expanded intelligent I/O service (EI^{2}OS) in both transmission and reception
Master/slave communication function (asynchronous, multi-processor mode)	Communication between 1 (master) and n (slaves) are available (usable as master only).

Note: Start/stop bit is not added upon clock-synchronous transmission. Data only is transmitted.

Table 12-4. UART Operation Modes

Operation Mode		Data Length		Synchronization	Stop Bit Length
		With Parity	Without Parity		
0	Asynchronous mode (normal mode)	7-bit or 8-bit		Asynchronous	1- bit or 2-bit *2
1	Multi processor mode	8+1*1	–	Asynchronous	
2	Synchronous mode	8	–	Synchronous	No

–: Disallowed

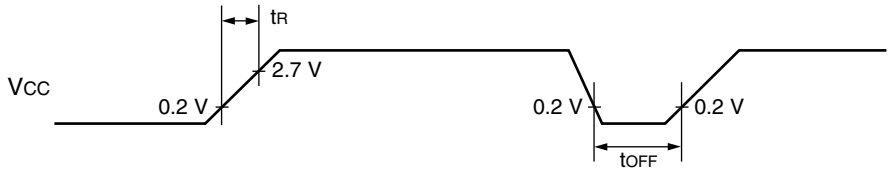
1: “+1” is an address/data selection bit used for communication control (bit 11 of SCR1 register: A/D).

2: Only 1 bit is detected as a stop bit on data reception.

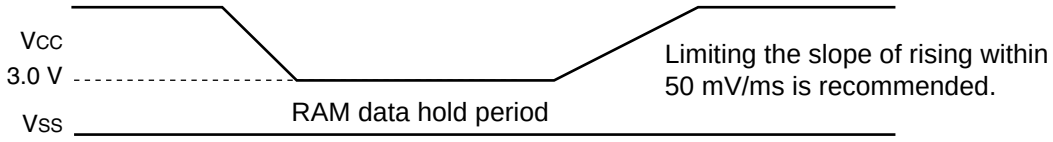
13.4.3 Power-on Reset

(V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Power supply rise time	t_R	V_{CC}	–	0.05	30	ms	
Power supply shutdown time	t_{OFF}	V_{CC}		1	–	ms	Waiting time until power-on



Sudden change of power supply voltage may activate the power-on reset function. When changing power supply voltages during operation, raise the power smoothly by suppressing variation of voltages as shown below. When raising the power, do not use PLL clock. However, if voltage drop is 1V/s or less, use of PLL clock is allowed during operation.



13.4.4 UART Timing

(V_{CC} = 4.5 V to 5.5 V, V_{SS} = 0.0 V, T_A = −40 °C to +105 °C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK1	Internal shift clock mode output pin is: CL = 80 pF+1TTL.	4 t_{CP} *	–	ns	
SCK ↓ → SOT delay time	t_{SLOV}	SCK1, SOT1		−80	+80	ns	
Valid SIN → SCK ↑	t_{IVSH}	SCK1, SIN1		100	–	ns	
SCK ↑ → valid SIN hold time	t_{SHIX}	SCK1, SIN1		60	–	ns	
Serial clock “H” pulse width	t_{SHSL}	SCK1	External shift clock mode output pin is: CL = 80 pF+1TTL.	2 t_{CP} *	–	ns	
Serial clock “L” pulse width	t_{SLSH}	SCK1		2 t_{CP} *	–	ns	
SCK ↓ → SOT delay time	t_{SLOV}	SCK1, SOT1		–	150	ns	
Valid SIN → SCK ↑	t_{IVSH}	SCK1, SIN1		60	–	ns	
SCK ↑ → valid SIN hold time	t_{SHIX}	SCK1, SIN1		60	–	ns	

*: Refer to Clock Timing ratings for t_{CP} (internal operation clock cycle time).

Notes:

■ AC Characteristics in CLK synchronous mode.

■ C_L is a load capacitance value on pins for testing.

13.5 A/D Converter

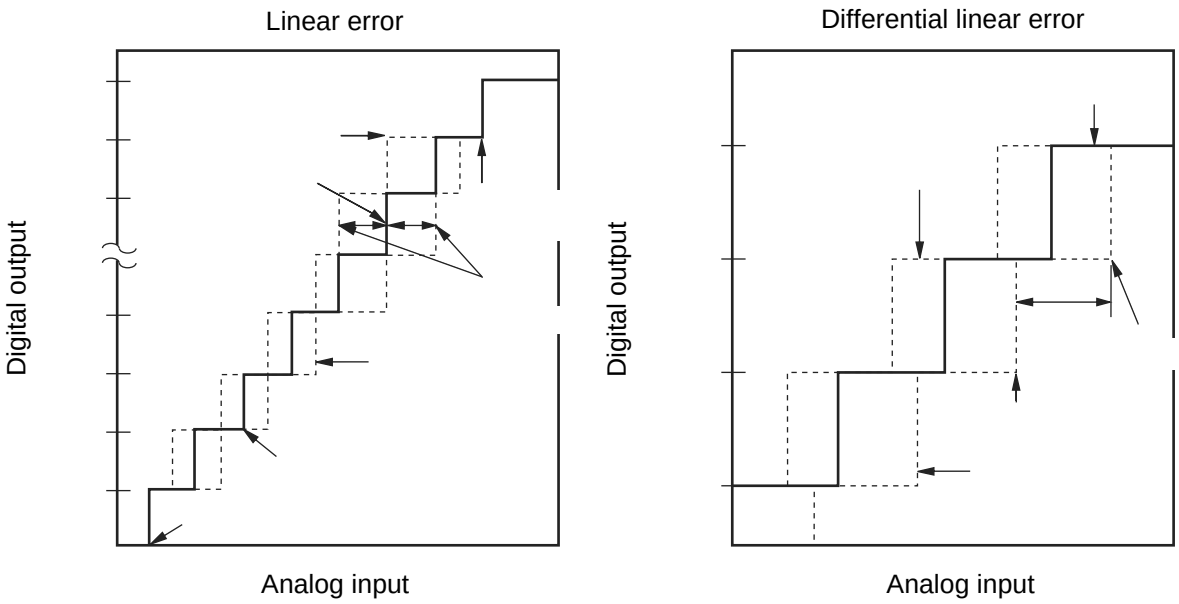
(V_{CC} = AV_{CC} = 4.0 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, 3.0 V ≤ AVR − AV_{SS}, T_A = −40 °C to +105 °C)

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	–	–	–	–	10	bit	
Total error	–	–	–	–	± 3.0	LSB	
Nonlinear error	–	–	–	–	± 2.5	LSB	
Differential linear error	–	–	–	–	± 1.9	LSB	
Zero transition voltage	V_{OT}	AN0 to AN7	AV_{SS} − 1.5 LSB	AV_{SS} + 0.5 LSB	AV_{SS} + 2.5 LSB	V	1 LSB = (AVR − AV_{SS}) / 1024
Full-scale transition voltage	V_{FST}	AN0 to AN7	AVR − 3.5 LSB	AVR − 1.5 LSB	AVR + 0.5 LSB	V	
Compare time	–	–	66 t_{CP} *1	–	–	ns	With 16 MHz machine clock 5.5 V ≥ AV_{CC} ≥ 4.5 V
			88 t_{CP} *1	–	–	ns	With 16 MHz machine clock 4.5 V > AV_{CC} ≥ 4.0 V
Sampling time	–	–	32 t_{CP} *1	–	–	ns	With 16 MHz machine clock 5.5 V ≥ AV_{CC} ≥ 4.5 V
			128 t_{CP} *1	–	–	ns	With 16 MHz machine clock 4.5 V > AV_{CC} ≥ 4.0 V
Analog port input current	I_{AIN}	AN0 to AN7	–	–	10	µA	
Analog input voltage	V_{AIN}	AN0 to AN7	AV_{SS}	–	AVR	V	
Reference voltage	–	AVR	AV_{SS} + 2.7	–	AV_{CC}	V	
Power supply current	I_A	AV_{CC}	–	3.5	7.5	mA	
	I_{AH}	AV_{CC}	–	–	5	µA	*2
Reference voltage supplying current	I_R	AVR	–	165	250	µA	
	I_{RH}	AVR	–	–	5	µA	*2
Variation among channels	–	AN0 to AN7	–	–	4	LSB	

*1: Refer to Clock Timing on AC Characteristics.

*2: If A/D converter is not operating, a current when CPU is stopped is applicable (Vcc=AVcc=AVR=5.0 V).

(Continued)



$$\text{Linear error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + V_{OT}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$\text{Differential linear error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\text{LSB}\ [\text{LSB}]$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ [\text{V}]$$

V_{OT}: Voltage at which digital output transits from “000_H” to “001_H.”
V_{FST}: Voltage at which digital output transits from “$3FE_H$” to “$3FF_H$.”

13.7 Notes on A/D Converter Section

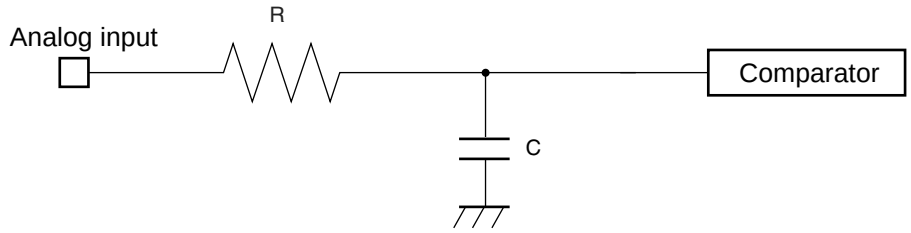
Use the device with external circuits of the following output impedance for analog inputs:

Recommended output impedance of external circuits are: Approx. 3.9 kΩ or lower (4.5 V ≤ AVcc ≤ 5.5 V) (sampling period=2.00 μs at 16 MHz machine clock), Approx. 11 kΩ or lower (4.0 V ≤ AVcc < 4.5 V) (sampling period=8.0 μs at 16 MHz machine clock).

If an external capacitor is used, in consideration of the effect by tap capacitance caused by external capacitors and on-chip capacitors, capacitance of the external one is recommended to be several thousand times as high as internal capacitor.

If output impedance of an external circuit is too high, a sampling period for an analog voltage may be insufficient.

- Analog input circuit model



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4.5 V ≤ AV_{CC} ≤ 5.5 V R ≅ 2.35 kΩ, C ≅ 36.4 pF

4.0 V ≤ AV_{CC} < 4.5 V R ≅ 16.4 kΩ, C ≅ 36.4 pF

Note: Use the values in the figure only as a guideline.

About errors

As [AVR-AVss] become smaller, values of relative errors grow larger.

13.8 Flash Memory Program/Erase Characteristics

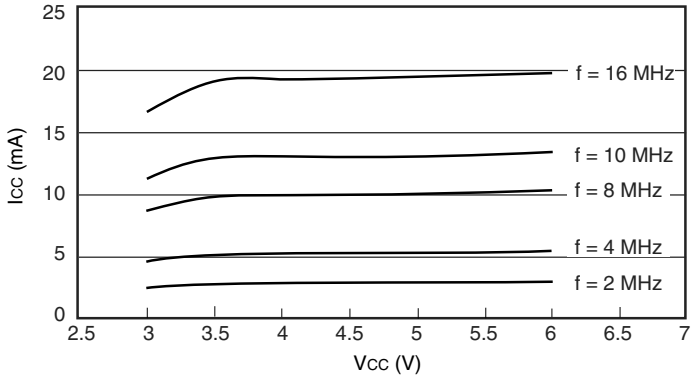
Parameter	Conditions	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	T_A = + 25 °C V_{CC} = 5.0 V	–	1	15	s	Excludes 00H programming prior to erasure
Chip erase time		–	4	–	s	Excludes 00H programming prior to erasure
Word (16-bit width) programming time		–	16	3,600	μs	Except for the over head time of the system
Program/Erase cycle	–	10,000	–	–	cycle	
Flash Data Retention Time	Average T_A = + 85 °C	20	–	–	Year	*

*: This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at + 85 °C).

MB90387

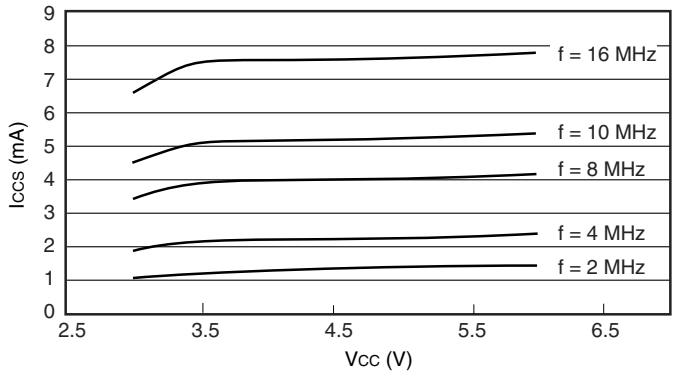
I_{CC} – V_{CC}

T_A = +25 °C, In external clock operation
f = Internal operating frequency



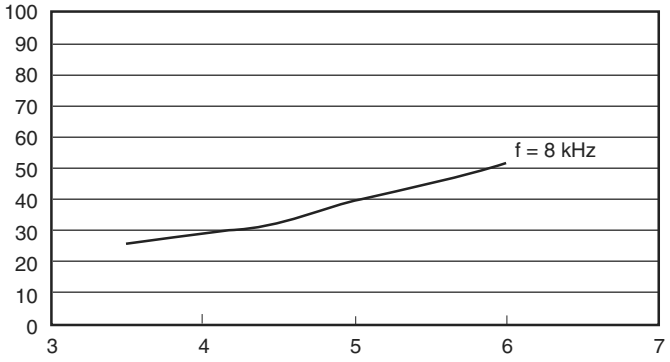
I_{CCS} – V_{CC}

T_A = +25 °C, In external clock operation
f = Internal operating frequency



I_{CCL} – V_{CC}

T_A = +25 °C, In external clock operation
f = Internal operating frequency



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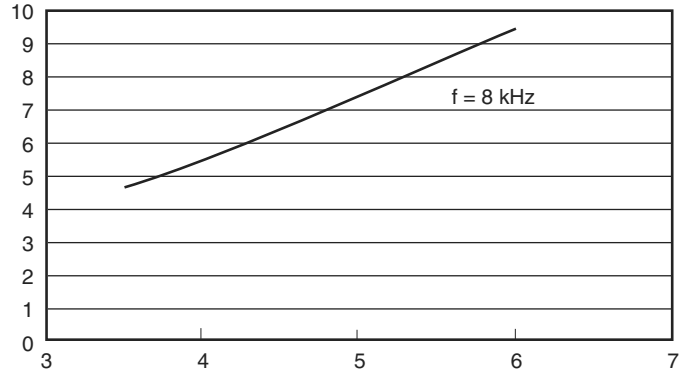
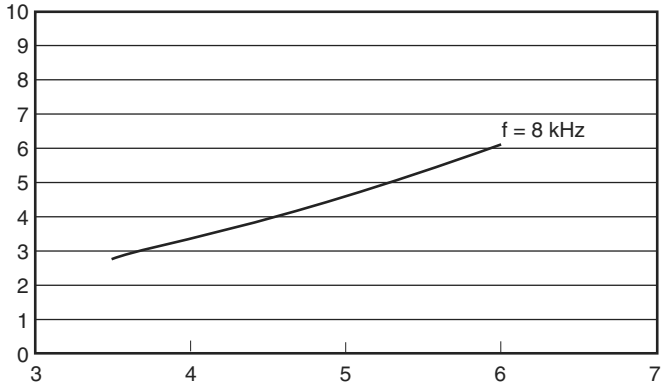
I_{CCLS} – V_{CC}

T_A = +25 °C, In external clock operation
f = Internal operating frequency



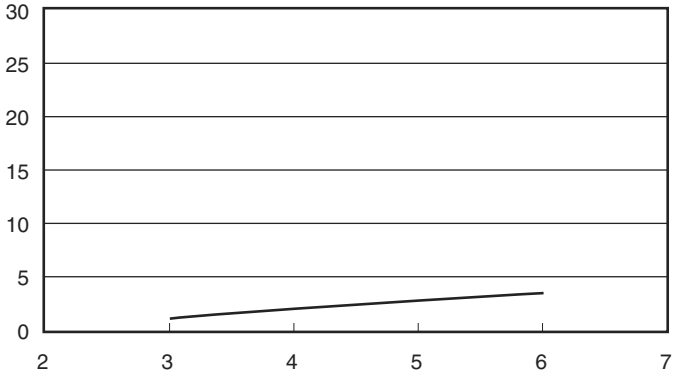
I_{CCT} – V_{CC}

T_A = +25 °C, In external clock operation
f = Internal operating frequency



I_{CCH} – V_{CC}

Stopping, T_A = +25 °C



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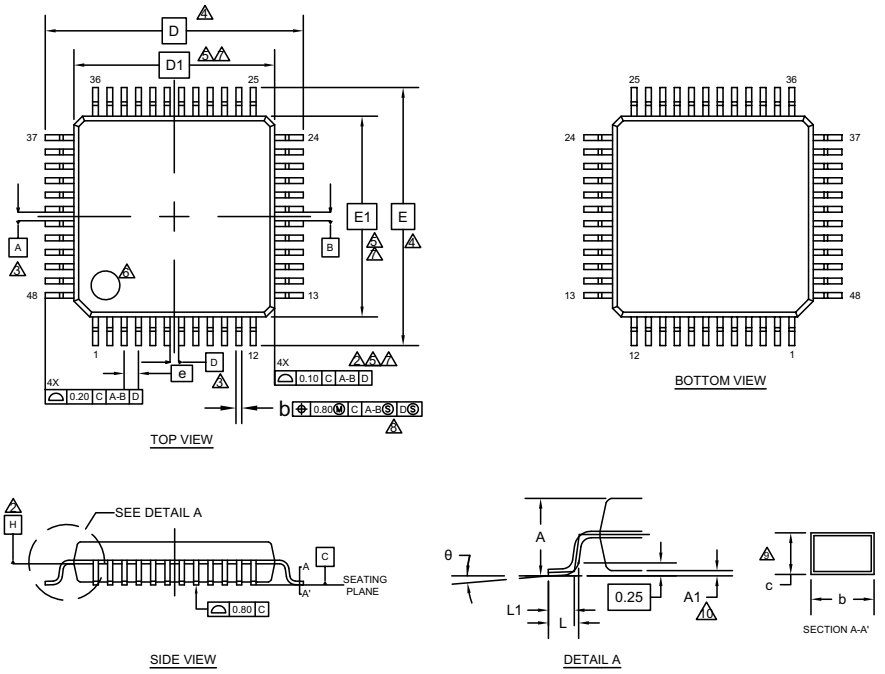
16. Package Dimension



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.00	—	0.20
b	0.15	—	0.27
c	0.09	—	0.20
D	9.00 BSC		
D1	7.00 BSC		
e	0.50 BSC		
E	9.00 BSC		
E1	7.00 BSC		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
θ	0°	—	8°

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-13731 **

PACKAGE OUTLINE, 48 LEAD LQFP
7.0X7.0X1.7 MM LQA048 REV**