What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details

Product Status	Obsolete
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, SCI, UART/USART
Peripherals	POR, WDT
Number of I/O	36
Program Memory Size	64KB (64K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90387spmt-gs-257e1

16-bit Microcontrollers
F^{2}MC-16LX MB90385 Series

MB90385 series devices are general-purpose high-performance 16-bit micro controllers designed for process control of consumer products, which require high-speed real-time processing. The devices of this series have the built-in full-CAN interface.

The system, inheriting the architecture of F^{2}MC family, employs additional instruction ready for high-level languages, expanded addressing mode, enhanced multiply-divide instructions, and enriched bit-processing instructions. Furthermore, employment of 32-bit accumulator achieves processing of long-word data (32 bits).

The peripheral resources of MB90385 series include the following:

8/10-bit A/D converter, UART (SCI), 8/16-bit PPG timer, 16-bit input-output timer (16-bit free-run timer, input capture 0, 1, 2, 3 (ICU)), and CAN controller.

Features

Clock

- Built-in PLL clock frequency multiplication circuit

- Selection of machine clocks (PLL clocks) is allowed among frequency division by two on oscillation clock, and multiplication of 1 to 4 times of oscillation clock (for 4-MHz oscillation clock, 4 MHz to 16 MHz).

- Operation by sub-clock (8.192 kHz) is allowed. (MB90387, MB90F387)

- Minimum execution time of instruction: 62.5 ns (when operating with 4-MHz oscillation clock, and 4-time multiplied PLL clock).

16 Mbyte CPU memory Space

- 24-bit internal addressing

Instruction System Best Suited to Controller

- Wide choice of data types (bit, byte, word, and long word)

- Wide choice of addressing modes (23 types)

- Enhanced multiply-divide instructions and RETI instructions

- Enhanced high-precision computing with 32-bit accumulator

Instruction System Compatible with High-level Language (C language) and Multitask

- Employing system stack pointer

- Enhanced various pointer indirect instructions

- Barrel shift instructions

Increased Processing Speed

- 4-byte instruction queue

Powerful Interrupt Function with 8 Levels and 34 Factors

Automatic Data Transfer Function Independent of CPU

- Expanded intelligent I/O service function (EI^2 OS): Maximum of 16 channels

Low Power Consumption (standby) Mode

- Sleep mode (a mode that halts CPU operating clock)

- Time-base timer mode (a mode that operates oscillation clock, sub clock, time-base timer and watch timer only)

- Watch mode (a mode that operates sub clock and watch timer only)

- Stop mode (a mode that stops oscillation clock and sub clock)

- CPU blocking operation mode

Process

- CMOS technology

I/O Port

- General-purpose input/output port (CMOS output):

  MB90387, MB90F387: 34 ports (including 4 high-current output ports)
  MB90387S, MB90F387S: 36 ports (including 4 high-current output ports)

Timer

- Time-base timer, watch timer, watchdog timer: 1 channel

- 8/16-bit PPG timer: 8-bit x 4 channels, or 16-bit x 2 channels

- 16-bit reload timer: 2 channels

- 16-bit input/output timer
  - 16-bit free run timer: 1 channel
  - 16-bit input capture: (ICU): 4 channels

  Interrupt request is issued upon latching a count value of 16-bit free run timer by detection of an edge on pin input.
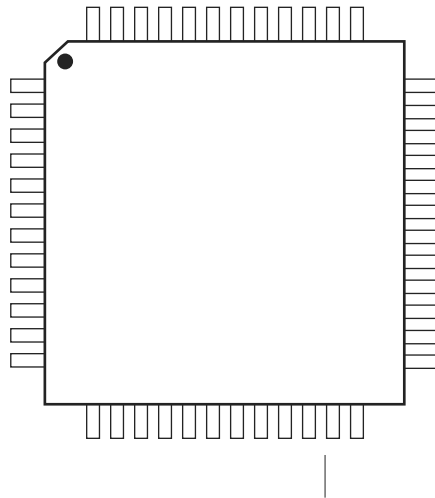
CAN Controller: 1 channel

- Compliant with Ver2.0A and Ver2.0B CAN specifications

- 8 built-in message buffers

- Transmission rate of 10 kbps to 1 Mbps (by 16 MHz machine clock)

- CAN wake-up

UART (SCI): 1 channel

- Equipped with full-duplex double buffer

- Clock-asynchronous or clock-synchronous serial transmission is available.
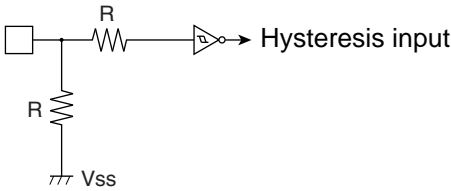
4. Pin Assignment

(Top View)
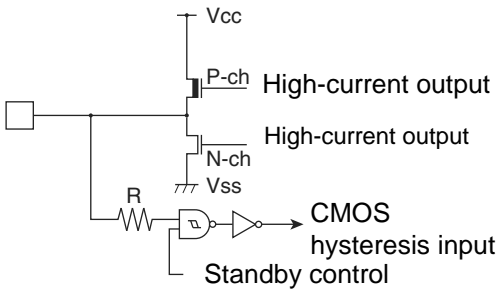
(LQA048)

*: MB90387, MB90F387   : X1A, X0A
   MB90387S, MB90F387S: P36, P35

6. I/O Circuit Type

Type	Circuit	Remarks
A		■ High-rate oscillation feedback resistor, approx.1 MΩ ■ Low-rate oscillation feedback resistor, approx.10 MΩ
B		■ Hysteresis input with pull-up resistor. ■ Pull-up resistor, approx.50 kΩ
C		■ Hysteresis input
D		■ CMOS hysteresis input ■ CMOS level output ■ Standby control provided
E		■ CMOS hysteresis input ■ CMOS level output ■ Shared for analog input pin ■ Standby control provided

Type	Circuit	Remarks
F		■ Hysteresis input with pull-down resistor ■ Pull-down resistor, approx. 50 kΩ ■ Flash product is not provided with pull-down resistor.
G		■ CMOS hysteresis input ■ CMOS level output (high-current output) ■ Standby control provided

7. Handling Devices

Do Not Exceed Maximum Rating (preventing "latch up")

■ On a CMOS IC, latch-up may occur when applying a voltage higher than Vcc or a voltage lower than Vss to input or output pin, which has no middle or high withstand voltage. Latch-up may also occur when a voltage exceeding maximum rating is applied across Vcc pin and Vss pin.

■ Latch-up causes drastic increase of power current, which may lead to destruction of elements by heat. Extreme caution must be taken not to exceed maximum rating.

■ When turning on and off analog power source, take extra care not to apply an analog power voltages (AVcc and AVR) and analog input voltage that are higher than digital power voltage (Vcc).

Handling Unused Pins

■ Leaving unused input pins open may cause permanent destruction by malfunction or latch-up. Apply pull-up or pull-down process to the unused pins using resistors of 2 kΩ or higher. Leave unused input/output pins open under output status, or process as input pins if they are under input status.

Using External Clock

■ When using an external clock, drive only X0 pin and leave X1 pin open. An example of using an external clock is shown below.

• Using external clock
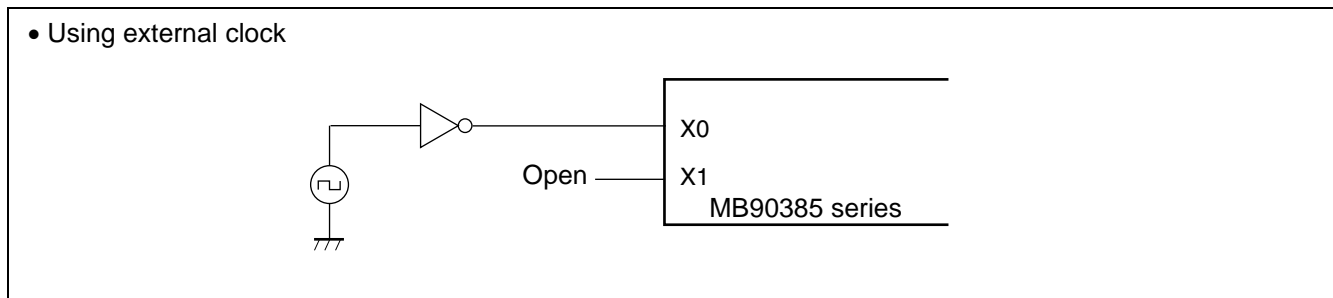
Notes When Using No Sub Clock

■ If an oscillator is not connected to X0A and X1A pin, apply pull-down resistor to X0A pin and leave X1A pin open.

About Power Supply Pins

■ If two or more Vcc and Vss pins exist, the pins that should be at the same potential are connected to each other inside the device. For reducing unwanted emissions and preventing malfunction of strobe signals caused by increase of ground level, however, be sure to connect the Vcc and Vss pins to the power source and the ground externally.

■ Pay attention to connect a power supply to Vcc and Vss of MB90385 series device in a lowest-possible impedance.

■ Near pins of MB90385 series device, connecting a bypass capacitor is recommended at 0.1 μF across Vcc pin and Vss pin.

Crystal Oscillator Circuit

■ Noises around X0 and X1 pins cause malfunctions on a MB90385 series device. Design a print circuit so that X0 and X1 pins, an crystal oscillator (or a ceramic oscillator), and bypass capacitor to the ground become as close as possible to each other. Furthermore, avoid wires to X0 and X1 pins crossing each other as much as possible.

■ Print circuit designing that surrounds X0 and X1 pins with grounding wires, which ensures stable operation, is strongly recommended.

Caution on Operations during PLL Clock Mode

■ If the PLL clock mode is selected, the microcontroller attempt to be working with the self-oscillating circuit even when there is no external oscillator or external clock input is stopped. Performance of this operation, however, cannot be guaranteed.

Sequence of Turning on Power of A/D Converter and Applying Analog Input

■ Be sure to turn on digital power (Vcc) before applying signals to the A/D converter and applying analog input signals (AN0 to AN7 pins).

■ Be sure to turn off the power of A/D converter and analog input before turning off the digital power source.

■ Be sure not to apply AVR exceeding AVcc when turning on and off. (No problems occur if analog and digital power is turned on and off simultaneously.)

Handling Pins When A/D Converter is Not Used

■ If the A/D converter is not used, connect the pins under the following conditions: "AVcc=AVR=Vcc," and "AVss=Vss"

Note on Turning on Power

■ For preventing malfunctions on built-in step-down circuit, maintain a minimum of 50 μs of voltage rising time (between 0.2 V and 2.7V) when turning on the power.

Stabilization of Supply Voltage

■ A sudden change in the supply voltage may cause the device to malfunction even within the specified Vcc supply voltage operating range. Therefore, the Vcc supply voltage should be stabilized.
For reference, the supply voltage should be controlled so that Vcc ripple variations (peak-to-peak values) at commercial frequencies (50 Hz / 60 Hz) fall below 10% of the standard Vcc supply voltage and the coefficient of fluctuation does not exceed 0.1 V/ms at instantaneous power switching.
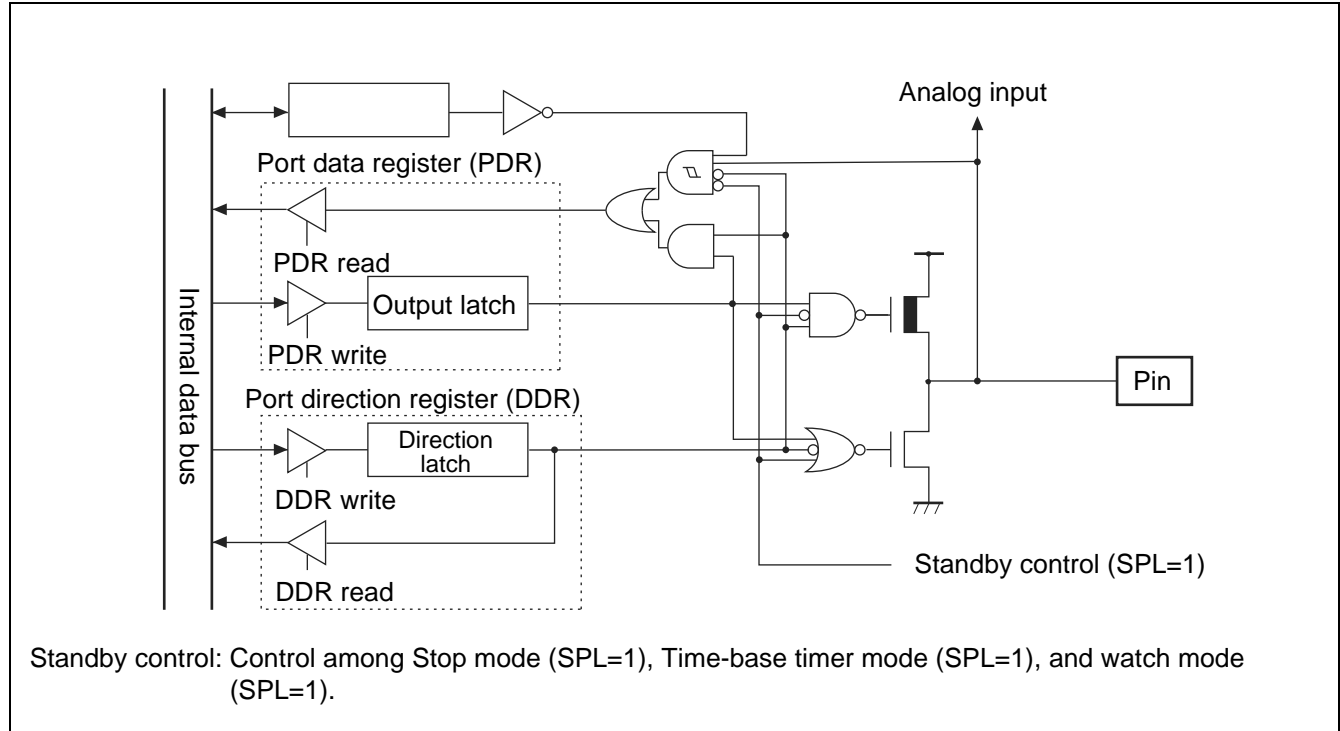
10. I/O Map

Address	Register Abbreviation	Register	Read/ Write	Resource	Initial Value
000000H		(Reserved area) *			
000001H	PDR1	Port 1 data register	R/W	Port 1	XXXXXXXXB
000002H	PDR2	Port 2 data register	R/W	Port 2	XXXXXXXXB
000003H	PDR3	Port 3 data register	R/W	Port 3	XXXXXXXXB
000004H	PDR4	Port 4 data register	R/W	Port 4	XXXXXXXXB
000005H	PDR5	Port 5 data register	R/W	Port 5	XXXXXXXXB
000006H to 000010H		(Reserved area) *			
000011H	DDR1	Port 1 direction data register	R/W	Port 1	00000000B
000012H	DDR2	Port 2 direction data register	R/W	Port 2	00000000B
000013H	DDR3	Port 3 direction data register	R/W	Port 3	000X0000B
000014H	DDR4	Port 4 direction data register	R/W	Port 4	XXX00000B
000015H	DDR5	Port 5 direction data register	R/W	Port 5	00000000B
000016H to 00001AH		(Reserved area) *			
00001BH	ADER	Analog input permission register	R/W	8/10-bit A/D converter	11111111B
00001CH to 000025H		(Reserved area) *			
000026H	SMR1	Serial mode register 1	R/W	UART1	00000000B
000027H	SCR1	Serial control register 1	R/W, W		00000100B
000028H	SIDR1/ SODR1	Serial input data register 1/ Serial output data register 1	R, W		XXXXXXXXB
000029H	SSR1	Serial status data register 1	R, R/W		00001000B
00002AH		(Reserved area) *			
00002BH	CDCR1	Communication prescaler control register 1	R/W	UART1	0XXX0000B
00002CH to 00002FH		(Reserved area) *			
000030H	ENIR	DTP/External interrupt permission register	R/W	DTP/External interrupt	00000000B
000031H	EIRR	DTP/External interrupt permission register	R/W		XXXXXXXXB
000032H	ELVR	Detection level setting register	R/W		00000000B
000033H			R/W		00000000B
000034H	ADCS	A/D control status register	R/W	8/10-bit A/D converter	00000000B
000035H			R/W, W		00000000B
000036H	ADCR	A/D data register	W, R		XXXXXXXXB
000037H			R		00101XXXB

Address	Register Abbreviation	Register	Read/Write	Resource	Initial Value
0000B0$_H$	ICR00	Interrupt control register 00	R/W	Interrupt controller	00000111$_B$
0000B1$_H$	ICR01	Interrupt control register 01			00000111$_B$
0000B2$_H$	ICR02	Interrupt control register 02			00000111$_B$
0000B3$_H$	ICR03	Interrupt control register 03			00000111$_B$
0000B4$_H$	ICR04	Interrupt control register 04			00000111$_B$
0000B5$_H$	ICR05	Interrupt control register 05			00000111$_B$
0000B6$_H$	ICR06	Interrupt control register 06			00000111$_B$
0000B7$_H$	ICR07	Interrupt control register 07			00000111$_B$
0000B8$_H$	ICR08	Interrupt control register 08			00000111$_B$
0000B9$_H$	ICR09	Interrupt control register 09			00000111$_B$
0000BA$_H$	ICR10	Interrupt control register 10			00000111$_B$
0000BB$_H$	ICR11	Interrupt control register 11			00000111$_B$
0000BC$_H$	ICR12	Interrupt control register 12			00000111$_B$
0000BD$_H$	ICR13	Interrupt control register 13			00000111$_B$
0000BE$_H$	ICR14	Interrupt control register 14			00000111$_B$
0000BF$_H$	ICR15	Interrupt control register 15			00000111$_B$
0000C0$_H$ to 0000FF$_H$		(Reserved area) *			
001FF0$_H$	PADR0	Detection address setting register 0 (low-order)	R/W	Address matching detection function	XXXXXXXX$_B$
001FF1$_H$		Detection address setting register 0 (middle-order)			XXXXXXXX$_B$
001FF2$_H$		Detection address setting register 0 (high-order)			XXXXXXXX$_B$
001FF3$_H$	PADR1	Detection address setting register 1 (low-order)	R/W		XXXXXXXX$_B$
001FF4$_H$		Detection address setting register 1 (middle-order)			XXXXXXXX$_B$
001FF5$_H$		Detection address setting register 1 (high-order)			XXXXXXXX$_B$
003900$_H$	TMR0/ TMRLR0	16-bit timer register 0/16-bit reload register	R,W	16-bit reload timer 0	XXXXXXXX$_B$
003901$_H$					XXXXXXXX$_B$
003902$_H$	TMR1/ TMRLR1	16-bit timer register 1/16-bit reload register	R,W	16-bit reload timer 1	XXXXXXXX$_B$
003903$_H$					XXXXXXXX$_B$
003904$_H$ to 00390F$_H$		(Reserved area) *			

Address	Register Abbreviation	Register	Read/ Write	Resource	Initial Value
003C38H, 003C39H	DLCR4	DLC register 4	R/W	CAN controller	XXXXXXXXB, XXXXXXXXB
003C3AH, 003C3BH	DLCR5	DLC register 5	R/W		XXXXXXXXB, XXXXXXXXB
003C3CH, 003C3DH	DLCR6	DLC register 6	R/W		XXXXXXXXB, XXXXXXXXB
003C3EH, 003C3FH	DLCR7	DLC register 7	R/W		XXXXXXXXB, XXXXXXXXB
003C40H to 003C47H	DTR0	Data register 0	R/W		XXXXXXXXB to XXXXXXXXB
003C48H to 003C4FH	DTR1	Data register 1	R/W		XXXXXXXXB to XXXXXXXXB
003C50H to 003C57H	DTR2	Data register 2	R/W		XXXXXXXXB to XXXXXXXXB
003C58H to 003C5FH	DTR3	Data register 3	R/W		XXXXXXXXB to XXXXXXXXB
003C60H to 003C67H	DTR4	Data register 4	R/W		XXXXXXXXB to XXXXXXXXB
003C68H to 003C6FH	DTR5	Data register 5	R/W		XXXXXXXXB to XXXXXXXXB
003C70H to 003C77H	DTR6	Data register 6	R/W		XXXXXXXXB to XXXXXXXXB
003C78H to 003C7FH	DTR7	Data register 7	R/W		XXXXXXXXB to XXXXXXXXB
003C80H to 003CFFH	(Reserved area) *				
003D00H, 003D01H	CSR	Control status register	R/W, R	CAN controller	0XXXX001B, 00XXX000B
003D02H	LEIR	Last event display register	R/W		000XX000B
003D03H	(Reserved area) *				
003D04H, 003D05H	RTEC	Send/receive error counter	R	CAN controller	00000000B, 00000000B
003D06H, 003D07H	BTR	Bit timing register	R/W		11111111B, X1111111B
003D08H	IDER	IDE register	R/W		XXXXXXXXB
003D09H	(Reserved area) *				
003D0AH	TRTRR	Send RTR register	R/W	CAN controller	00000000B
003D0BH	(Reserved area) *				
003D0CH	RFWTR	Remote frame receive wait register	R/W	CAN controller	XXXXXXXXB

Port 5 Pins Block Diagram

Analog input

Port data register (PDR)

PDR read

Output latch

PDR write

Port direction register (DDR)

Direction latch

DDR write

DDR read

Internal data bus

Pin

Standby control (SPL=1)

Standby control: Control among Stop mode (SPL=1), Time-base timer mode (SPL=1), and watch mode (SPL=1).

Port 5 Registers

■ Port 5 registers include port 5 data register (PDR5), port 5 direction register (DDR5), and analog input permission register (ADER).

■ Analog input permission register (ADER) allows or disallows input of analog signal to the analog input pin.

■ The bits configuring the register correspond to port 5 pins on a one-to-one basis.

Relation between Port 5 Registers and Pins

Port Name	Bits of Register and Corresponding Pins								
Port 5	PDR5, DDR5	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	ADER	ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0
	Corresponding pins	P57	P56	P55	P54	P53	P52	P51	P50

Watchdog Timer Block Diagram

Watchdog timer control register(WDTC)   Watch timer control register (WTC)

| PONR | — | WRST | ERST | SRST | WTE | WT1 | WT0 |

| WDCS |

Watchdog timer

Activate

Reset occurs
Shift to sleep mode
Shift to time-base timer mode
Shift to watch mode
Shift to stop mode

Counter clear control circuit

Count clock selector

2-bit counter

Watchdog reset generation circuit

Internal reset generation circuit

Clear

Time-base timer counter

Main clock (dividing HCLK by 2)

$\times 2^1$ | $\times 2^2$ | $\cdots$ | $\times 2^8$ | $\times 2^9$ | $\times 2^{10}$ | $\times 2^{11}$ | $\times 2^{12}$ | $\times 2^{13}$ | $\times 2^{14}$ | $\times 2^{15}$ | $\times 2^{16}$ | $\times 2^{17}$ | $\times 2^{18}$

Watch counter

Sub clock SCLK

$\times 2^1$ | $\times 2^2$ | $\cdots$ | $\times 2^5$ | $\times 2^6$ | $\times 2^7$ | $\times 2^8$ | $\times 2^9$ | $\times 2^{10}$ | $\times 2^{11}$ | $\times 2^{12}$ | $\times 2^{13}$ | $\times 2^{14}$ | $\times 2^{15}$

HCLK: Oscillation clock
SCLK: Sub clock
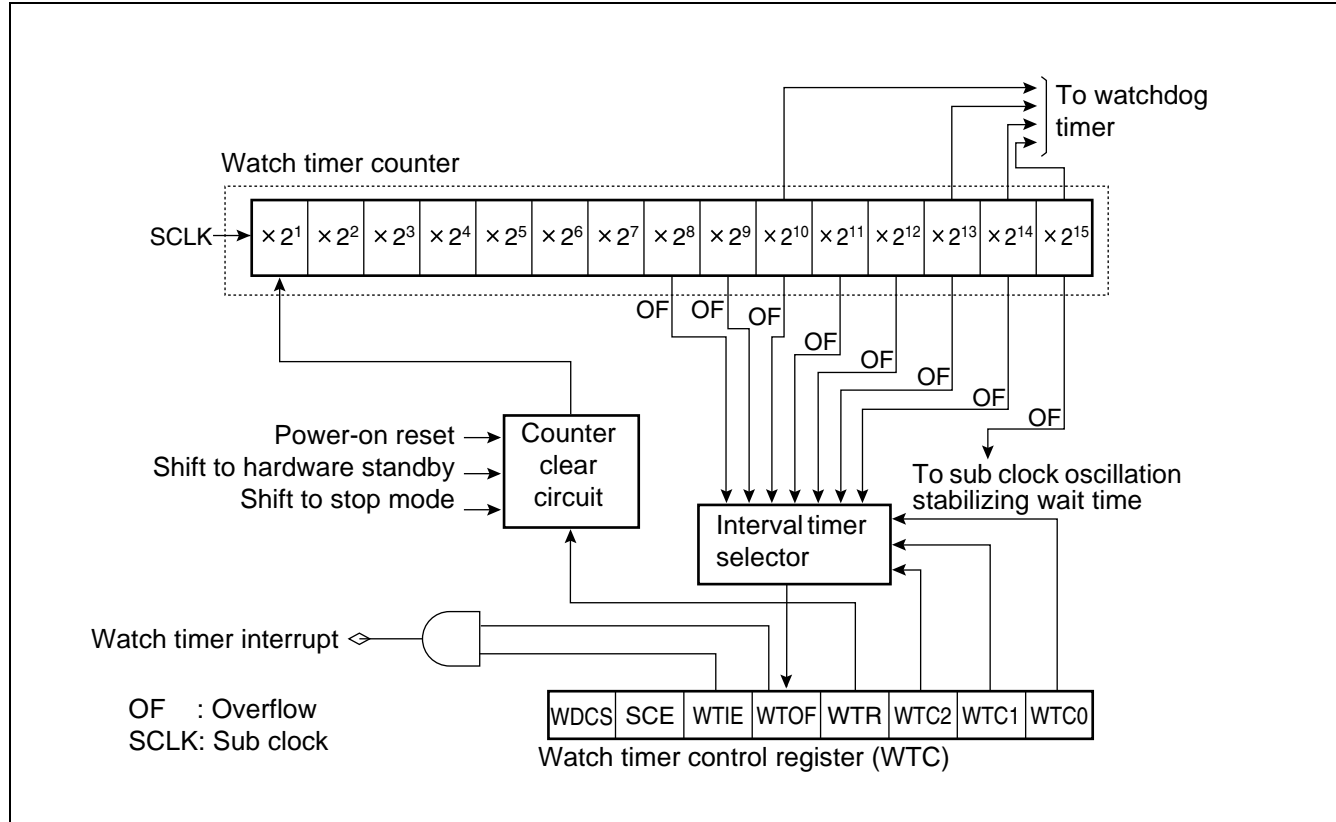
Input Capture Block Diagram
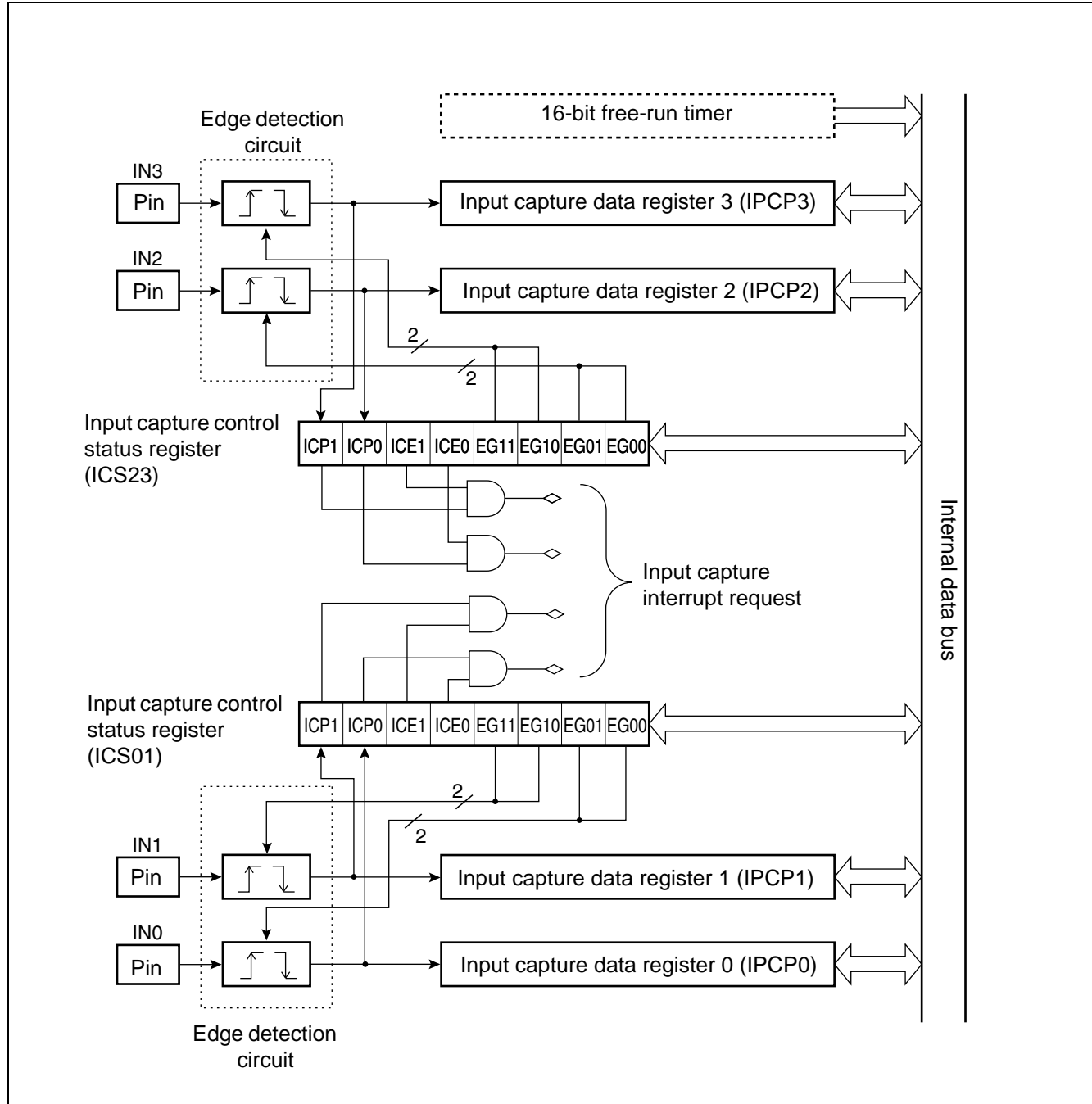
Watch Timer Block Diagram

Actual interrupt request number of watch timer is as follows:
Interrupt request number: #28 (1C$_H$)

Watch Timer Counter

A 15-bit up counter that uses sub clock (SCLK) as a count clock.

Counter Clear Circuit

A circuit that clears the watch timer counter.

12.7 8/16-bit PPG Timer Outline

The 8/16-bit PPG timer is a 2-channel reload timer module (PPG0 and PPG1) that allows outputting pulses of arbitrary cycle and duty cycle. Combination of the two channels allows selection among the following operations:

■ 8-bit PPG output 2-channel independent operation mode

■ 16-bit PPG output operation mode

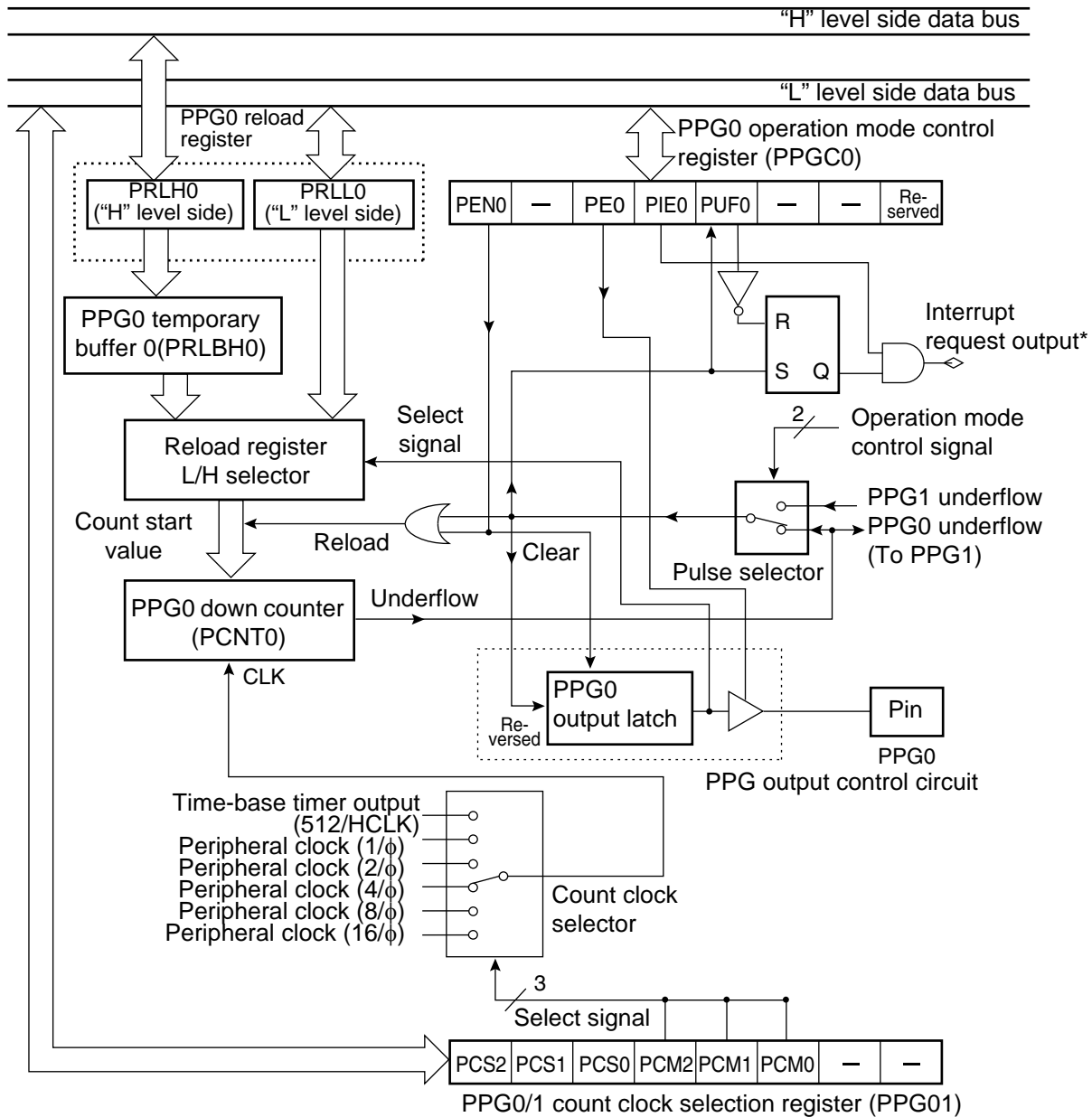■ 8-bit and 8-bit PPG output operation mode

MB90385 series device has two 8/16-bit built-in PPG timers. This section describes functions of PPG0/1. PPG2/3 have the same functions as those of PPG0/1.

Functions of 8/16-bit PPG Timer

The 8/16-bit PPG timer is composed of four 8-bit reload register (PRLH0/PRLL0, PRLH1/PRLL1) and two PPG down counters (PCNT0, PCNT1).

■ Widths of "H" and "L" in output pulse are specifiable independently. Cycle and duty factor of output pulse is specifiable arbitrarily.

■ Count clock is selectable among 6 internal clocks.

■ The timer is usable as an interval timer, by generating interrupt requests for each interval.

■ The time is usable as a D/A converter, with an external circuit.

8/16-bit PPG Timer 0 Block Diagram

"H" level side data bus

"L" level side data bus

PPG0 reload register

PRLH0 ("H" level side)   PRLL0 ("L" level side)

PPG0 operation mode control register (PPGC0)

PEN0 | — | PE0 | PIE0 | PUF0 | — | — | Reserved

PPG0 temporary buffer 0(PRLBH0)

R
S   Q

Interrupt request output*

Select signal

Reload register L/H selector

Count start value

Reload

2 — Operation mode control signal

PPG1 underflow
PPG0 underflow (To PPG1)

Pulse selector

PPG0 down counter (PCNT0)   Underflow

CLK

Clear

Reversed

PPG0 output latch

Pin

PPG0

PPG output control circuit

Time-base timer output (512/HCLK)
Peripheral clock (1/φ)
Peripheral clock (2/φ)
Peripheral clock (4/φ)
Peripheral clock (8/φ)
Peripheral clock (16/φ)

Count clock selector

3

Select signal

PCS2 | PCS1 | PCS0 | PCM2 | PCM1 | PCM0 | — | —

PPG0/1 count clock selection register (PPG01)

−   : Undefined
Reserved: Reserved bit
HCLK   : Oscillation clock frequency
φ   : Machine clock frequency
*   : Interrupt output of 8/16-bit PPG timer 0 is incorporated into one by the OR circuit against interrupt output of 8/16-bit PPG timer 1.

DTP/External Interrupt/CAN Wakeup Block Diagram

Detection level setting register (ELVR)

| LB7 | LA7 | LB6 | LA6 | LB5 | LA5 | LB4 | LA4 | Re-served | Re-served | Re-served | Re-served | Re-served | Re-served | LB0 | LA0 |

Internal data bus

Pin INT7 — Level/edge selector

Pin INT6 — Level/edge selector

Pin INT5 — Level/edge selector

Pin INT4 — Level/edge selector

Pin RX — Level/edge selector

DTP/external interrupt input detection circuit

| ER7 | ER6 | ER5 | ER4 | Re-served | Re-served | Re-served | ER0 |

DTP/external interrupt cause register (EIRR)

Interrupt request signal

Interrupt request signal

| EN7 | EN6 | EN5 | EN4 | Re-served | Re-served | Re-served | EN0 |

DTP/external interrupt permission register (ENIR)

13.6 Definition of A/D Converter Terms

Resolution:	Analog variation that is recognized by an A/D converter.
Linear error:	Deviation between a line across zero-transition line ("00 0000 00 0 0" $\longleftrightarrow$ "00 0000 0001") and full-scale transition line ("11 1111 11 1 0" $\longleftrightarrow$ "11 1111 1111") and actual conversion characteristics.
Differential linear error:	Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.
Total error:	Difference between an actual value and an ideal value. A total error includes zero transition error, full-scale transition error, and linear error.

Total error

Actual conversion characteristics

Digital output

(Actually-measured value)

Actual conversion characteristics

Ideal characteristics

Analog input
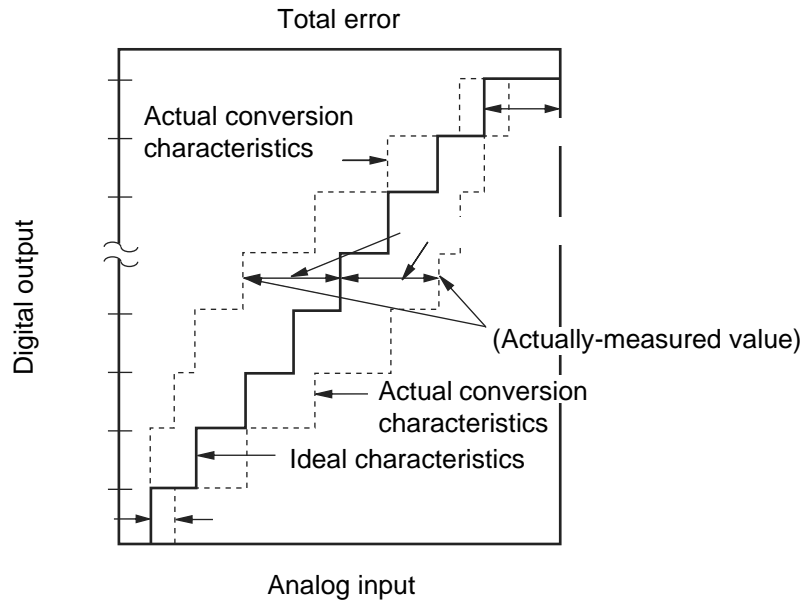
$$\text{Total error of digital output "N"} = \frac{V_{NT} - \{1\,\text{LSB} \times (N-1) + 0.5\,\text{LSB}\}}{1\,\text{LSB}}\quad[\text{LSB}]$$

$$1\,\text{LSB} = (\text{Ideal value})\,\frac{AVR - AV_{SS}}{1024}\,[\text{V}]$$

V_{OT} (Ideal value) $= AV_{SS} + 0.5\,\text{LSB}$ [V]

V_{FST} (Ideal value) $= AVR - 1.5\,\text{LSB}$ [V]

V_{NT}: A voltage at which digital output transits from $(N-1)_H$ to N_H.

(Continued)

13.7 Notes on A/D Converter Section

Use the device with external circuits of the following output impedance for analog inputs:

Recommended output impedance of external circuits are: Approx. 3.9 kΩ or lower (4.5 V $\leq$ AVcc $\leq$ 5.5 V) (sampling period=2.00 μs at 16 MHz machine clock), Approx. 11 kΩ or lower (4.0 V $\leq$ AVcc < 4.5 V) (sampling period=8.0 μs at 16 MHz machine clock).

If an external capacitor is used, in consideration of the effect by tap capacitance caused by external capacitors and on-chip capacitors, capacitance of the external one is recommended to be several thousand times as high as internal capacitor.

If output impedance of an external circuit is too high, a sampling period for an analog voltage may be insufficient.

- Analog input circuit model
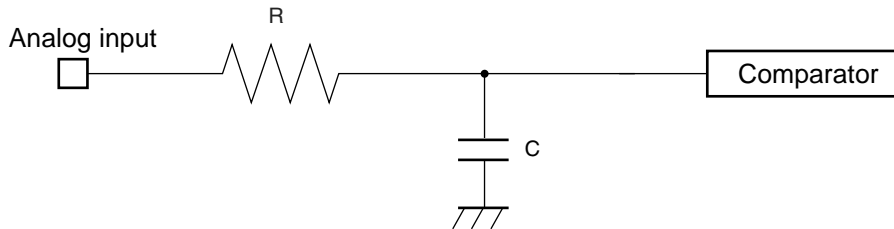
MB90F387/S, MB90387/S
4.5 V $\leq$ AV$_{CC}$ $\leq$ 5.5 V   R $\cong$ 2.35 kΩ, C $\cong$ 36.4 pF
4.0 V $\leq$ AV$_{CC}$ < 4.5 V   R $\cong$ 16.4 kΩ, C $\cong$ 36.4 pF

Note: Use the values in the figure only as a guideline.
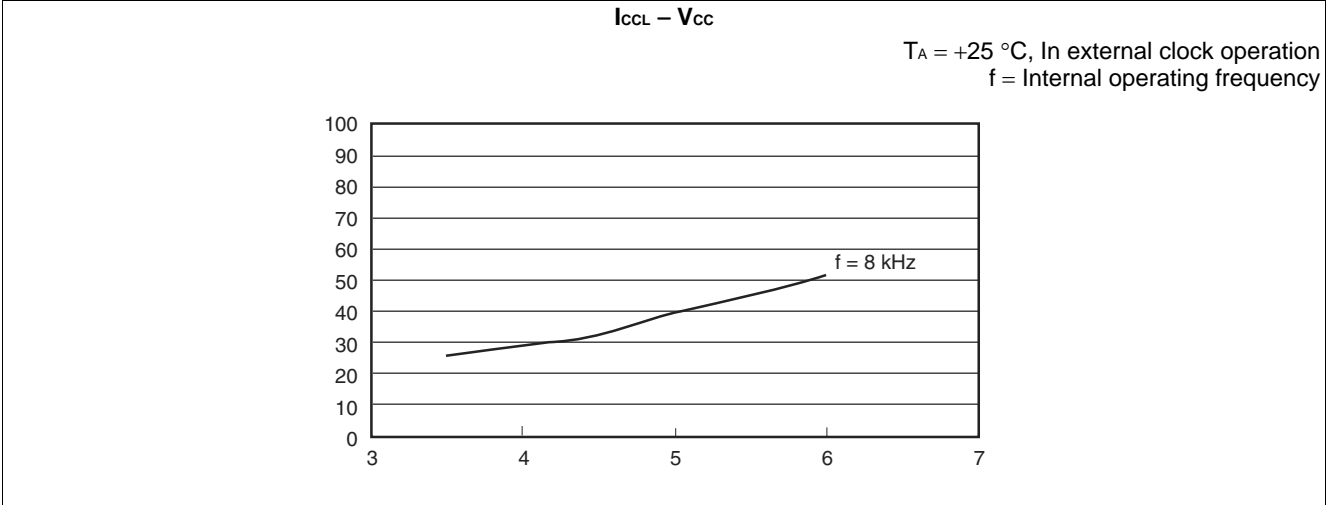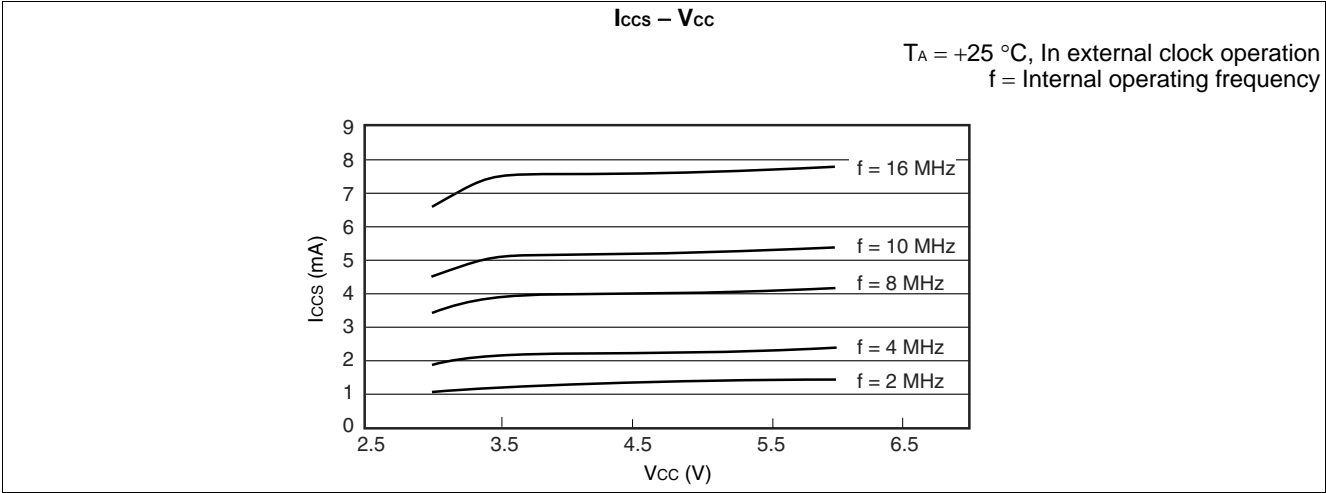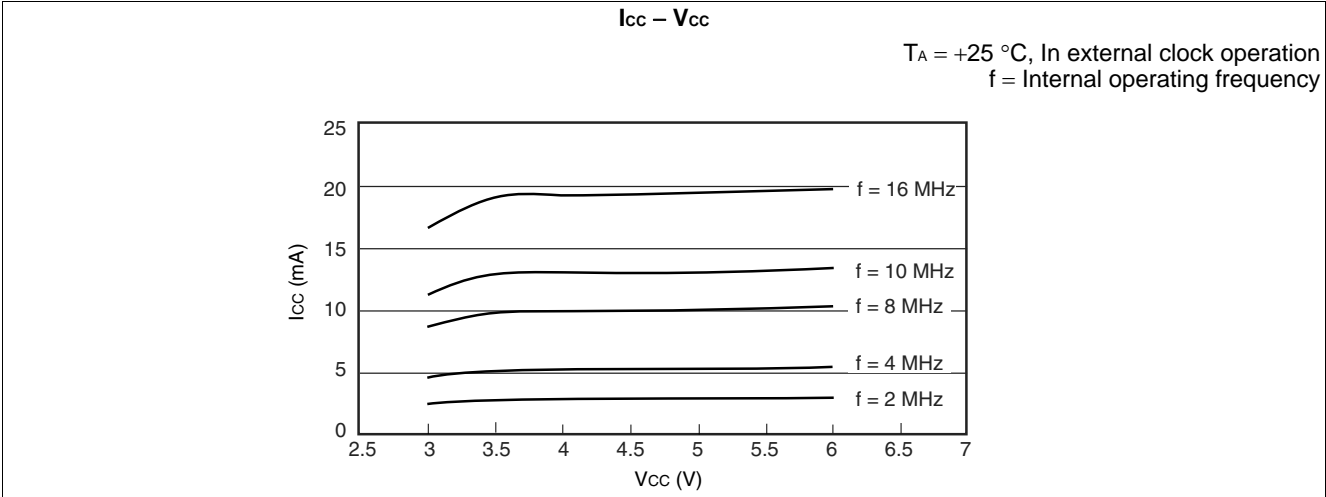
About errors

As [AVR-AVss] become smaller, values of relative errors grow larger.

13.8 Flash Memory Program/Erase Characteristics

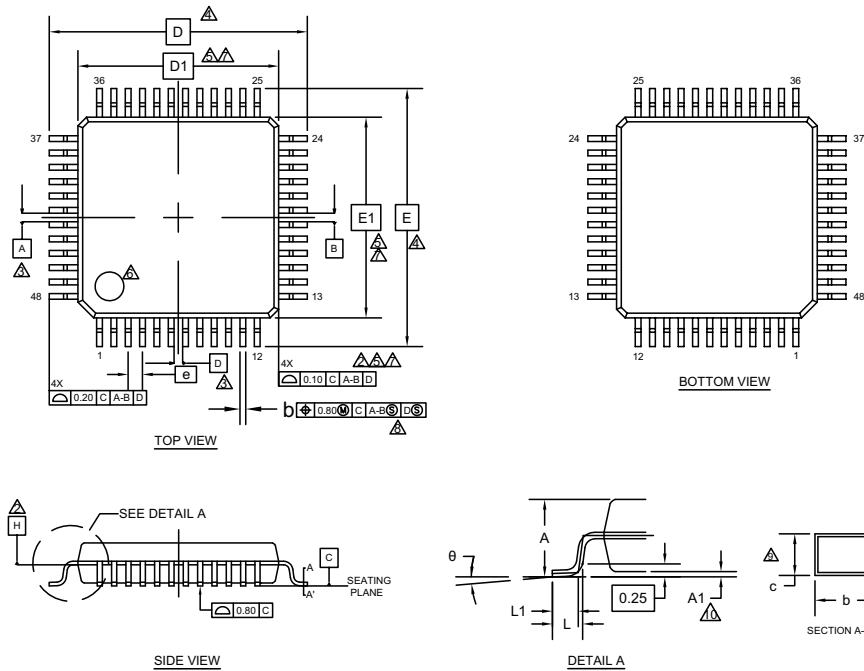| Parameter	Conditions	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	T_A = + 25 °C V_{CC} = 5.0 V	–	1	15	s	Excludes 00H programming prior to erasure
Chip erase time		–	4	–	s	Excludes 00H programming prior to erasure
Word (16-bit width) programming time		–	16	3,600	μs	Except for the over head time of the system
Program/Erase cycle	–	10,000	–	–	cycle	
Flash Data Retention Time	Average T_A = + 85 °C	20	–	–	Year	*

*: This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at + 85 °C).

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I$_{CC}$ – V$_{CC}$

T$_A$ = +25 °C, In external clock operation
f = Internal operating frequency

I$_{CCS}$ – V$_{CC}$

T$_A$ = +25 °C, In external clock operation
f = Internal operating frequency

I$_{CCL}$ – V$_{CC}$

T$_A$ = +25 °C, In external clock operation
f = Internal operating frequency

(Continued)

16. Package Dimension

TOP VIEW

BOTTOM VIEW

SIDE VIEW

DETAIL A

SECTION A-A'

SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.00	—	0.20
b	0.15	—	0.27
c	0.09	—	0.20
D	9.00 BSC		
D1	7.00 BSC		
e	0.50 BSC		
E	9.00 BSC		
E1	7.00 BSC		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
θ	0°	—	8°

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.

2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.

3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.

4. TO BE DETERMINED AT SEATING PLANE C.

5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.

7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.

8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.

9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.

10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-13731 **

PACKAGE OUTLINE, 48 LEAD LQFP
7.0X7.0X1.7 MM LQA048 REV**

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