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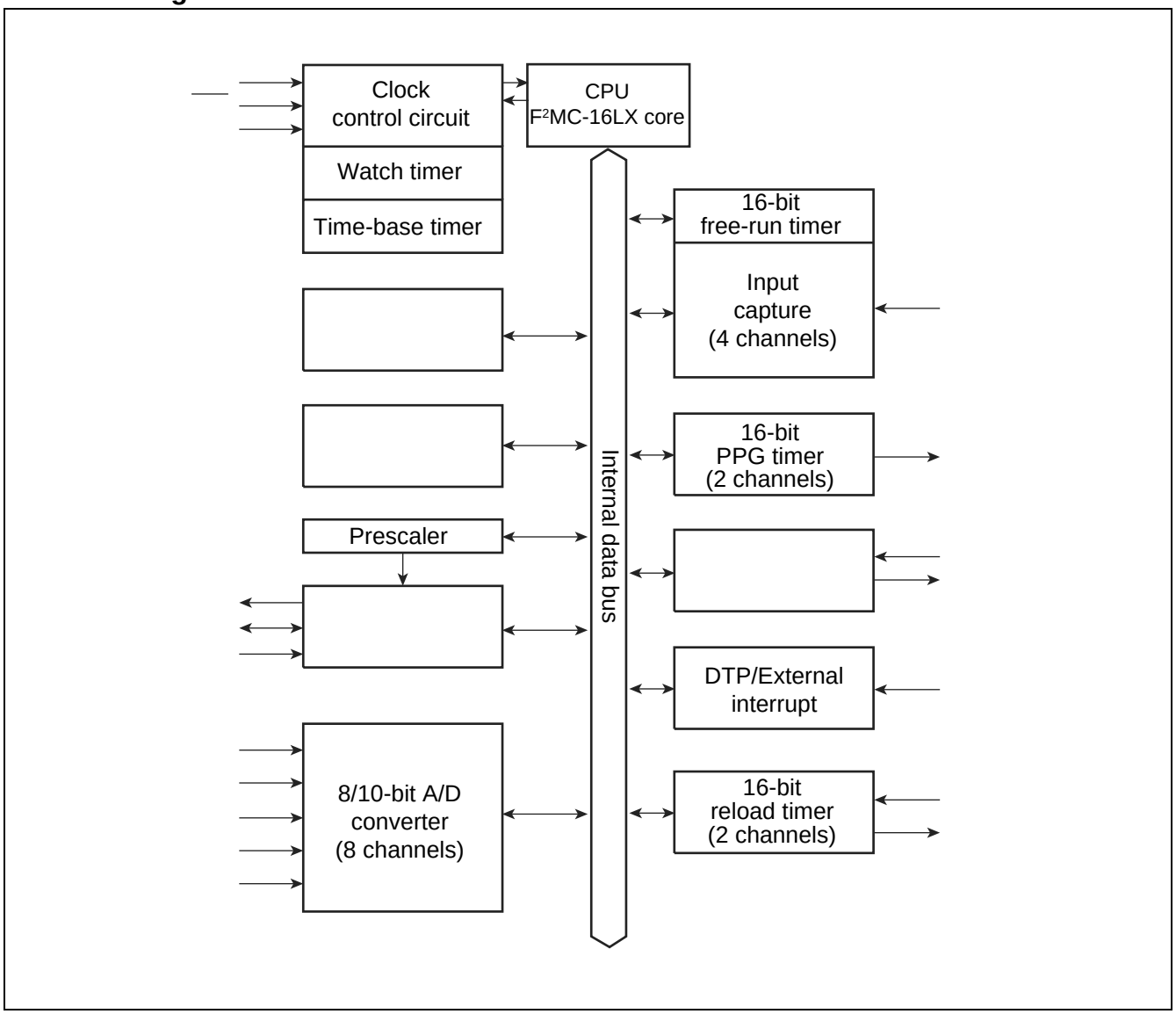
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, SCI, UART/USART
Peripherals	POR, WDT
Number of I/O	36
Program Memory Size	64KB (64K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90387spmt-gs-259

8. Block Diagram



9. Memory Map

MB90385 series allows specifying a memory access mode “single chip mode.”

9.1 Memory Allocation of MB90385

MB90385 series model has 24-bit wide internal address bus and up to 24-bit bus of external address bus.
A maximum of 16-Mbyte memory space of external access memory is accessible.

Address	Register Abbreviation	Register	Read/ Write	Resource	Initial Value
0000B0H	ICR00	Interrupt control register 00	R/W	Interrupt controller	00000111B
0000B1H	ICR01	Interrupt control register 01			00000111B
0000B2H	ICR02	Interrupt control register 02			00000111B
0000B3H	ICR03	Interrupt control register 03			00000111B
0000B4H	ICR04	Interrupt control register 04			00000111B
0000B5H	ICR05	Interrupt control register 05			00000111B
0000B6H	ICR06	Interrupt control register 06			00000111B
0000B7H	ICR07	Interrupt control register 07			00000111B
0000B8H	ICR08	Interrupt control register 08			00000111B
0000B9H	ICR09	Interrupt control register 09			00000111B
0000BAH	ICR10	Interrupt control register 10			00000111B
0000BBH	ICR11	Interrupt control register 11			00000111B
0000BCH	ICR12	Interrupt control register 12			00000111B
0000BDH	ICR13	Interrupt control register 13			00000111B
0000BEH	ICR14	Interrupt control register 14			00000111B
0000BFH	ICR15	Interrupt control register 15			00000111B
0000C0H to 0000FFH	(Reserved area) *				
001FF0H	PADR0	Detection address setting register 0 (low-order)	R/W	Address matching detection function	XXXXXXXXB
001FF1H		Detection address setting register 0 (middle-order)			XXXXXXXXB
001FF2H		Detection address setting register 0 (high-order)			XXXXXXXXB
001FF3H	PADR1	Detection address setting register 1 (low-order)	R/W		XXXXXXXXB
001FF4H		Detection address setting register 1 (middle-order)			XXXXXXXXB
001FF5H		Detection address setting register 1 (high-order)			XXXXXXXXB
003900H	TMR0/ TMRLR0	16-bit timer register 0/16-bit reload register	R,W	16-bit reload timer 0	XXXXXXXXB
003901H					XXXXXXXXB
003902H	TMR1/ TMRLR1	16-bit timer register 1/16-bit reload register	R,W	16-bit reload timer 1	XXXXXXXXB
003903H					XXXXXXXXB
003904H to 00390FH	(Reserved area) *				

Address	Register Abbreviation	Register	Read/ Write	Resource	Initial Value
003D0D$_H$	(Reserved area) *				
003D0E$_H$	TIER	Send completion interrupt permission register	R/W	CAN controller	00000000$_B$
003D0F$_H$	(Reserved area) *				
003D10$_H$, 003D11$_H$	AMSR	Acceptance mask selection register	R/W	CAN controller	XXXXXXXX$_B$, XXXXXXXX$_B$
003D12$_H$, 003D13$_H$	(Reserved area) *				
003D14$_H$ to 003D17$_H$	AMR0	Acceptance mask register 0	R/W	CAN controller	XXXXXXXX$_B$ to XXXXXXXX$_B$
003D18$_H$ to 003D1B$_H$	AMR1	Acceptance mask register 1	R/W		XXXXXXXX$_B$ to XXXXXXXX$_B$
003D1C$_H$ to 003DFF$_H$	(Reserved area) *				
003E00$_H$ to 003EFF$_H$	(Reserved area) *				
003FF0$_H$ to 003FFF$_H$	(Reserved area) *				

Initial values:

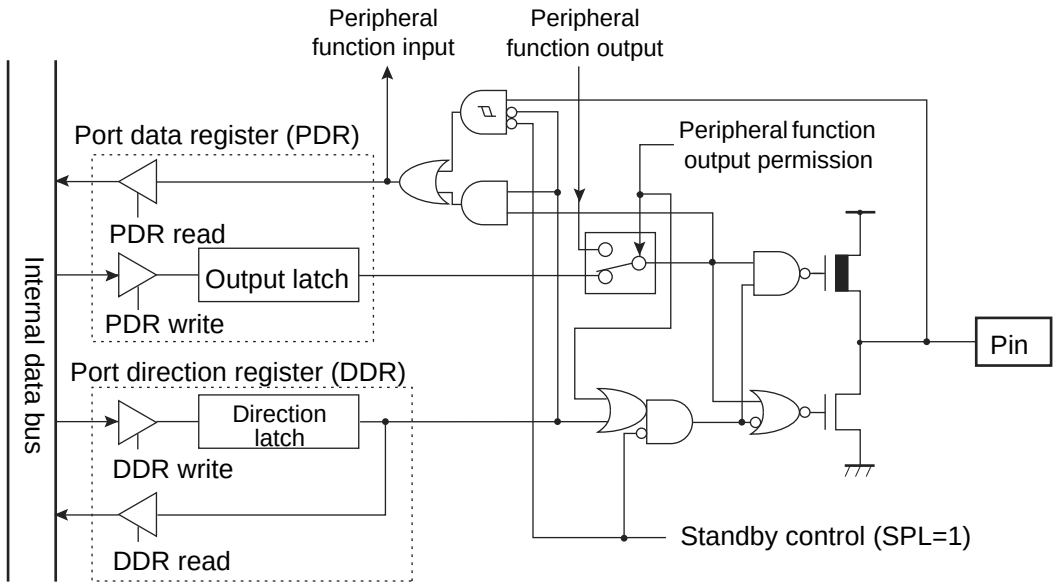
0: Initial value of this bit is “0.”

1: Initial value of this bit is “1.”

X: Initial value of this bit is undefined.

*: “Reserved area” should not be written anything. Result of reading from “Reserved area” is undefined.

Port 3 Pins Block Diagram (general-purpose input/output port)



Standby control: Control among Stop mode (SPL=1), Time-base timer mode (SPL=1), and watch mode (SPL=1).

Port 3 Registers

■ Port 3 registers include port 3 data register (PDR3) and port 3 direction register (DDR3).

■ The bits configuring the register correspond to port 3 pins on a one-to-one basis.

Relation between Port 3 Registers and Pins

Port Name	Bits of Register and Corresponding Pins								
Port 3	PDR3, DDR3	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	Corresponding pins	P37	P36*	P35*	–	P33	P32	P31	P30

*: P35 and P36 do not exist on MB90387and MB90F387.

12.4 16-bit Input/Output Timer

The 16-bit input/output timer is a compound module composed of 16-bit free-run timer, (1 unit) and input capture (2 units, 4 input pins). The timer, using the 16-bit free-run timer as a basis, enables measurement of clock cycle of an input signal and its pulse width.

Configuration of 16-bit Input/Output Timer

The 16-bit input/output timer is composed of the following modules:

- 16-bit free-run timer (1 unit)
- Input capture (2 units, 2 input pins per unit)

Functions of 16-bit Input/Output Timer

Functions of 16-bit Free-run Timer

The 16-bit free-run timer is composed of 16-bit up counter, timer counter control status register, and prescaler. The 16-bit up counter increments in synchronization with dividing ratio of machine clock.

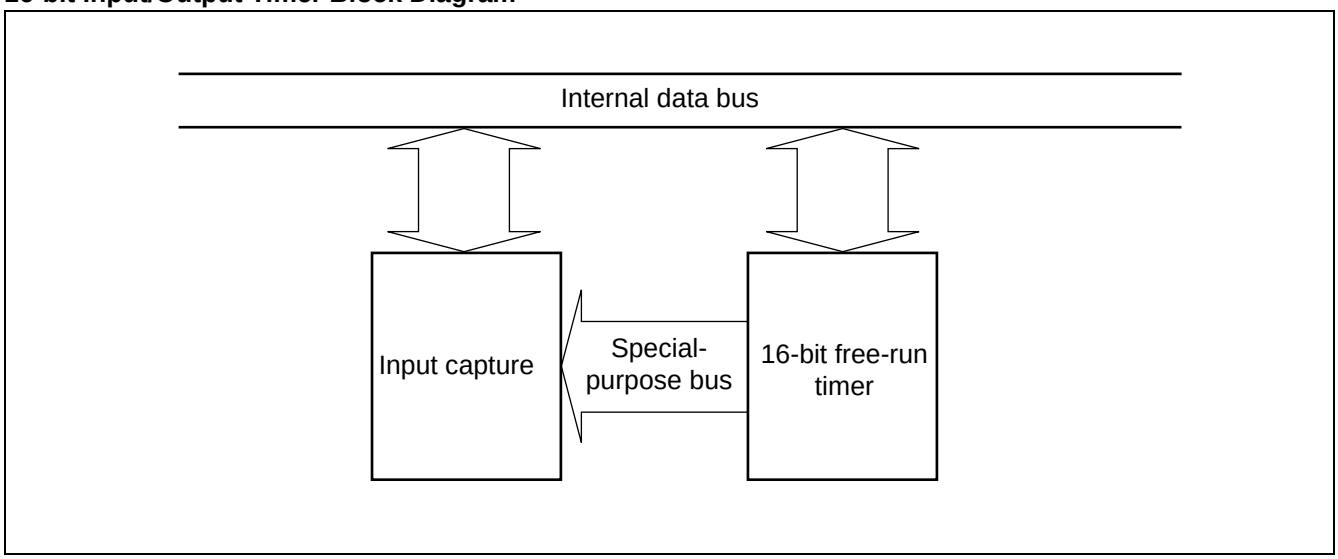
- Count clock is set among four types of machine clock dividing rates.
- Generation of interrupt is allowed by counter value overflow.
- Activation of expanded intelligent I/O service (EI^{2}OS) is allowed by interrupt generation.
- Counter value of 16-bit free-run timer is cleared to "0000$_H$" by either resetting or software-clearing with timer count clear bit (TCCS: CLR).
- Counter value of 16-bit free-run timer is output to input capture, which is available as base time for capture operation.

Functions of Input Capture

The input capture, upon detecting an edge of a signal input to the input pin from external device, stores a counter value of 16-bit free-run timer at the time of detection into the input capture data register. The function includes the input capture data registers corresponding to four input pins, input capture control status register, and edge detection circuit.

- Rising edge, falling edge, and both edges are selectable for detection.
- Generating interrupt on CPU is allowed by detecting an edge of input signal.
- Expanded intelligent I/O service (EI^{2}OS) is activated by interrupt generation.
- The four input capture input pins and input capture data registers allows monitoring of a maximum of four events.

16-bit Input/Output Timer Block Diagram



12.6 Watch Timer Outline

The watch timer is a 15-bit free-run counter that increments in synchronization with sub clock.

- Interval time is selectable among 7 choices, and generation of interrupt request is allowed for each interval.
- Provides operation clock to the subclock oscillation stabilizing wait timer and watchdog timer.
- Always uses subclock as a count clock regardless of settings of clock selection register (CKSCR).

Interval Timer Function

- In the watch timer, a bit corresponding to the interval time overflows (carry-over) when an interval time, which is specified by interval time selection bit, is reached. Then overflow flag bit is set (WTC: WTOF=1).
- If an interrupt by overflow is permitted (WTC: WTIE=1), an interrupt request is generated upon setting an overflow flag bit.
- Interval time of watch timer is selectable among the following seven choices:

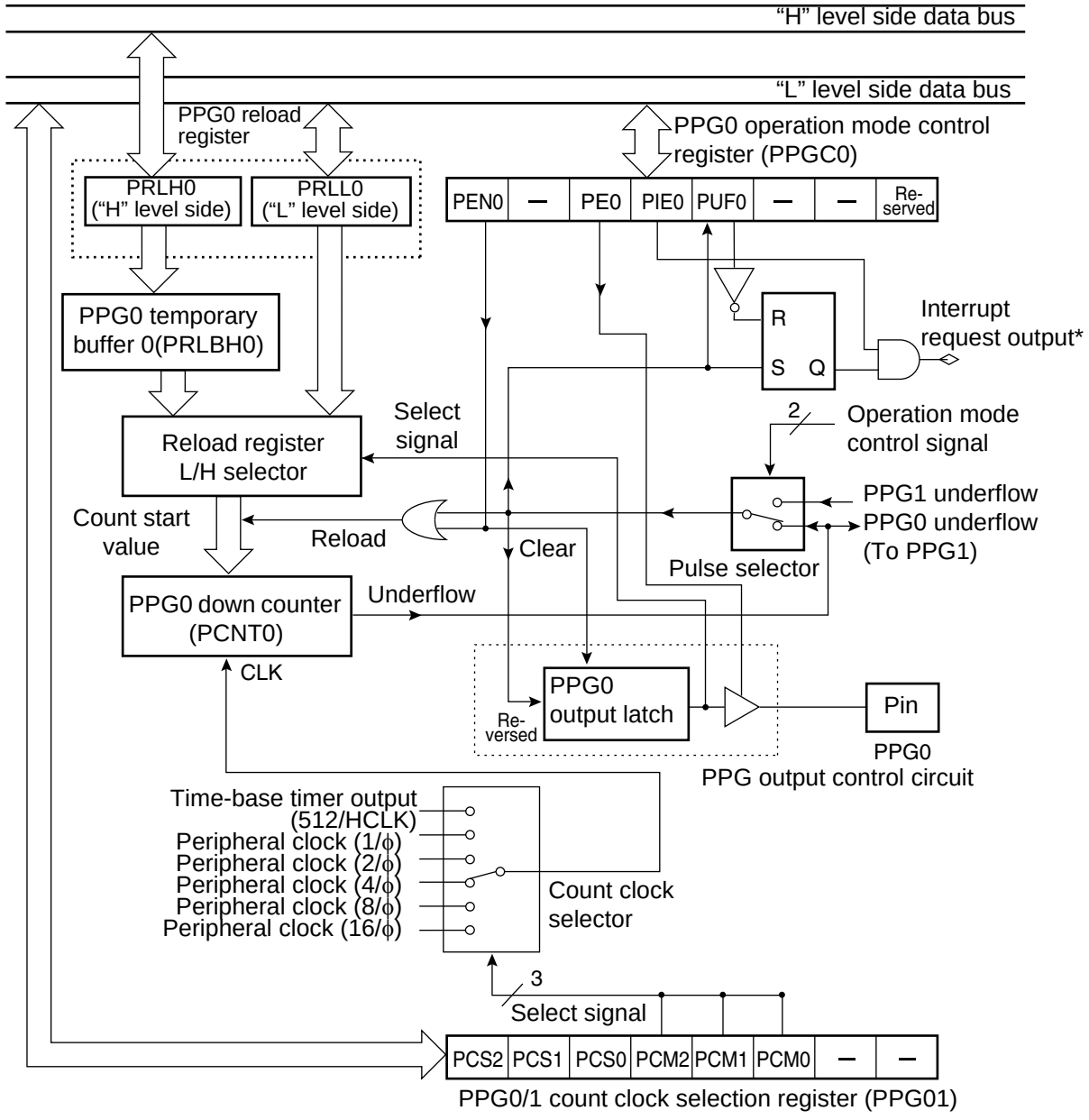
Interval Time of Watch Timer

Sub Clock Cycle	Interval Time
1/SCLK (122 μs)	2^8/SCLK (31.25 ms)
	2^9/SCLK (62.5 ms)
	2^{10}/SCLK (125 ms)
	2^{11}/SCLK (250 ms)
	2^{12}/SCLK (500 ms)
	2^{13}/SCLK (1.0 s)
	2^{14}/SCLK (2.0 s)

SCLK: Sub clock frequency

Values in parentheses “( )” are calculation when operating with 8.192 kHz clock.

8/16-bit PPG Timer 0 Block Diagram



– : Undefined
Reserved: Reserved bit
HCLK : Oscillation clock frequency
ϕ : Machine clock frequency
* : Interrupt output of 8/16-bit PPG timer 0 is incorporated into one by the OR circuit against interrupt output of 8/16-bit PPG timer 1.

12.8 Delay Interrupt Generation Module Outline

The delay interrupt generation module is a module that generates interrupts for switching tasks. Generation of a hardware interrupt request is performed by software.

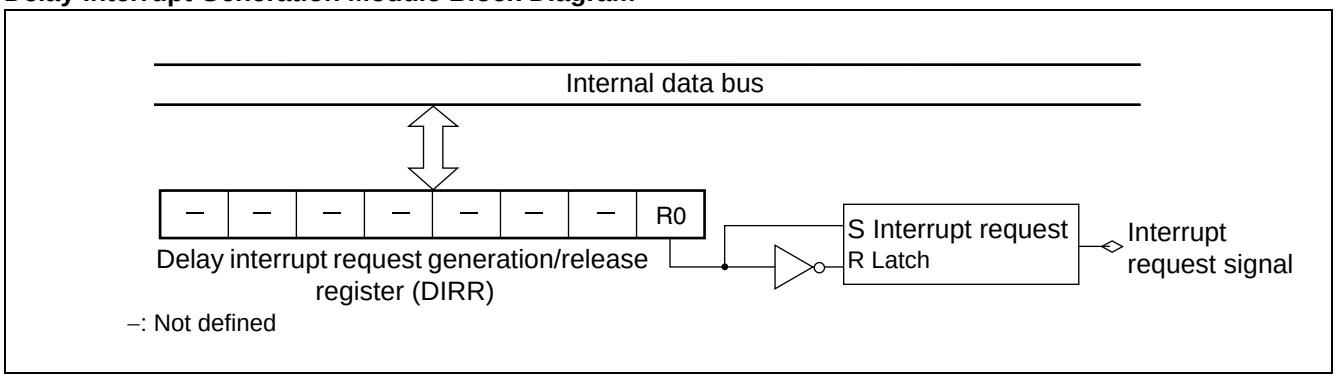
Delay Interrupt Generation Module Outline

Using the delay interrupt generation module, hardware interrupt request is generated and released by software.

Table 12-1. Delay Interrupt Generation Module Outline

	Function and Control
Cause of interrupt	Set “1” in R0 bit of delay interrupt request generation/release register (DIRR: R0=1), generating an interrupt request. Set “0” in R0 bit of delay interrupt request generation/release register (DIRR: R0=0), releasing an interrupt request.
Interrupt number	#42 ($2A_H$)
Interrupt control	No setting of permission register is provided.
Interrupt flag	Retained in DIRR: R0 bit
EI^2OS	Not ready for expanded intelligent I/O service.

Delay Interrupt Generation Module Block Diagram



Interrupt Request Latch

A latch that retains settings on delay interrupt request generation/release register (generation or release of delay interrupt request).

Delay Interrupt Request Generation/Release Register (DIRR)

Generates or releases delay interrupt request.

Interrupt Number

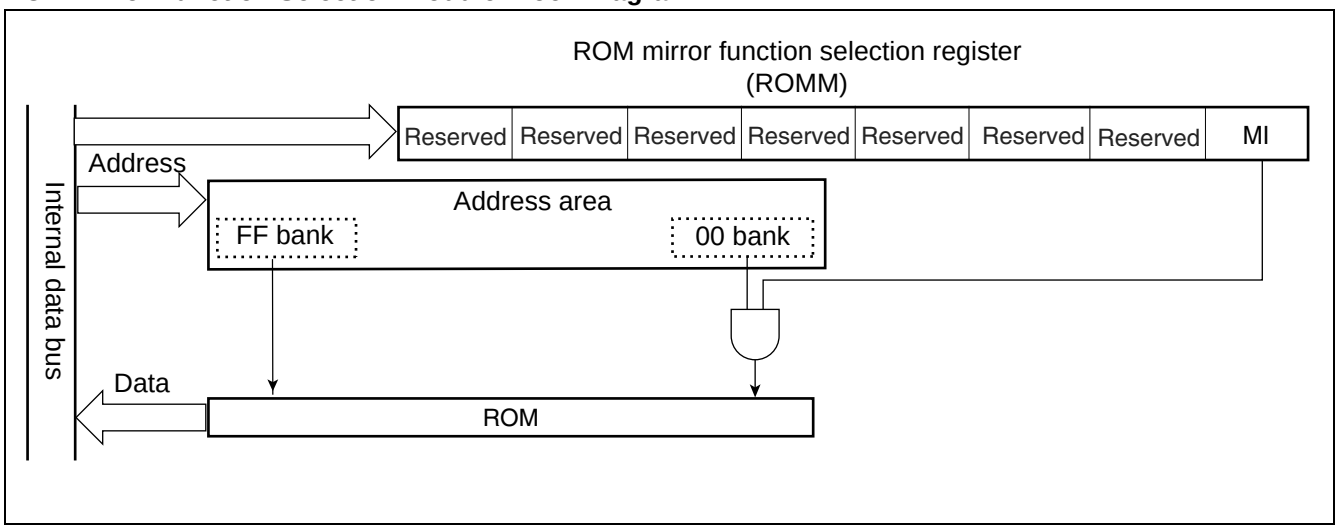
An interrupt number used in delay interrupt generation module is as follows:

Interrupt number: #42 ($2A_H$)

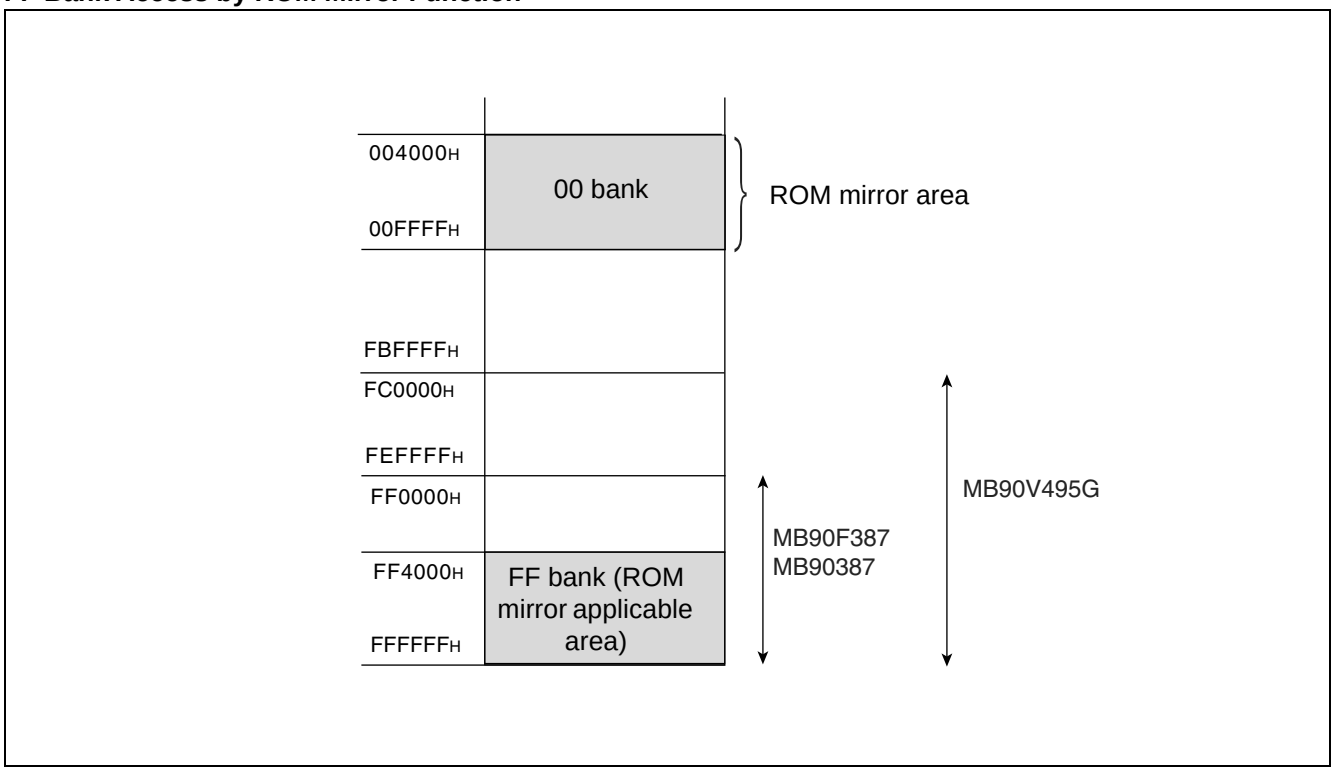
12.14 ROM Mirror Function Selection Module Outline

The ROM mirror function selection module sets the data in ROM assigned to FF bank so that the data is read by access to 00 bank.

ROM Mirror Function Selection Module Block Diagram



FF Bank Access by ROM Mirror Function



Sector Configuration of 512 Kbit Flash Memory

Flash memory	CPU address	Writer address*
SA0 (32 Kbytes)	FF0000H FF7FFFH	70000H 77FFFH
SA1 (8 Kbytes)	FF8000H FF9FFFH	78000H 79FFFH
SA2 (8 Kbytes)	FFA000H FFBFFFH	7A000H 7BFFFH
SA3 (16 Kbytes)	FFC000H FFFFFFH	7C000H 7FFFFH

*: “Writer address” is an address equivalent to CPU address, which is used when data is written on Flash memory, using parallel writer. When writing/deleting data with general-purpose writer, the writer address is used for writing and deleting.

13. Electrical Characteristics

13.1 Absolute Maximum Rating

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	
	AV_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	$V_{CC} = AV_{CC}$*2
	AVR	V_{SS} – 0.3	V_{SS} + 6.0	V	$AV_{CC} \geq AVR$*2
Input voltage*1	V_I	V_{SS} – 0.3	V_{SS} + 6.0	V	*3
Output voltage*1	V_O	V_{SS} – 0.3	V_{SS} + 6.0	V	*3
Maximum clamp current	I_{CLAMP}	– 2.0	+ 2.0	mA	*7
Total maximum clamp current	$\Sigma \mid I_{CLAMP} \mid$	–	20	mA	*7
“L” level maximum output current	I_{OL1}	–	15	mA	Normal output*4
	I_{OL2}	–	40	mA	High-current output*4
“L” level average output current	I_{OLAV1}	–	4	mA	Normal output*5
	I_{OLAV2}	–	30	mA	High-current output*5
“L” level maximum total output current	ΣI_{OL1}	–	125	mA	Normal output
	ΣI_{OL2}	–	160	mA	High-current output
“L” level average total output current	ΣI_{OLAV1}	–	40	mA	Normal output*6
	ΣI_{OLAV2}	–	40	mA	High-current output*6
“H” level maximum output current	I_{OH1}	–	–15	mA	Normal output*4
	I_{OH2}	–	–40	mA	High-current output*4
“H” level average output current	I_{OHAV1}	–	–4	mA	Normal output*5
	I_{OHAV2}	–	–30	mA	High-current output*5
“H” level maximum total output current	ΣI_{OH1}	–	–125	mA	Normal output
	ΣI_{OH2}	–	–160	mA	High-current output
“H” level average total output current	ΣI_{OHAV1}	–	–40	mA	Normal output*6
	ΣI_{OHAV2}	–	–40	mA	High-current output*6
Power consumption	P_D	–	245	mW	
Operating temperature	T_A	–40	+105	°C	
Storage temperature	Tstg	–55	+150	°C	

*1: The parameter is based on $V_{SS} = AV_{SS} = 0.0$ V.

*2: AVcc and AVR should not exceed Vcc.

*3: V_I and V_O should not exceed Vcc + 0.3 V. However if the maximum current to/from an input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating.

*4: A peak value of an applicable one pin is specified as a maximum output current.

*5: An average current value of an applicable one pin within 100 ms is specified as an average output current. (Average value is found by multiplying operating current by operating rate.)

*6: An average current value of all pins within 100 ms is specified as an average total output current. (Average value is found by multiplying operating current by operating rate.)

*7:

■ Applicable to pins: P10 to P17, P20 to P27, P30 to P33, P35*, P36*, P37, P40 to P44, P50 to P57
*: P35 and P36 are MB90387S and MB90F387S only.

13.2 Recommended Operating Conditions

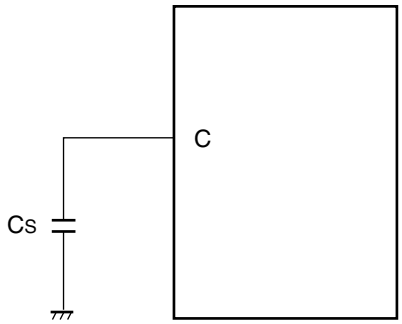
(V_{SS} = AV_{SS} = 0.0V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	V_{CC}	3.5	5.0	5.5	V	Under normal operation
		3.0	–	5.5	V	Retain status of stop operation
	AV_{CC}	4.0	–	5.5	V	*2
Smoothing capacitor	C_S	0.1	–	1.0	μF	*1
Operating temperature	T_A	−40	–	+105	°C	

*1: Use a ceramic capacitor, or a capacitor of similar frequency characteristics. On the Vcc pin, use a bypass capacitor that has a larger capacity than that of Cs.
Refer to the following figure for connection of smoothing capacitor Cs.

*2: AVcc is a voltage at which accuracy is guaranteed. AVcc should not exceed Vcc.

- C pin connection diagram



WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

13.3 DC Characteristics

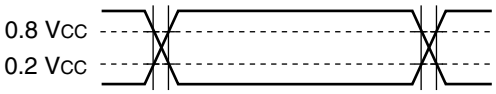
(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IHS}	CMOS hysteresis input pin	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	
	V_{IHM}	MD input pin	—	V_{CC} – 0.3	—	V_{CC} + 0.3	V	
"L" level input voltage	V_{ILS}	CMOS hysteresis input pin	—	V_{SS} – 0.3	—	0.2 V_{CC}	V	
	V_{ILM}	MD input pin	—	V_{SS} – 0.3	—	V_{SS} + 0.3	V	
"H" level output voltage	V_{OH1}	Pins other than P14 to P17	V_{CC} = 4.5 V, I_{OH} = –4.0 mA	V_{CC} – 0.5	—	—	V	
	V_{OH2}	P14 to P17	V_{CC} = 4.5 V, I_{OH} = –14.0 mA	V_{CC} – 0.5	—	—	V	
"L" level output voltage	V_{OL1}	Pins other than P14 to P17	V_{CC} = 4.5 V, I_{OL} = 4.0 mA	—	—	0.4	V	
	V_{OL2}	P14 to P17	V_{CC} = 4.5 V, I_{OL} = 20.0 mA	—	—	0.4	V	
Input leak current	I_{IL}	All input pins	V_{CC} = 5.5 V, V_{SS} < V_I < V_{CC}	–5	—	+5	µA	
Power supply current*	I_{CC}	V_{CC}	V_{CC} = 5.0 V, Internally operating at 16 MHz, normal operation.	—	25	30	mA	
			V_{CC} = 5.0 V, Internally operating at 16 MHz, writing on Flash memory.	—	45	50	mA	MB90F387/S
			V_{CC} = 5.0 V, Internally operating at 16 MHz, deleting on Flash memory.	—	45	50	mA	MB90F387/S
	I_{CCS}		V_{CC} = 5.0 V, Internally operating at 16 MHz, sleeping.	—	8	12	mA	
	I_{CTS}		V_{CC} = 5.0 V, Internally operating at 2 MHz, transition from main clock mode, in time-base timer mode.	—	0.75	1.0	mA	MB90F387/S
					0.2	0.35		MB90387/S

Rating values of alternating current is defined by the measurement reference voltage values shown below:

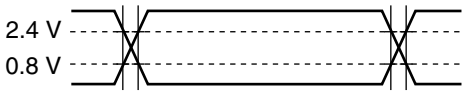
- Input signal waveform

Hysteresis input pin



- Output signal waveform

Output pin



13.4.2 Reset Input Timing

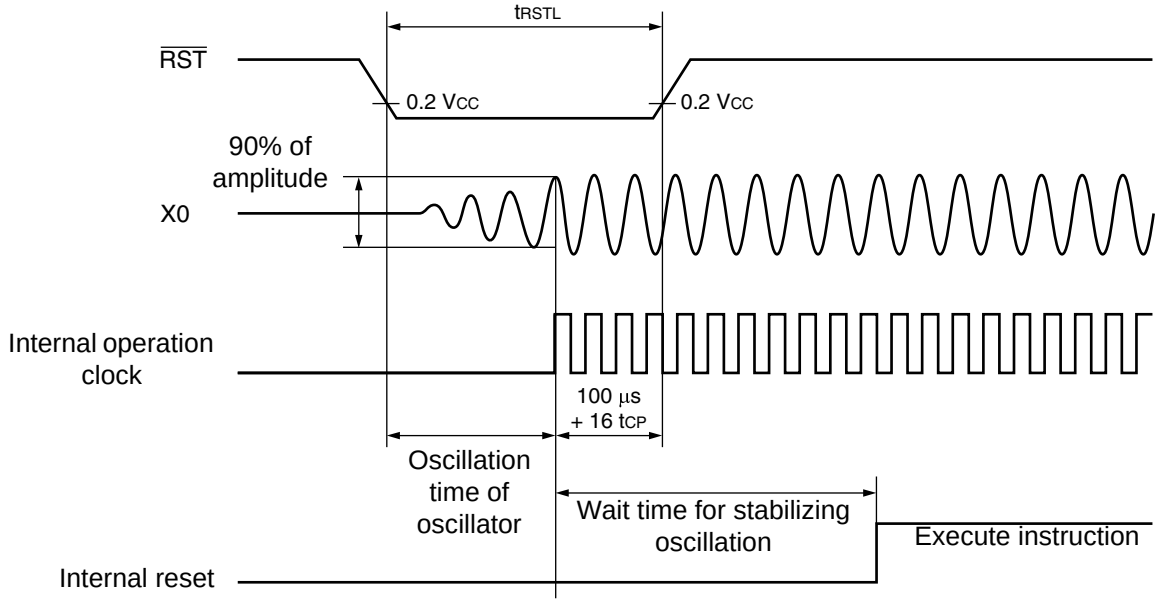
Parameter	Symbol	Pin Name	Value		Unit	Remarks
			Min	Max		
Reset input time	t_{RSTL}	RST	16 t_{CP}*3	–	ns	Normal operation
			Oscillation time of oscillator*1 + 100 μs + 16 t_{CP}*3	–	–	In sub clock*2, sub sleep*2, watch*2 and stop mode
			100	–	μs	In timebase timer

*1: Oscillation time of oscillator is time that the amplitude reached the 90%. In the crystal oscillator, the oscillation time is between several ms to tens of ms. In ceramic oscillator, the oscillation time is between hundreds of μs to several ms. In the external clock, the oscillation time is 0 ms.

*2: Except for MB90F387S and MB90387S.

*3: Refer to "(1) Clock timing" ratings for t_{CP} (internal operation clock cycle time).

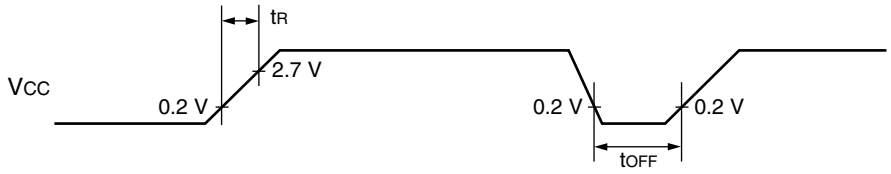
- In sub clock, sub sleep, watch and stop mode



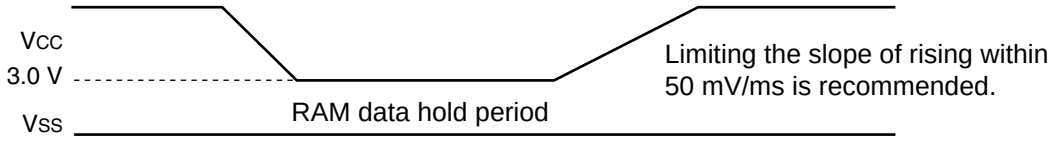
13.4.3 Power-on Reset

(V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Power supply rise time	t_R	V_{CC}	–	0.05	30	ms	
Power supply shutdown time	t_{OFF}	V_{CC}		1	–	ms	Waiting time until power-on



Sudden change of power supply voltage may activate the power-on reset function. When changing power supply voltages during operation, raise the power smoothly by suppressing variation of voltages as shown below. When raising the power, do not use PLL clock. However, if voltage drop is 1V/s or less, use of PLL clock is allowed during operation.



13.7 Notes on A/D Converter Section

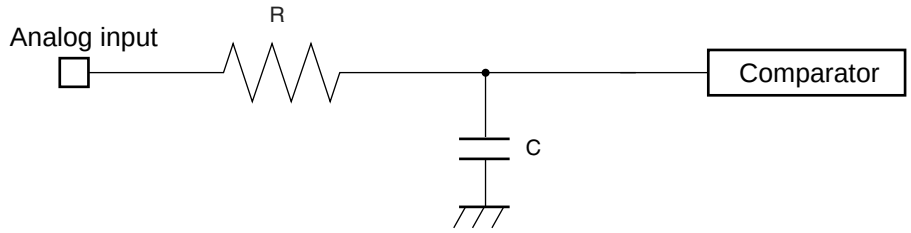
Use the device with external circuits of the following output impedance for analog inputs:

Recommended output impedance of external circuits are: Approx. 3.9 kΩ or lower (4.5 V ≤ AVcc ≤ 5.5 V) (sampling period=2.00 μs at 16 MHz machine clock), Approx. 11 kΩ or lower (4.0 V ≤ AVcc < 4.5 V) (sampling period=8.0 μs at 16 MHz machine clock).

If an external capacitor is used, in consideration of the effect by tap capacitance caused by external capacitors and on-chip capacitors, capacitance of the external one is recommended to be several thousand times as high as internal capacitor.

If output impedance of an external circuit is too high, a sampling period for an analog voltage may be insufficient.

- Analog input circuit model



MB90F387/S, MB90387/S

4.5 V ≤ AV_{CC} ≤ 5.5 V R ≅ 2.35 kΩ, C ≅ 36.4 pF

4.0 V ≤ AV_{CC} < 4.5 V R ≅ 16.4 kΩ, C ≅ 36.4 pF

Note: Use the values in the figure only as a guideline.

About errors

As [AVR-AVss] become smaller, values of relative errors grow larger.

13.8 Flash Memory Program/Erase Characteristics

Parameter	Conditions	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	T_A = + 25 °C V_{CC} = 5.0 V	–	1	15	s	Excludes 00H programming prior to erasure
Chip erase time		–	4	–	s	Excludes 00H programming prior to erasure
Word (16-bit width) programming time		–	16	3,600	μs	Except for the over head time of the system
Program/Erase cycle	–	10,000	–	–	cycle	
Flash Data Retention Time	Average T_A = + 85 °C	20	–	–	Year	*

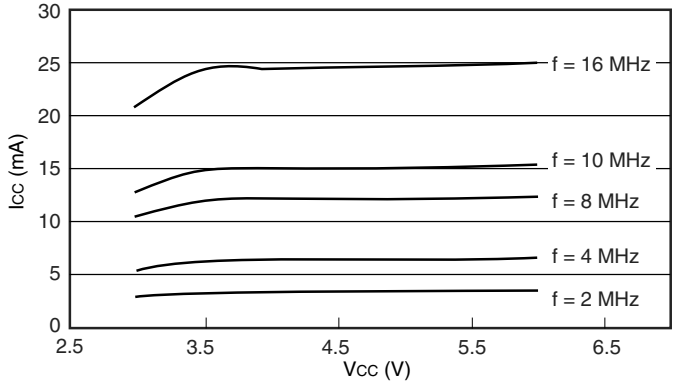
*: This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at + 85 °C).

14. Example Characteristics

MB90F387

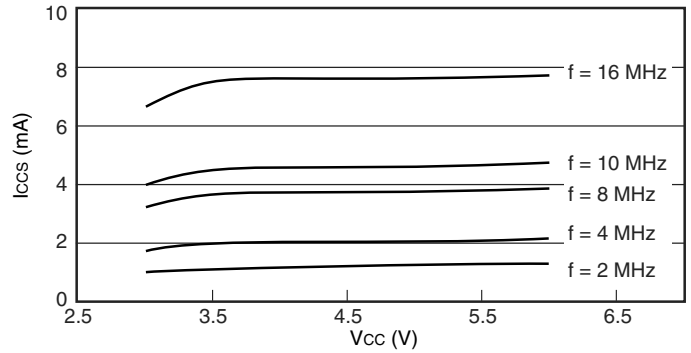
I_{CC} – V_{CC}

T_A = +25 °C, In external clock operation
f = Internal operating frequency



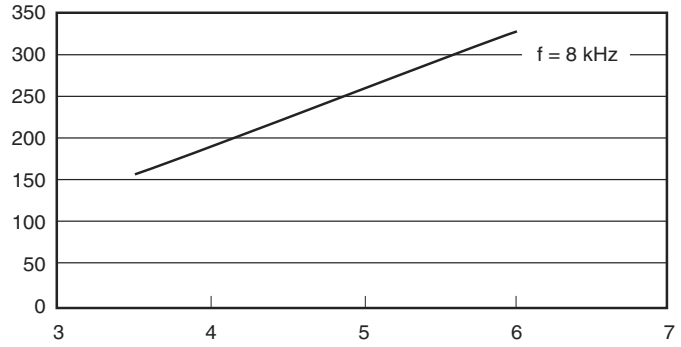
I_{CCS} – V_{CC}

T_A = +25 °C, In external clock operation
f = Internal operating frequency



I_{CCL} – V_{CC}

T_A = +25 °C, In external clock operation
f = Internal operating frequency



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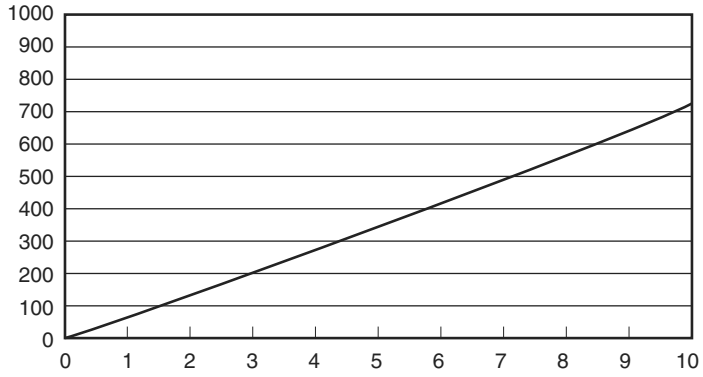
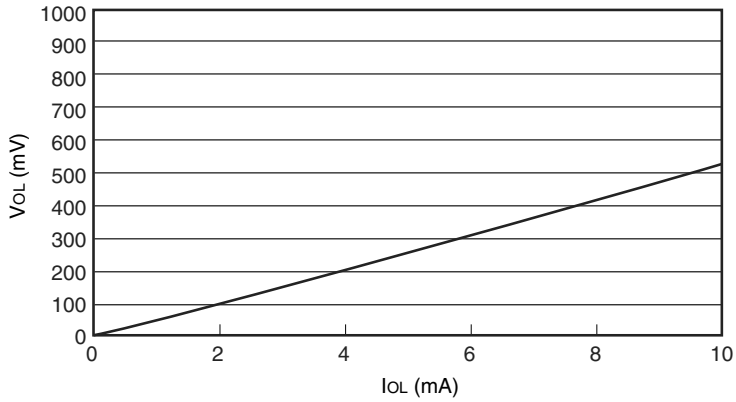
(V_{CC} - V_{OH}) – I_{OH}

T_A = +25 °C, V_{CC} = 4.5 V



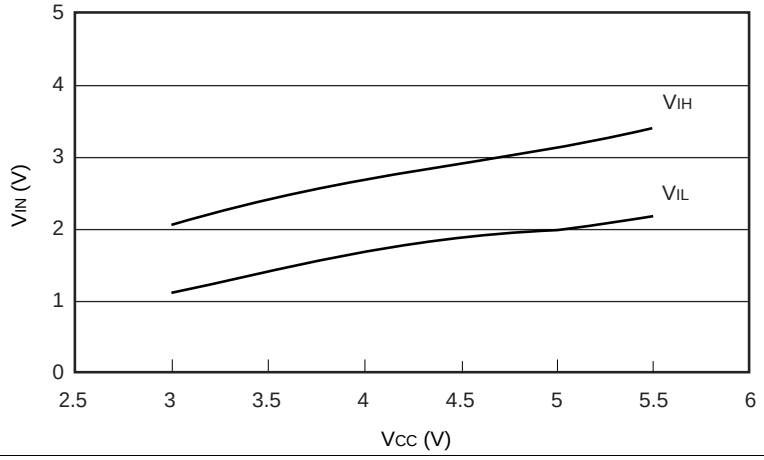
V_{OL} – I_{OL}

T_A = +25 °C, V_{CC} = 4.5 V



H level input voltage/ L level input voltage
V_{IN} – V_{CC}

T_A = +25 °C



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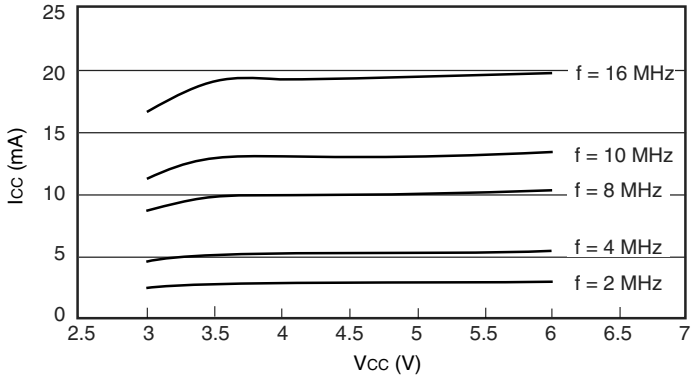
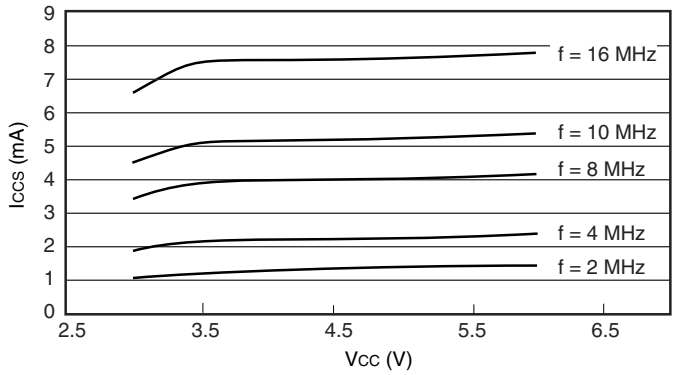
I_{CC} – V_{CC}

T_A = +25 °C, In external clock operation
f = Internal operating frequency



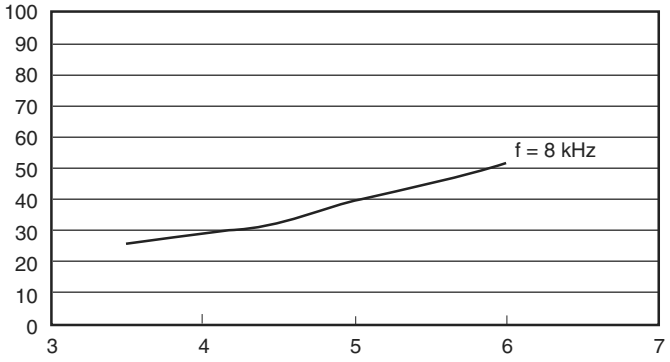
I_{CCS} – V_{CC}

T_A = +25 °C, In external clock operation
f = Internal operating frequency



I_{CCL} – V_{CC}

T_A = +25 °C, In external clock operation
f = Internal operating frequency



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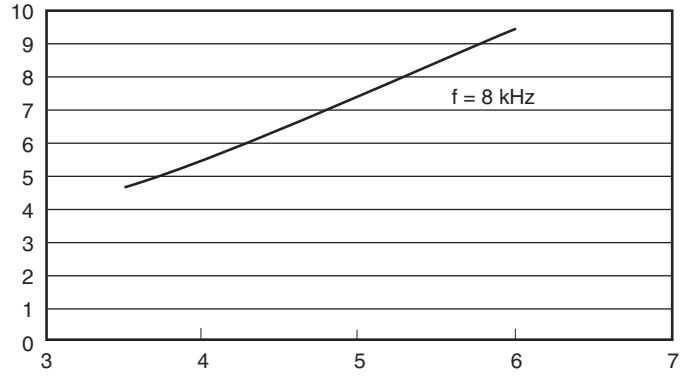
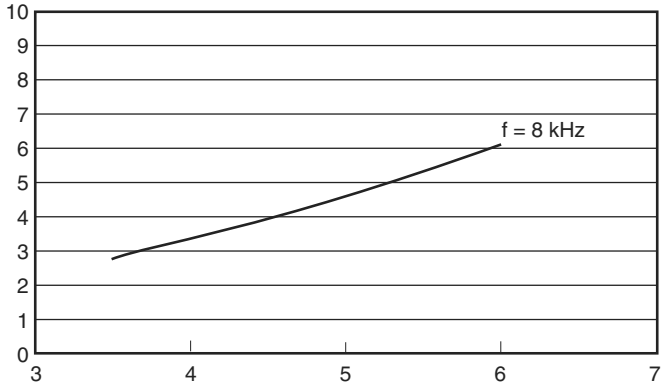
I_{CCLS} – V_{CC}

T_A = +25 °C, In external clock operation
f = Internal operating frequency



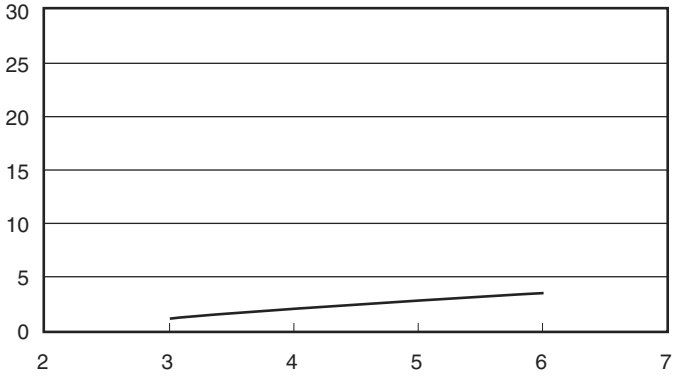
I_{CCT} – V_{CC}

T_A = +25 °C, In external clock operation
f = Internal operating frequency



I_{CCH} – V_{CC}

Stopping, T_A = +25 °C



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