Infineon Technologies - MB90387SPMT-GS-331E1 Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, SCI, UART/USART
Peripherals	POR, WDT
Number of I/O	36
Program Memory Size	64KB (64K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90387spmt-gs-331e1

MB90387/387S/F387/F387S
MB90V495G

16-bit Microcontrollers
F²MC-16LX MB90385 Series

MB90385 series devices are general-purpose high-performance 16-bit micro controllers designed for process control of consumer products, which require high-speed real-time processing. The devices of this series have the built-in full-CAN interface.
The system, inheriting the architecture of F²MC family, employs additional instruction ready for high-level languages, expanded addressing mode, enhanced multiply-divide instructions, and enriched bit-processing instructions. Furthermore, employment of 32-bit accumulator achieves processing of long-word data (32 bits).
The peripheral resources of MB90385 series include the following:
8/10-bit A/D converter, UART (SCI), 8/16-bit PPG timer, 16-bit input-output timer (16-bit free-run timer, input capture 0, 1, 2, 3 (ICU)), and CAN controller.

Features

Clock

- Built-in PLL clock frequency multiplication circuit
- Selection of machine clocks (PLL clocks) is allowed among frequency division by two on oscillation clock, and multiplication of 1 to 4 times of oscillation clock (for 4-MHz oscillation clock, 4 MHz to 16 MHz).
- Operation by sub-clock (8.192 kHz) is allowed. (MB90387, MB90F387)
- Minimum execution time of instruction: 62.5 ns (when operating with 4-MHz oscillation clock, and 4-time multiplied PLL clock).

16 Mbyte CPU memory Space

- 24-bit internal addressing

Instruction System Best Suited to Controller

- Wide choice of data types (bit, byte, word, and long word)
- Wide choice of addressing modes (23 types)
- Enhanced multiply-divide instructions and RETI instructions
- Enhanced high-precision computing with 32-bit accumulator

Instruction System Compatible with High-level Language (C language) and Multitask

- Employing system stack pointer
- Enhanced various pointer indirect instructions
- Barrel shift instructions

Increased Processing Speed

- 4-byte instruction queue

Powerful Interrupt Function with 8 Levels and 34 Factors

Automatic Data Transfer Function Independent of CPU

- Expanded intelligent I/O service function (EI² OS): Maximum of 16 channels

Low Power Consumption (standby) Mode

- Sleep mode (a mode that halts CPU operating clock)
- Time-base timer mode (a mode that operates oscillation clock, sub clock, time-base timer and watch timer only)
- Watch mode (a mode that operates sub clock and watch timer only)
- Stop mode (a mode that stops oscillation clock and sub clock)
- CPU blocking operation mode

Process

- CMOS technology

I/O Port

- General-purpose input/output port (CMOS output):

  MB90387, MB90F387: 34 ports (including 4 high-current output ports)
  MB90387S, MB90F387S: 36 ports (including 4 high-current output ports)

Timer

- Time-base timer, watch timer, watchdog timer: 1 channel
- 8/16-bit PPG timer: 8-bit x 4 channels, or 16-bit x 2 channels
- 16-bit reload timer: 2 channels
- 16-bit input/output timer
  - ❒ 16-bit free run timer: 1 channel
  - ❒ 16-bit input capture: (ICU): 4 channels

  Interrupt request is issued upon latching a count value of 16-bit free run timer by detection of an edge on pin input.

CAN Controller: 1 channel

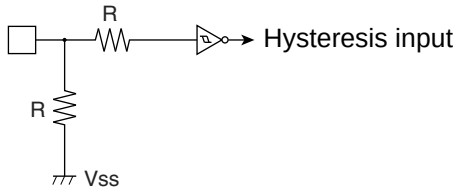
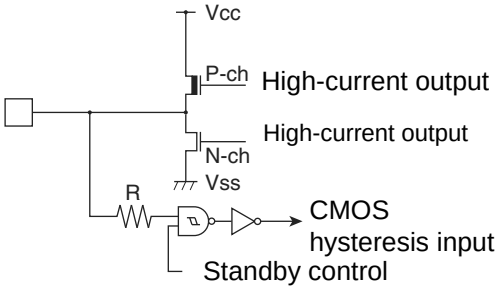
- Compliant with Ver2.0A and Ver2.0B CAN specifications
- 8 built-in message buffers
- Transmission rate of 10 kbps to 1 Mbps (by 16 MHz machine clock)
- CAN wake-up

UART (SCI): 1 channel

- Equipped with full-duplex double buffer
- Clock-asynchronous or clock-synchronous serial transmission is available.

Pin No.	Pin Name	Circuit Type	Function
39	P42	D	General-purpose input/output port.
	SOT1		Serial data input pin for UART. Valid only when serial data input/output setting on UART is “enabled.”
40	P43	D	General-purpose input/output port.
	TX		Transmission output pin for CAN. Valid only when output setting is “enabled.”
41	P44	D	General-purpose input/output port.
	RX		Transmission output pin for CAN. Valid only when output setting is “enabled.”
42 to 45	P30 to P33	D	General-purpose input/output ports.
46	X0A*	A	Pin for low-rate oscillation.
	P35*		General-purpose input/output port.
47	X1A*	A	Pin for low-rate oscillation.
	P36*		General-purpose input/output port.
48	AVss	–	Vss power source input pin for A/D converter.

*: MB90387, MB90F387: X1A, X0A
MB90387S, MB90F387S: P36, P35

Type	Circuit	Remarks
F		■ Hysteresis input with pull-down resistor ■ Pull-down resistor, approx. 50 kΩ ■ Flash product is not provided with pull-down resistor.
G		■ CMOS hysteresis input ■ CMOS level output (high-current output) ■ Standby control provided

7. Handling Devices

Do Not Exceed Maximum Rating (preventing “latch up”)

■ On a CMOS IC, latch-up may occur when applying a voltage higher than Vcc or a voltage lower than Vss to input or output pin, which has no middle or high withstand voltage. Latch-up may also occur when a voltage exceeding maximum rating is applied across Vcc pin and Vss pin.

■ Latch-up causes drastic increase of power current, which may lead to destruction of elements by heat. Extreme caution must be taken not to exceed maximum rating.

■ When turning on and off analog power source, take extra care not to apply an analog power voltages (AVcc and AVR) and analog input voltage that are higher than digital power voltage (Vcc).

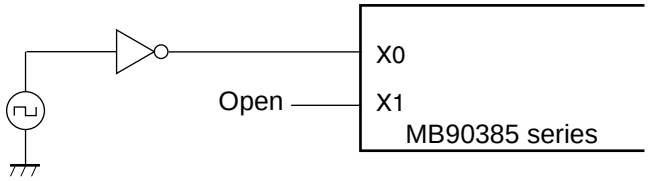
Handling Unused Pins

■ Leaving unused input pins open may cause permanent destruction by malfunction or latch-up. Apply pull-up or pull-down process to the unused pins using resistors of 2 kΩ or higher. Leave unused input/output pins open under output status, or process as input pins if they are under input status.

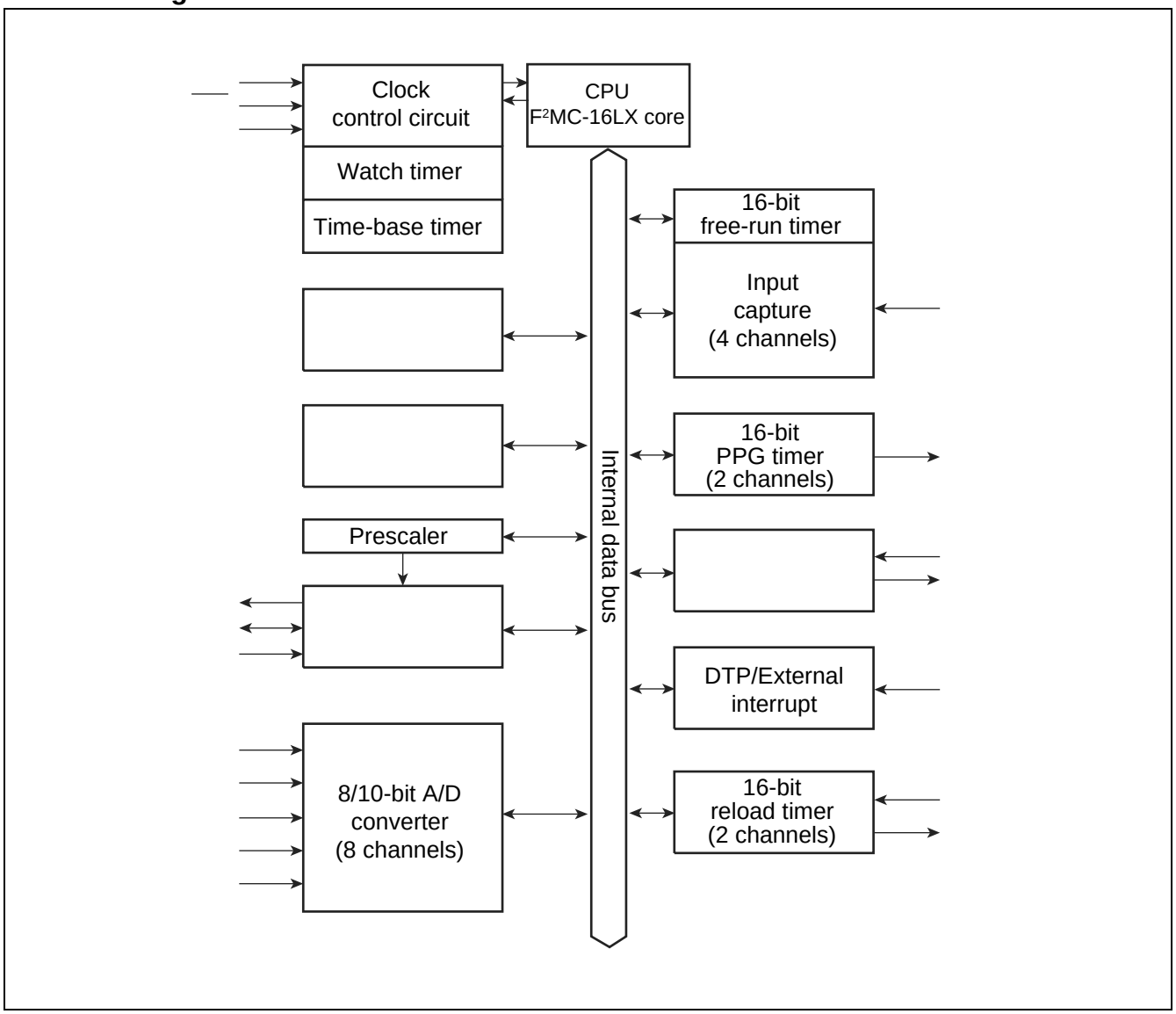
Using External Clock

■ When using an external clock, drive only X0 pin and leave X1 pin open. An example of using an external clock is shown below.

• Using external clock



8. Block Diagram



9. Memory Map

MB90385 series allows specifying a memory access mode “single chip mode.”

9.1 Memory Allocation of MB90385

MB90385 series model has 24-bit wide internal address bus and up to 24-bit bus of external address bus.
A maximum of 16-Mbyte memory space of external access memory is accessible.

Interrupt Source	EI²OS Readiness	Interrupt Vector			Interrupt Control Register		Priority*3
		Number		Address	ICR	Address	
UART1 reception completed	◎	#37	25H	FFFF68H	ICR13	0000BDH*1	High
UART1 transmission completed	Δ	#38	26H	FFFF64H			↑
Reserved	×	#39	27H	FFFF60H	ICR14	0000BEH*1	
Reserved	×	#40	28H	FFFF5CH			
Flash memory	×	#41	29H	FFFF58H	ICR15	0000BFH*1	↓
Delay interrupt generation module	×	#42	2AH	FFFF54H			Low

○ : Available

× : Unavailable

◎ : Available EI²OS function is provided.

Δ: Available when a cause of interrupt sharing a same ICR is not used.

*1:

- ❒ Peripheral functions sharing an ICR register have the same interrupt level.
- ❒ If peripheral functions share an ICR register, only one function is available when using expanded intelligent I/O service.
- ❒ If peripheral functions share an ICR register, a function using expanded intelligent I/O service does not allow interrupt by another function.

*2: Input capture 1 corresponds to EI²OS, however, PPG does not. When using EI²OS by input capture 1, interrupt should be disabled for PPG.

*3:Priority when two or more interrupts of a same level occur simultaneously.

12. Peripheral Resources

12.1 I/O Ports

The I/O ports are used as general-purpose input/output ports (parallel I/O ports). The MB60385 series model is provided with 5 ports (34 inputs). The ports function as input/output pins for peripheral functions also.

I/O Port Functions

An I/O port, using port data resister (PDR), outputs the output data to I/O pin and input a signal input to I/O port. The port direction register (DDR) specifies direction of input/output of I/O pins on a bit-by-bit basis.

The following summarizes functions of the ports and sharing peripheral functions:

■ Port 1: General-purpose input/output port, used also for PPG timer output and input capture inputs.

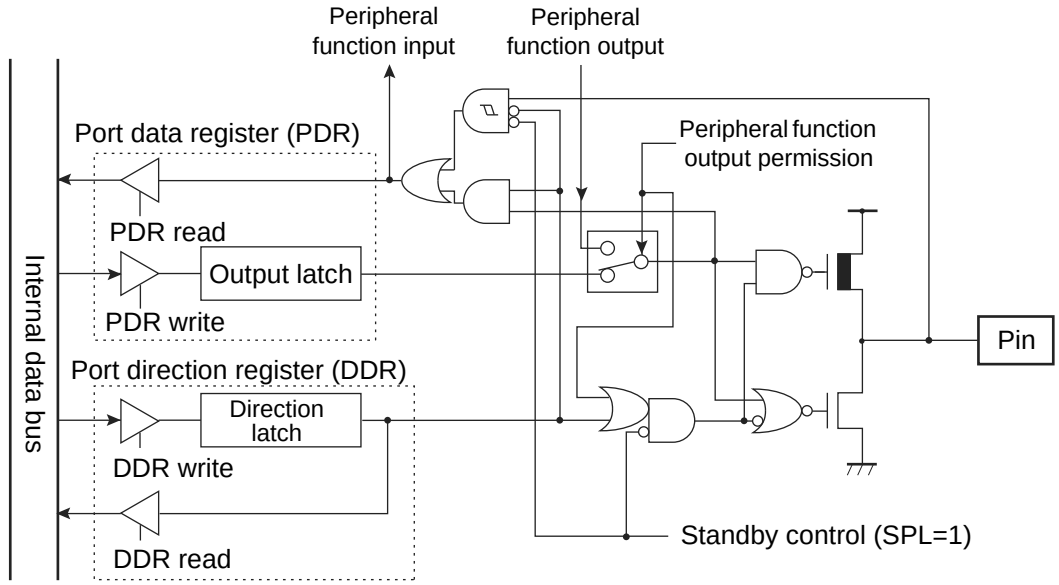
■ Port 2: General-purpose input/output port, used also for reload timer input/output and external interrupt input.

■ Port 3: General-purpose input/output port, used also for A/D converter activation trigger pin.

■ Port 4: General-purpose input/output port, used also for UART input/output and CAN controller send/receive pin.

■ Port 5: General-purpose input/output port, used also analog input pin.

Port 1 Pins Block Diagram (single-chip mode)



Standby control: Control among Stop mode (SPL=1), Time-base timer mode (SPL=1), and watch mode (SPL=1).

Port 1 Registers (single-chip mode)

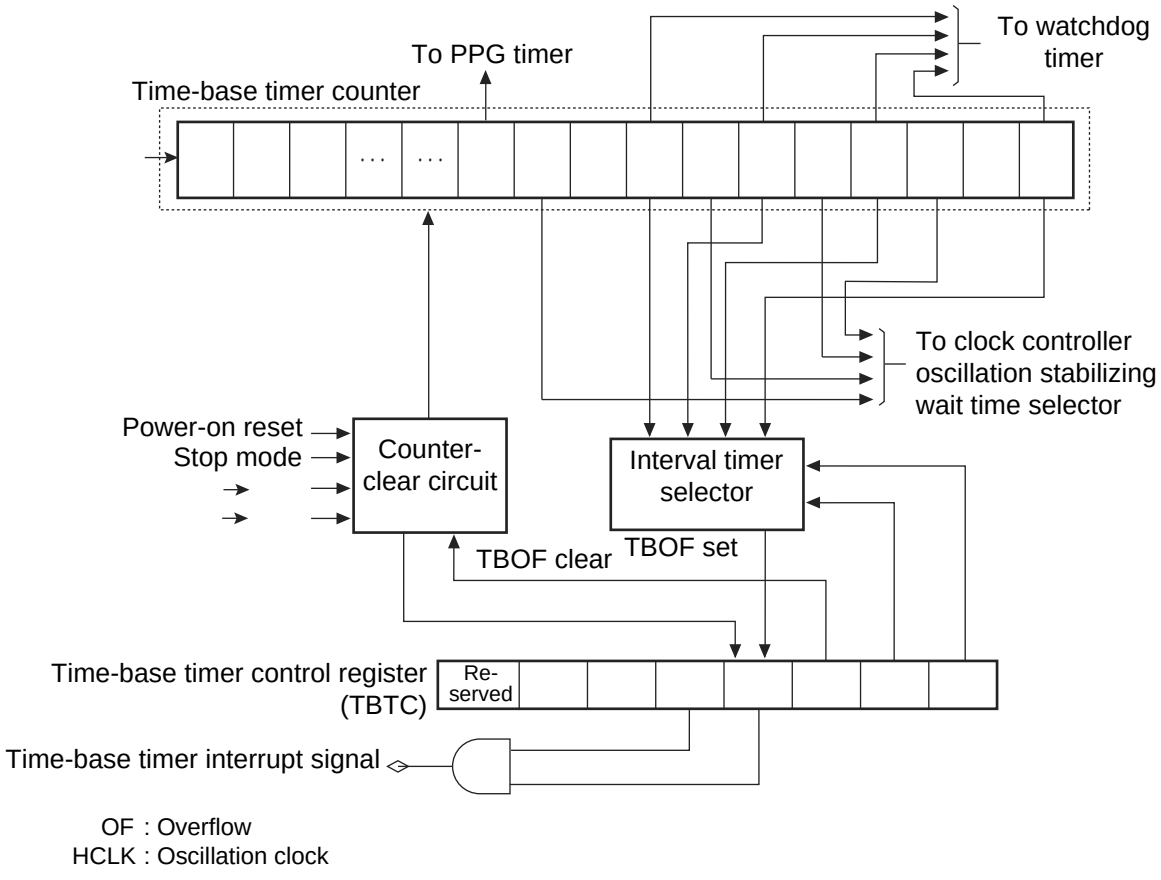
■ Port 1 registers include port 1 data register (PDR1) and port 1 direction register (DDR1).

■ The bits configuring the register correspond to port 1 pins on a one-to-one basis.

Relation between Port 1 Registers and Pins

Port Name	Bits of Register and Corresponding Pins								
Port 1	PDR1, DDR1	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	Corresponding pins	P17	P16	P15	P14	P13	P12	P11	P10

Time-base Timer Block Diagram



OF : Overflow
HCLK : Oscillation clock

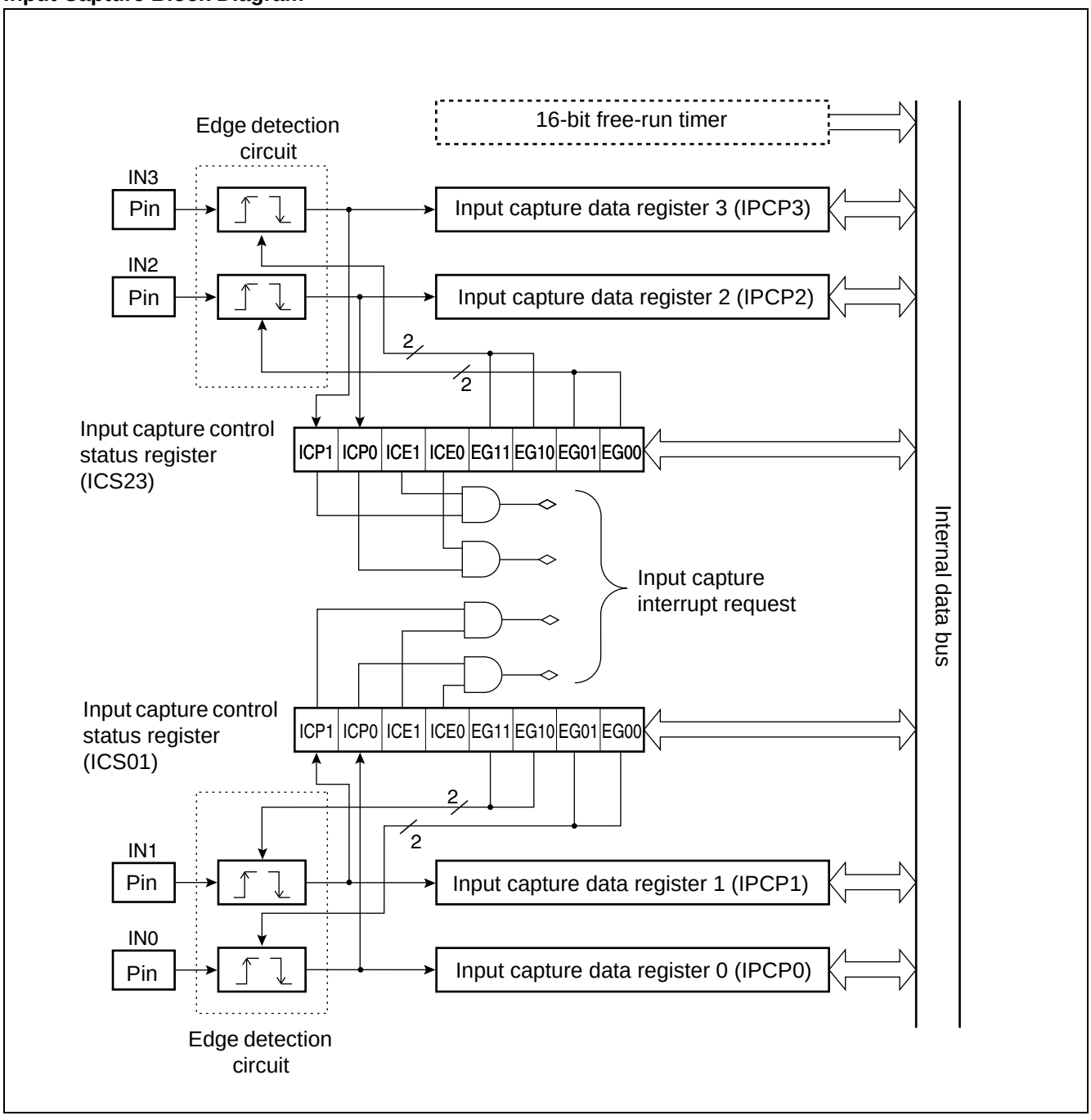
*1: Switch machine clock from main clock to PLL clock.

*2: Switch machine clock from sub clock to main clock.

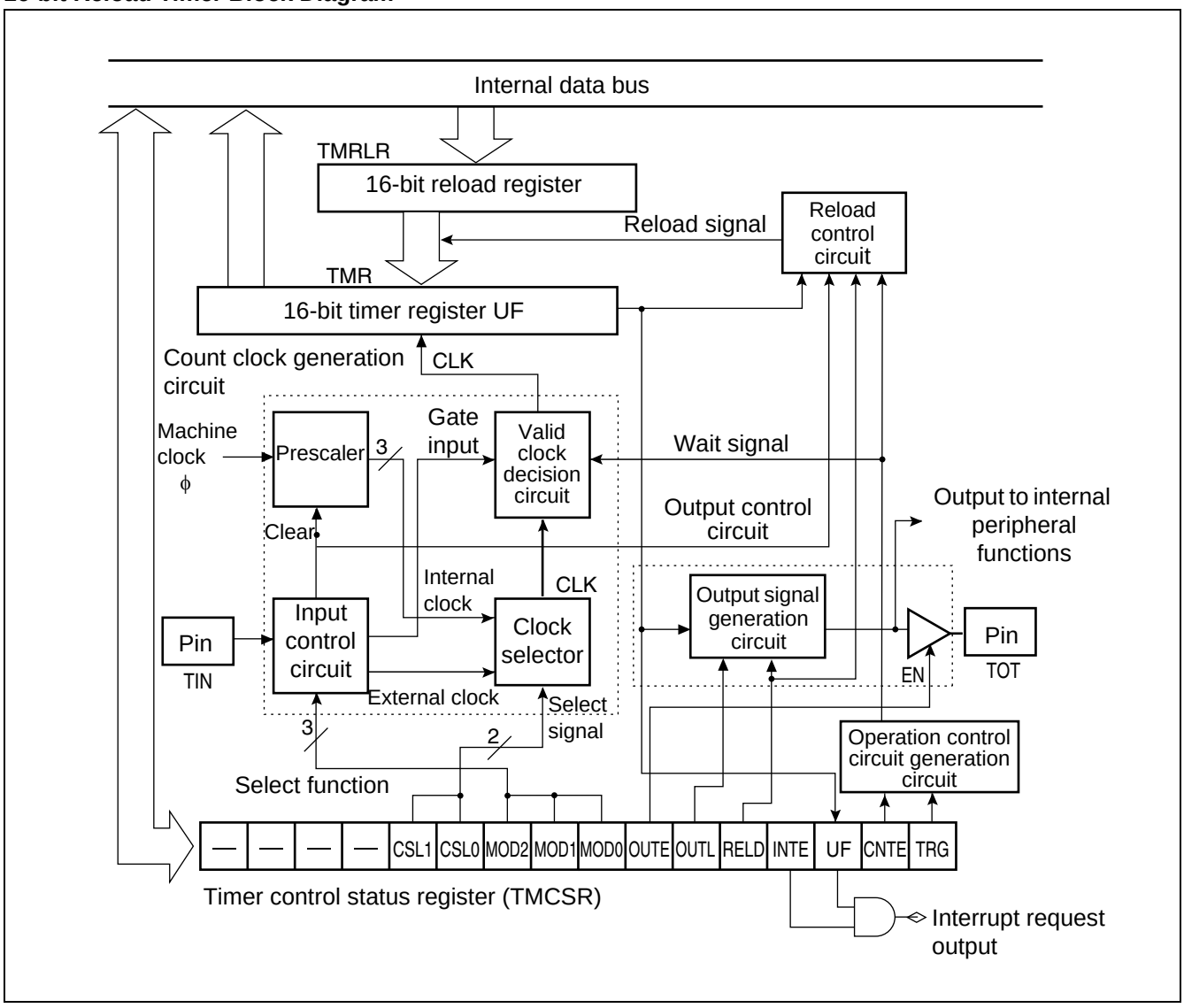
Actual interrupt request number of time-base timer is as follows:

Interrupt request number: #16 (10_H)

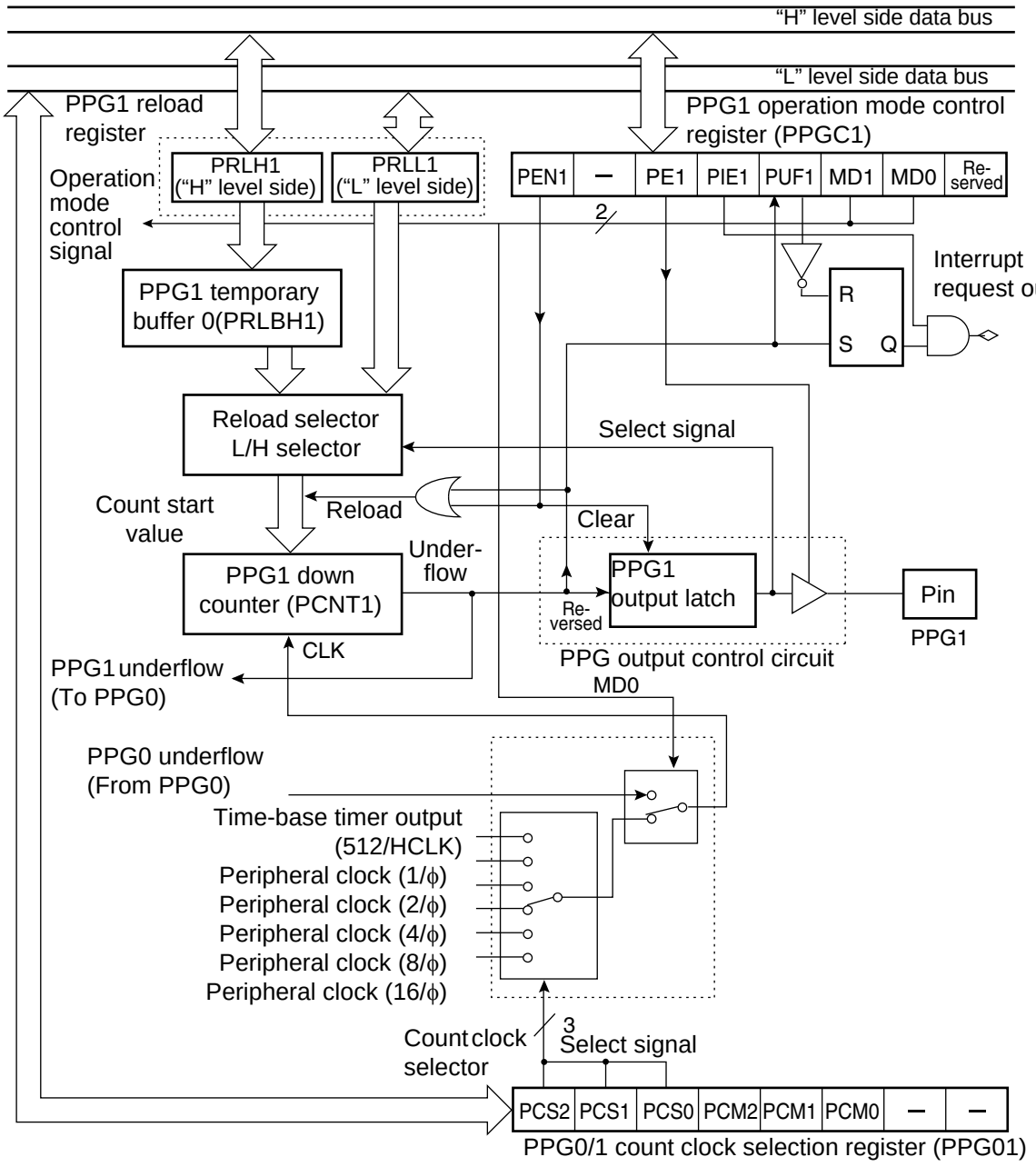
Input Capture Block Diagram



16-bit Reload Timer Block Diagram



8/16-bit PPG Timer 1 Block Diagram



– : Undefined
Reserved: Reserved bit
HCLK : Oscillation clock frequency
ϕ : Machine clock frequency
* : Interrupt output of 8/16-bit PPG timer 1 is incorporated into one by the OR circuit against interrupt output of 8/16-bit PPG timer 0.

12.12 CAN Controller

The Controller Area Network (CAN) is a serial communication protocol compliant with CANVer2.0A and Ver2.0B. The protocol allows data transmission and reception in both standard frame format and expanded frame format.

Features of CAN Controller

- CAN controller format is compliant with CANVer2.0A and Ver2.0B.
- The protocol allows data transmission and reception in standard frame format and expanded frame format.
- Automatic transmission of data frame by remote frame reception is allowed.
- Baud rate ranges from 10 kbps to 1 Mbps (with 16-MHz machine clock).

Table 12-5. Data Transmission Baud Rate

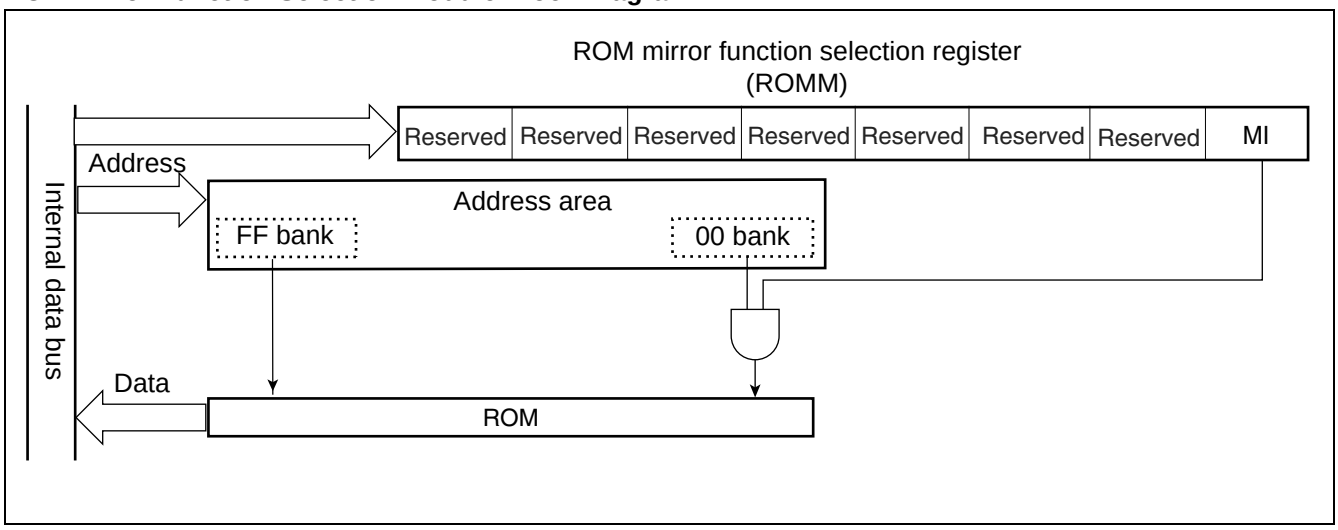
Machine Clock	Baud Rate (Max)
16 MHz	1 Mbps
12 MHz	1 Mbps
8 MHz	1 Mbps
4 MHz	500 kbps
2 MHz	250 kbps

- Provided with 8 transmission/reception message buffers.
- Transmission/reception is allowed at ID 11 bit in standard format, and at ID 29 bit in expanded frame format.
- Specifying 0 byte to 8 bytes is allowed in message data.
- Multi-level message buffer configuration is allowed.
- CAN controller has two built-in acceptance masks. Mask settings are independently allowed for the two acceptance masks on reception IDs.
- The two acceptance masks allow reception in standard frame format and expanded frame format.
- For types of masking, all-bit comparison, all-bit masking, and partial masking with acceptance mask register 0/1, are specifiable.

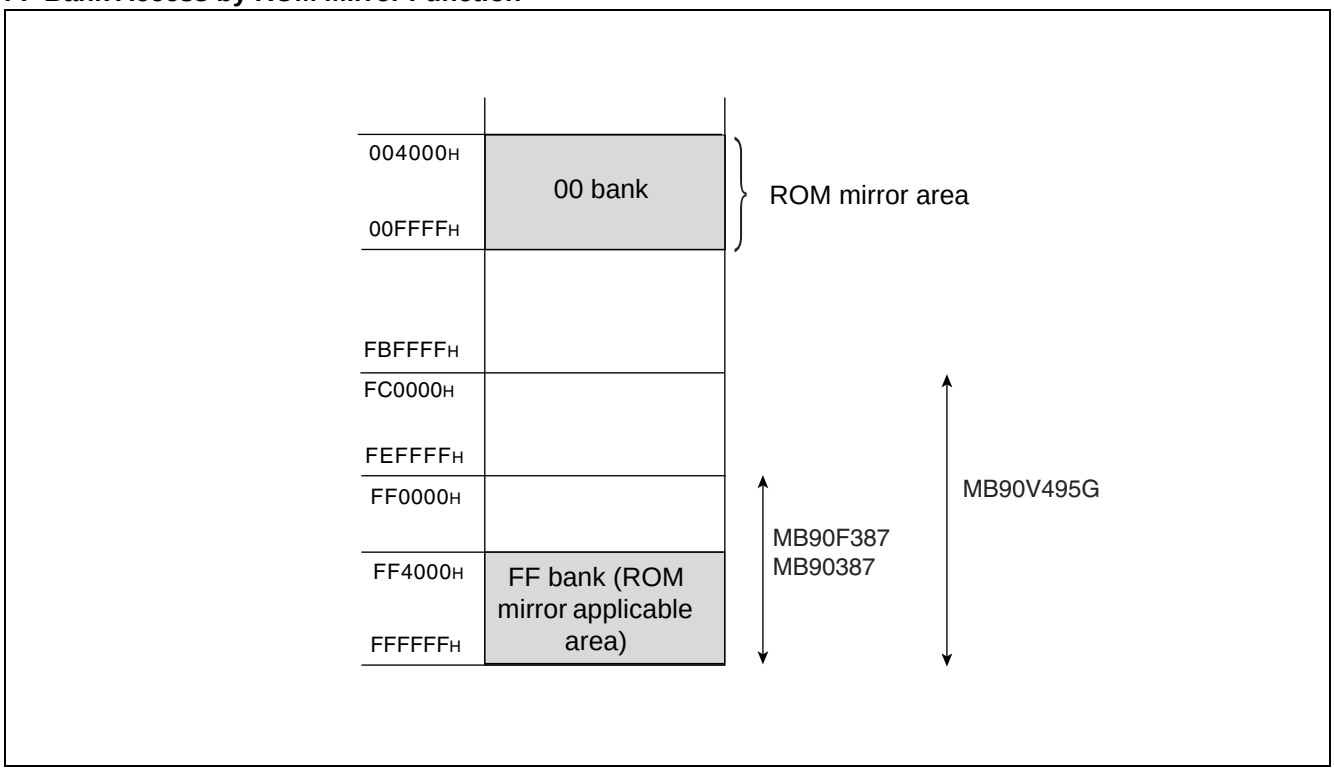
12.14 ROM Mirror Function Selection Module Outline

The ROM mirror function selection module sets the data in ROM assigned to FF bank so that the data is read by access to 00 bank.

ROM Mirror Function Selection Module Block Diagram



FF Bank Access by ROM Mirror Function



Sector Configuration of 512 Kbit Flash Memory

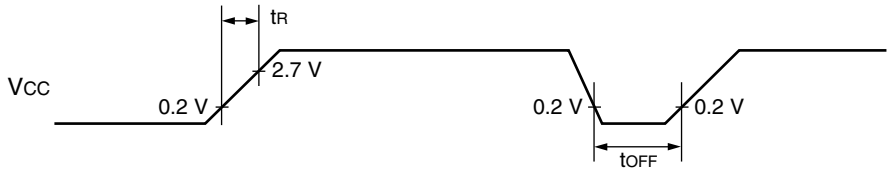
Flash memory	CPU address	Writer address*
SA0 (32 Kbytes)	FF0000H FF7FFFH	70000H 77FFFH
SA1 (8 Kbytes)	FF8000H FF9FFFH	78000H 79FFFH
SA2 (8 Kbytes)	FFA000H FFBFFFH	7A000H 7BFFFH
SA3 (16 Kbytes)	FFC000H FFFFFFH	7C000H 7FFFFH

*: “Writer address” is an address equivalent to CPU address, which is used when data is written on Flash memory, using parallel writer. When writing/deleting data with general-purpose writer, the writer address is used for writing and deleting.

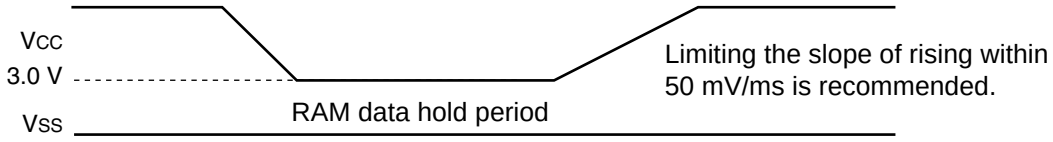
13.4.3 Power-on Reset

(V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

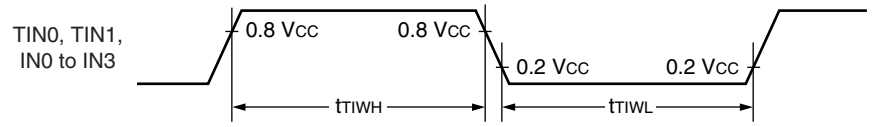
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Power supply rise time	t_R	V_{CC}	–	0.05	30	ms	
Power supply shutdown time	t_{OFF}	V_{CC}		1	–	ms	Waiting time until power-on



Sudden change of power supply voltage may activate the power-on reset function. When changing power supply voltages during operation, raise the power smoothly by suppressing variation of voltages as shown below. When raising the power, do not use PLL clock. However, if voltage drop is 1V/s or less, use of PLL clock is allowed during operation.



• Timer input timing



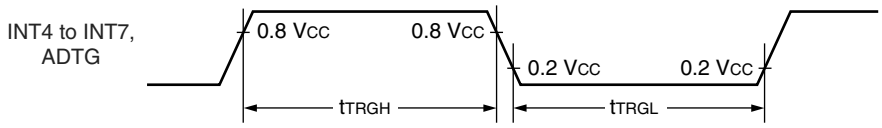
13.4.6 Trigger Input Timing

(V_{CC} = 4.5 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH} t_{TRGL}	INT4 to INT7, ADTG	–	5 t_{CP} *	–	ns	

*: Refer to Clock Timing ratings for t_{CP} (internal operation clock cycle time).

• Trigger input timing



13.5 A/D Converter

(V_{CC} = AV_{CC} = 4.0 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, 3.0 V ≤ AVR − AV_{SS}, T_A = −40 °C to +105 °C)

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	–	–	–	–	10	bit	
Total error	–	–	–	–	± 3.0	LSB	
Nonlinear error	–	–	–	–	± 2.5	LSB	
Differential linear error	–	–	–	–	± 1.9	LSB	
Zero transition voltage	V_{OT}	AN0 to AN7	AV_{SS} − 1.5 LSB	AV_{SS} + 0.5 LSB	AV_{SS} + 2.5 LSB	V	1 LSB = (AVR − AV_{SS}) / 1024
Full-scale transition voltage	V_{FST}	AN0 to AN7	AVR − 3.5 LSB	AVR − 1.5 LSB	AVR + 0.5 LSB	V	
Compare time	–	–	66 t_{CP} *1	–	–	ns	With 16 MHz machine clock 5.5 V ≥ AV_{CC} ≥ 4.5 V
			88 t_{CP} *1	–	–	ns	With 16 MHz machine clock 4.5 V > AV_{CC} ≥ 4.0 V
Sampling time	–	–	32 t_{CP} *1	–	–	ns	With 16 MHz machine clock 5.5 V ≥ AV_{CC} ≥ 4.5 V
			128 t_{CP} *1	–	–	ns	With 16 MHz machine clock 4.5 V > AV_{CC} ≥ 4.0 V
Analog port input current	I_{AIN}	AN0 to AN7	–	–	10	µA	
Analog input voltage	V_{AIN}	AN0 to AN7	AV_{SS}	–	AVR	V	
Reference voltage	–	AVR	AV_{SS} + 2.7	–	AV_{CC}	V	
Power supply current	I_A	AV_{CC}	–	3.5	7.5	mA	
	I_{AH}	AV_{CC}	–	–	5	µA	*2
Reference voltage supplying current	I_R	AVR	–	165	250	µA	
	I_{RH}	AVR	–	–	5	µA	*2
Variation among channels	–	AN0 to AN7	–	–	4	LSB	

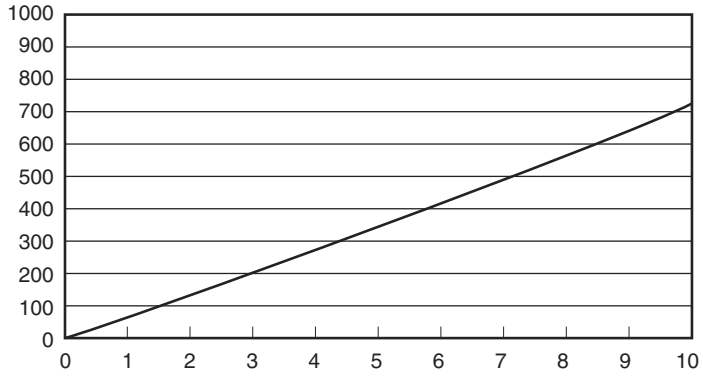
*1: Refer to Clock Timing on AC Characteristics.

*2: If A/D converter is not operating, a current when CPU is stopped is applicable (Vcc=AVcc=AVR=5.0 V).

(Continued)

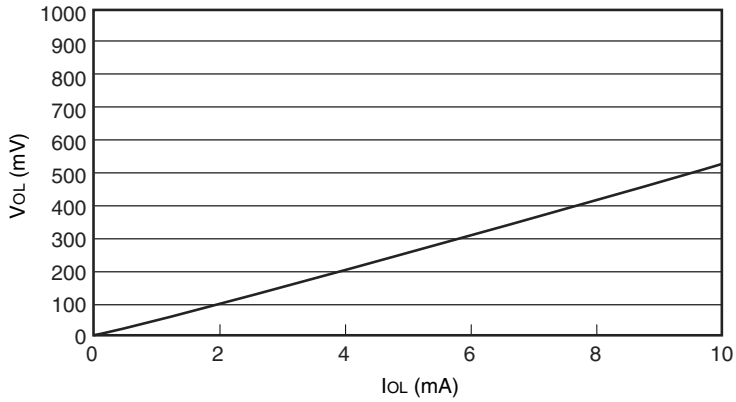
(V_{CC} - V_{OH}) – I_{OH}

T_A = +25 °C, V_{CC} = 4.5 V



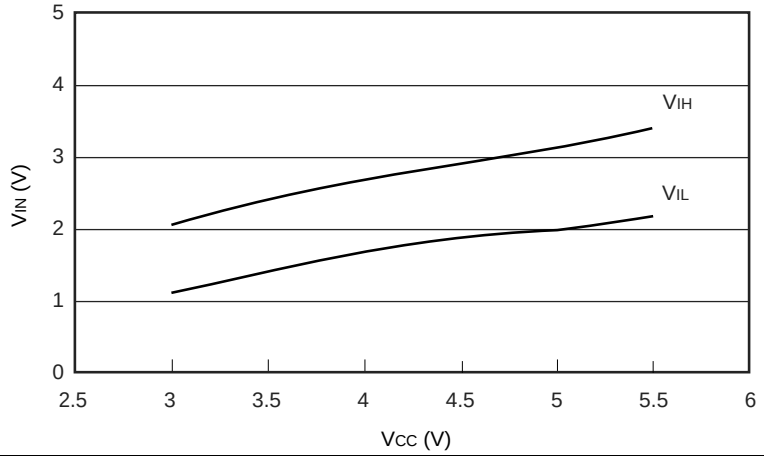
V_{OL} – I_{OL}

T_A = +25 °C, V_{CC} = 4.5 V



H level input voltage/ L level input voltage
V_{IN} – V_{CC}

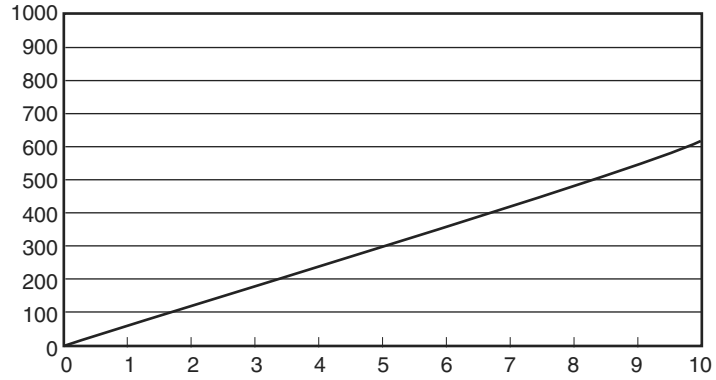
T_A = +25 °C



(Continued)

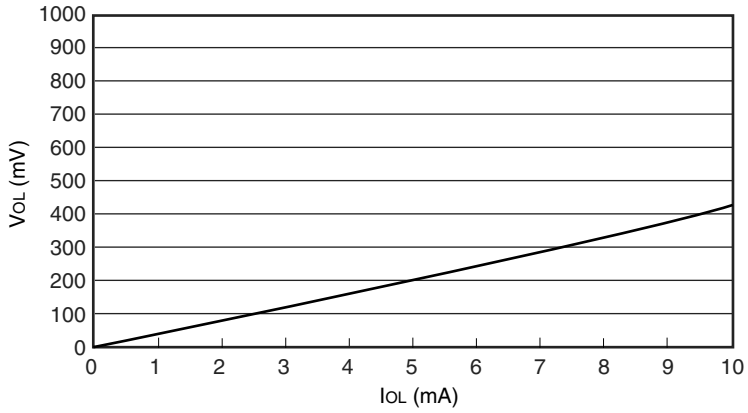
(V_{CC} - V_{OH}) – I_{OH}

T_A = +25 °C, V_{CC} = 4.5 V



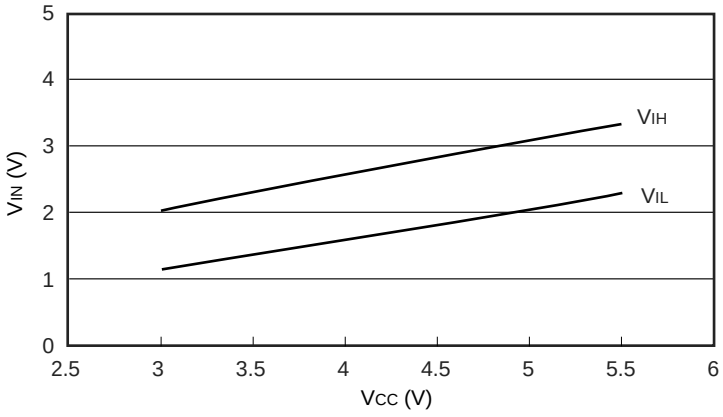
V_{OL} – I_{OL}

T_A = +25 °C, V_{CC} = 4.5 V



H level input voltage/ L level input voltage
V_{IN} – V_{CC}

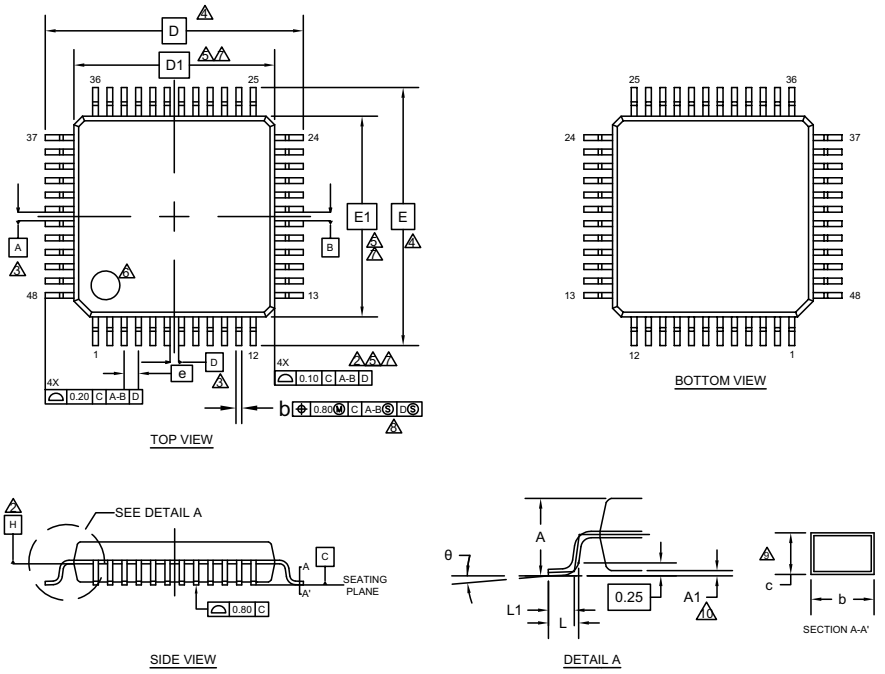
T_A = +25 °C



15. Ordering Information

Part Number	Package	Remarks
MB90F387PMT MB90387PMT MB90F387SPMT MB90387SPMT	48-pin plastic LQFP (LQA048)	

16. Package Dimension



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.00	—	0.20
b	0.15	—	0.27
c	0.09	—	0.20
D	9.00 BSC		
D1	7.00 BSC		
e	0.50 BSC		
E	9.00 BSC		
E1	7.00 BSC		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
θ	0°	—	8°

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-13731 **

PACKAGE OUTLINE, 48 LEAD LQFP
7.0X7.0X1.7 MM LQA048 REV**