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## Details

| | |
|---|---|
| Product Status | Active |
| Core Processor | F²MC-16LX |
| Core Size | 16-Bit |
| Speed | 16MHz |
| Connectivity | CANbus, SCI, UART/USART |
| Peripherals | POR, WDT |
| Number of I/O | 36 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | Mask ROM |
| EEPROM Size | - |
| RAM Size | 2K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3.5V ~ 5.5V |
| Data Converters | A/D 8x8/10b |
| Oscillator Type | External |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 48-LQFP |
| Supplier Device Package | 48-LQFP (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/mb90387spmt-gt-105 |

## 16-bit Microcontrollers
## F$^2$MC-16LX MB90385 Series

MB90385 series devices are general-purpose high-performance 16-bit micro controllers designed for process control of consumer products, which require high-speed real-time processing. The devices of this series have the built-in full-CAN interface.

The system, inheriting the architecture of F$^2$MC family, employs additional instruction ready for high-level languages, expanded addressing mode, enhanced multiply-divide instructions, and enriched bit-processing instructions. Furthermore, employment of 32-bit accumulator achieves processing of long-word data (32 bits).

The peripheral resources of MB90385 series include the following:

8/10-bit A/D converter, UART (SCI), 8/16-bit PPG timer, 16-bit input-output timer (16-bit free-run timer, input capture 0, 1, 2, 3 (ICU)), and CAN controller.

## Features

### Clock

■ Built-in PLL clock frequency multiplication circuit

■ Selection of machine clocks (PLL clocks) is allowed among frequency division by two on oscillation clock, and multiplication of 1 to 4 times of oscillation clock (for 4-MHz oscillation clock, 4 MHz to 16 MHz).

■ Operation by sub-clock (8.192 kHz) is allowed. (MB90387, MB90F387)

■ Minimum execution time of instruction: 62.5 ns (when operating with 4-MHz oscillation clock, and 4-time multiplied PLL clock).

### 16 Mbyte CPU memory Space

■ 24-bit internal addressing

### Instruction System Best Suited to Controller

■ Wide choice of data types (bit, byte, word, and long word)

■ Wide choice of addressing modes (23 types)

■ Enhanced multiply-divide instructions and RETI instructions

■ Enhanced high-precision computing with 32-bit accumulator

### Instruction System Compatible with High-level Language (C language) and Multitask

■ Employing system stack pointer

■ Enhanced various pointer indirect instructions

■ Barrel shift instructions

### Increased Processing Speed

■ 4-byte instruction queue

### Powerful Interrupt Function with 8 Levels and 34 Factors

### Automatic Data Transfer Function Independent of CPU

■ Expanded intelligent I/O service function (EI$^2$ OS): Maximum of 16 channels

### Low Power Consumption (standby) Mode

■ Sleep mode (a mode that halts CPU operating clock)

■ Time-base timer mode (a mode that operates oscillation clock, sub clock, time-base timer and watch timer only)

■ Watch mode (a mode that operates sub clock and watch timer only)

■ Stop mode (a mode that stops oscillation clock and sub clock)

■ CPU blocking operation mode

### Process

■ CMOS technology

### I/O Port

■ General-purpose input/output port (CMOS output):

MB90387, MB90F387: 34 ports (including 4 high-current output ports)
MB90387S, MB90F387S: 36 ports (including 4 high-current output ports)

### Timer

■ Time-base timer, watch timer, watchdog timer: 1 channel

■ 8/16-bit PPG timer: 8-bit x 4 channels, or 16-bit x 2 channels

■ 16-bit reload timer: 2 channels

■ 16-bit input/output timer
  ❑ 16-bit free run timer: 1 channel
  ❑ 16-bit input capture: (ICU): 4 channels

  Interrupt request is issued upon latching a count value of 16-bit free run timer by detection of an edge on pin input.

### CAN Controller: 1 channel

■ Compliant with Ver2.0A and Ver2.0B CAN specifications

■ 8 built-in message buffers

■ Transmission rate of 10 kbps to 1 Mbps (by 16 MHz machine clock)

■ CAN wake-up

### UART (SCI): 1 channel

■ Equipped with full-duplex double buffer

■ Clock-asynchronous or clock-synchronous serial transmission is available.

**DTP/External Interrupt: 4 channels, CAN wakeup: 1channel**

■ Module for activation of expanded intelligent I/O service (EI²OS), and generation of external interrupt.

**Delay Interrupt Generator Module**

■ Generates interrupt request for task switching.
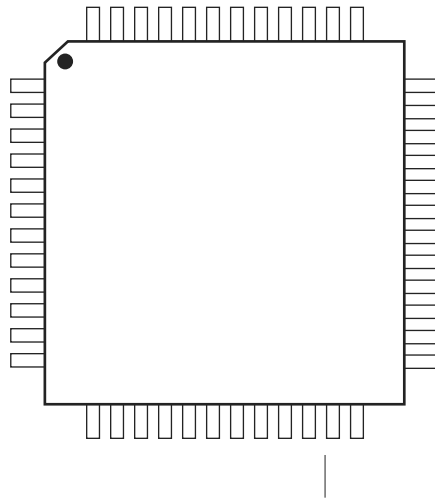
**8/10-bit A/D Converter: 8 channels**

■ Resolution is selectable between 8-bit and 10-bit.

■ Activation by external trigger input is allowed.

■ Conversion time: 6.125 $\mu$s (at 16 MHz machine clock, including sampling time)

**Program Patch Function**

■ Address matching detection for 2 address pointers.

## 4. Pin Assignment

(Top View)

(LQA048)

\*: MB90387, MB90F387     : X1A, X0A
   MB90387S, MB90F387S: P36, P35

## 11. Interrupt Sources, Interrupt Vectors, And Interrupt Control Registers

| Interrupt Source | EI²OS Readiness | Interrupt Vector | | Interrupt Control Register | | Priority*3 |
|---|---|---|---|---|---|---|
| | | Number | Address | ICR | Address | |
| Reset | × | #08 | 08H | FFFFDCH | – | – | High |
| INT 9 instruction | × | #09 | 09H | FFFFD8H | – | – | ↑ |
| Exceptional treatment | × | #10 | 0AH | FFFFD4H | – | – | |
| CAN controller reception completed (RX) | ´ | #11 | 0BH | FFFFD0H | ICR00 | 0000B0H*1 | |
| CAN controller transmission completed (TX) / Node status transition (NS) | ´ | #12 | 0CH | FFFFCCH | | | |
| Reserved | × | #13 | 0DH | FFFFC8H | ICR01 | 0000B1H | |
| Reserved | × | #14 | 0EH | FFFFC4H | | | |
| CAN wakeup | △ | #15 | 0FH | FFFFC0H | ICR02 | 0000B2H*1 | |
| Time-base timer | × | #16 | 10H | FFFFBCH | | | |
| 16-bit reload timer 0 | △ | #17 | 11H | FFFFB8H | ICR03 | 0000B3H*1 | |
| 8/10-bit A/D converter | △ | #18 | 12H | FFFFB4H | | | |
| 16-bit free-run timer overflow | △ | #19 | 13H | FFFFB0H | ICR04 | 0000B4H*1 | |
| Reserved | × | #20 | 14H | FFFFACH | | | |
| Reserved | × | #21 | 15H | FFFFA8H | ICR05 | 0000B5H*1 | |
| PPG timer ch0, ch1 underflow | ´ | #22 | 16H | FFFFA4H | | | |
| Input capture 0-input | △ | #23 | 17H | FFFFA0H | ICR06 | 0000B6H*1 | |
| External interrupt (INT4/INT5) | △ | #24 | 18H | FFFF9CH | | | |
| Input capture 1-input | △ | #25 | 19H | FFFF98H | ICR07 | 0000B7H*2 | |
| PPG timer ch2, ch3 underflow | ´ | #26 | 1AH | FFFF94H | | | |
| External interrupt (INT6/INT7) | △ | #27 | 1BH | FFFF90H | ICR08 | 0000B8H*1 | |
| Watch timer | △ | #28 | 1CH | FFFF8CH | | | |
| Reserved | × | #29 | 1DH | FFFF88H | ICR09 | 0000B9H*1 | |
| Input capture 2-input Input capture 3-input | ´ | #30 | 1EH | FFFF84H | | | |
| Reserved | × | #31 | 1FH | FFFF80H | ICR10 | 0000BAH*1 | |
| Reserved | × | #32 | 20H | FFFF7CH | | | |
| Reserved | × | #33 | 21H | FFFF78H | ICR11 | 0000BBH*1 | |
| Reserved | × | #34 | 22H | FFFF74H | | | |
| Reserved | × | #35 | 23H | FFFF70H | ICR12 | 0000BCH*1 | ↓ |
| 16-bit reload timer 1 | ○ | #36 | 24H | FFFF6CH | | | Low |

**Port 3 Pins Block Diagram (general-purpose input/output port)**



Standby control: Control among Stop mode (SPL=1), Time-base timer mode (SPL=1), and watch mode (SPL=1).
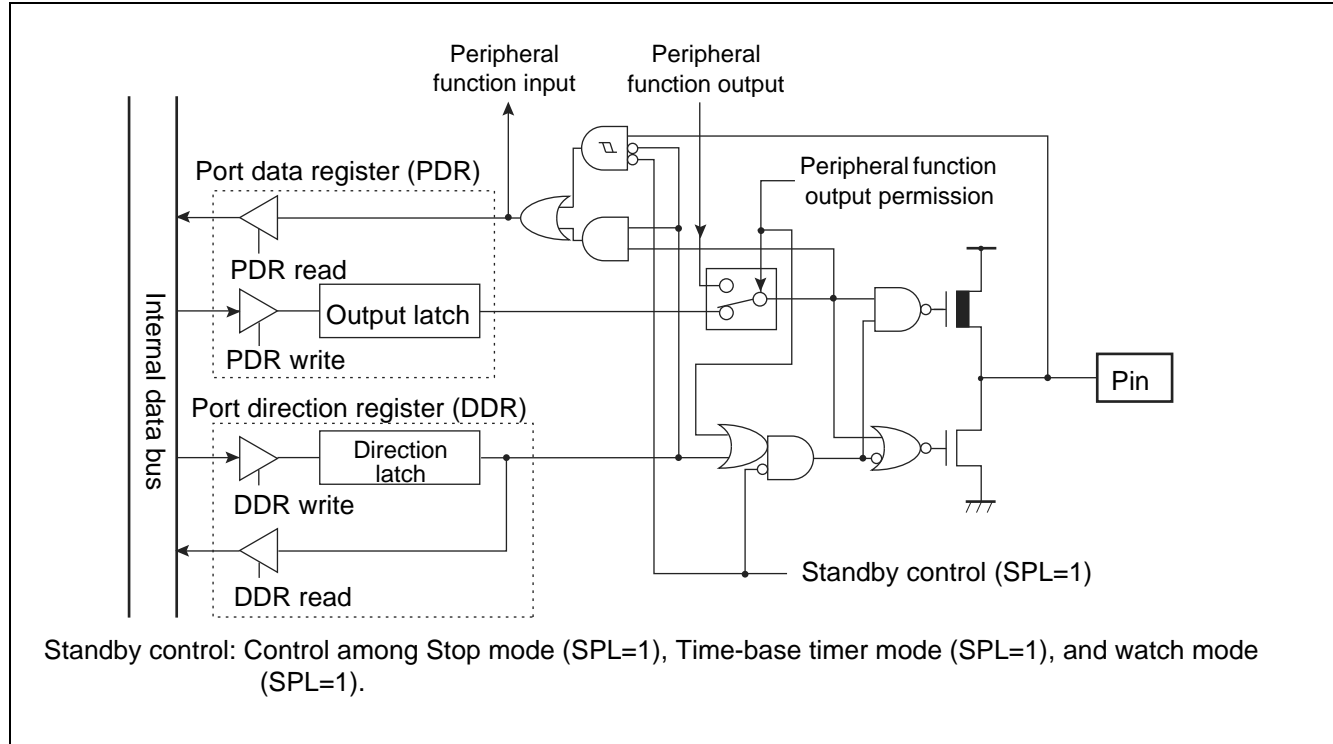
**Port 3 Registers**

■ Port 3 registers include port 3 data register (PDR3) and port 3 direction register (DDR3).

■ The bits configuring the register correspond to port 3 pins on a one-to-one basis.

**Relation between Port 3 Registers and Pins**

| Port Name | Bits of Register and Corresponding Pins | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Port 3 | PDR3, DDR3 | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
| | Corresponding pins | P37 | P36* | P35* | – | P33 | P32 | P31 | P30 |

*: P35 and P36 do not exist on MB90387and MB90F387.

### 12.3  Watchdog Timer

The watchdog timer is a 2-bit counter that uses time-base timer or watch timer as count clock. If the counter is not cleared within an interval time, CPU is reset.

### Watchdog Timer Functions

■ The watchdog timer is a timer counter that prevents runaway of a program. Once a watchdog timer is activated, the counter of watchdog timer must always be cleared within a specified time of interval. If specified interval time elapses without clearing the counter of a watchdog timer, CPU resetting occurs. This is the function of a watchdog timer.

■ The interval time of a watchdog timer is determined by a clock cycle, which is input as a count clock. Watchdog resetting occurs between a minimum time and a maximum time specified.

■ The output target of a clock source is specified by the watchdog clock selection bit (WTC: WDCS) in the watch timer control register.

■ Interval time of a watchdog timer is specified by the time-base timer output selection bit / watch timer output selection bit (WDTC: WT1, WT0) in the watchdog timer control register.

### Interval Timer of Watchdog Timer

| Min | Max | Clock Cycle | Min | Max | Clock Cycle |
|---|---|---|---|---|---|
| Approx. 3.58 ms | Approx. 4.61 ms | $(2^{14}\pm2^{11})$ /HCLK | Approx. 0.457 s | Approx. 0.576 s | $(2^{12}\pm2^{9})$ /SCLK |
| Approx. 14.33 ms | Approx. 18.3 ms | $(2^{16}\pm2^{13})$ /HCLK | Approx. 3.584 s | Approx. 4.608 s | $(2^{15}\pm2^{12})$ /SCLK |
| Approx. 57.23 ms | Approx. 73.73 ms | $(2^{18}\pm2^{15})$ /HCLK | Approx. 7.168 s | Approx. 9.216 s | $(2^{16}\pm2^{13})$ /SCLK |
| Approx. 458.75 ms | Approx. 589.82 ms | $(2^{21}\pm2^{18})$ /HCLK | Approx. 14.336 s | Approx. 18.432 s | $(2^{17}\pm2^{14})$ /SCLK |

HCLK: Oscillation clock (4 MHz), CSCLK: Sub clock (8.192 kHz)

Notes:

■ If the time-base timer is cleared when watchdog timer count clock is used as time base timer output (carry-over signal), watchdog reset time may become longer.

■ When using the sub clock as machine clock, be sure to specify watchdog timer clock source selection bit (WDCS) in watch timer control register (WTC) at "0," selecting output of watch timer.

**16-bit Reload Timer Block Diagram**
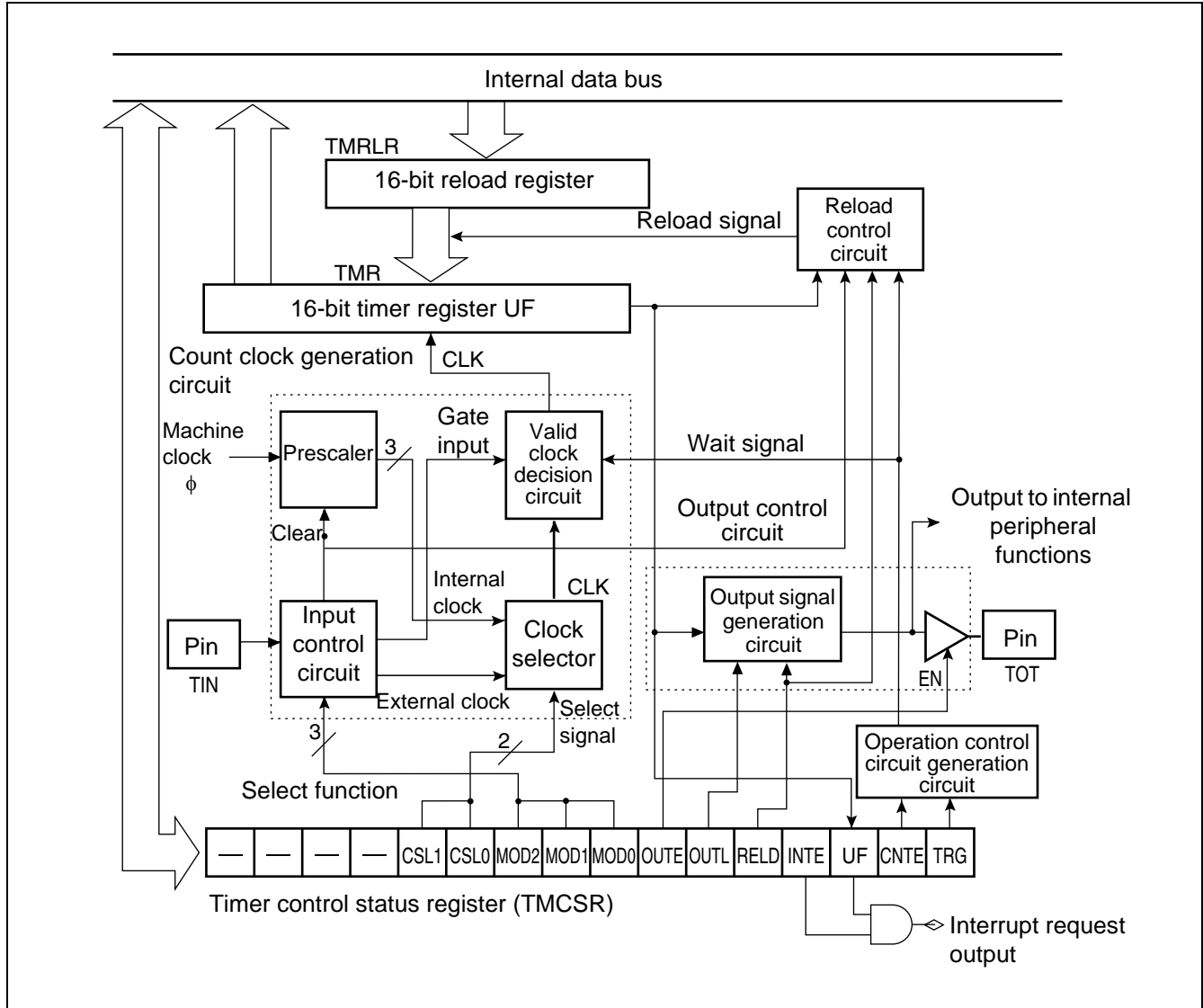
**Watch Timer Block Diagram**
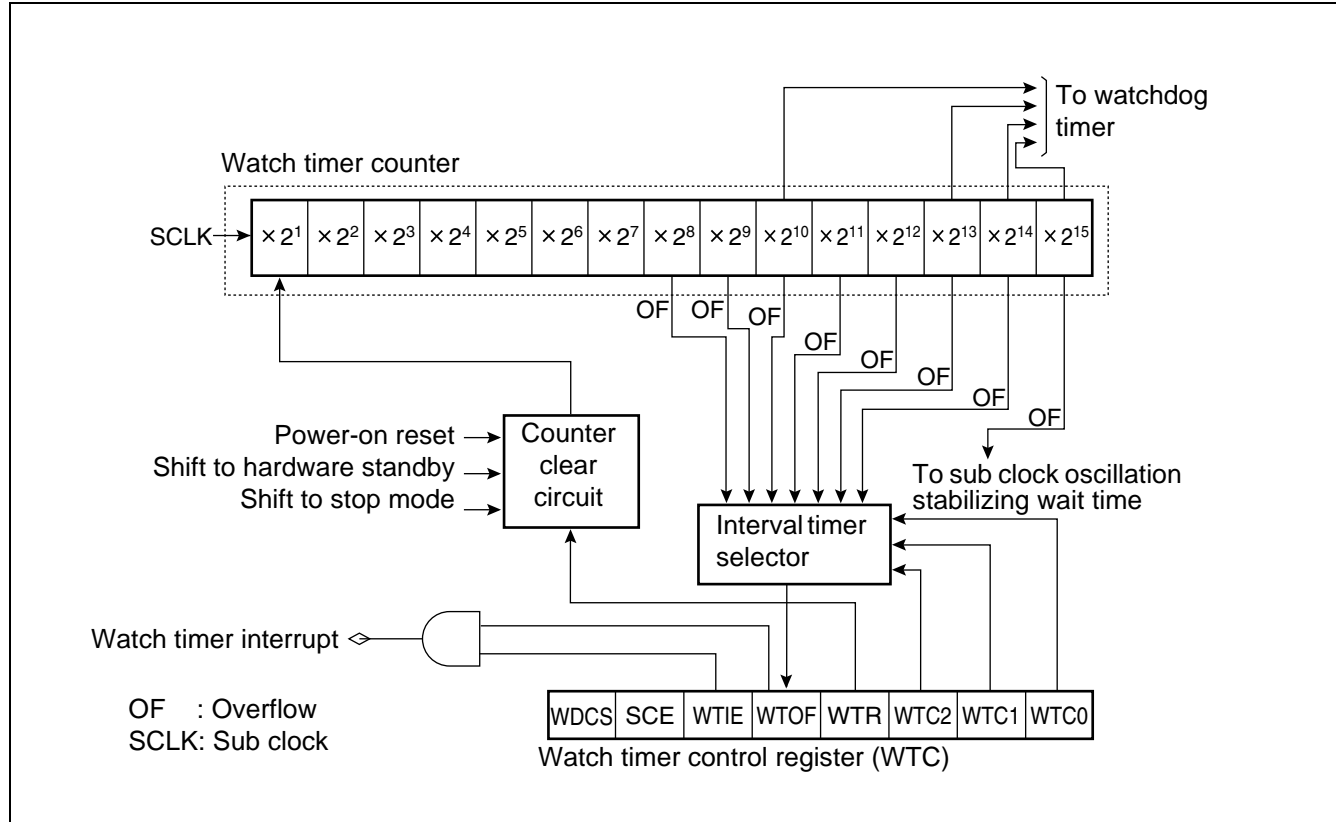


Actual interrupt request number of watch timer is as follows:

Interrupt request number: #28 (1C$_H$)

**Watch Timer Counter**

A 15-bit up counter that uses sub clock (SCLK) as a count clock.

**Counter Clear Circuit**

A circuit that clears the watch timer counter.

## 12.8  Delay Interrupt Generation Module Outline

The delay interrupt generation module is a module that generates interrupts for switching tasks. Generation of a hardware interrupt request is performed by software.

### Delay Interrupt Generation Module Outline

Using the delay interrupt generation module, hardware interrupt request is generated and released by software.

**Table 12-1.  Delay Interrupt Generation Module Outline**

| | **Function and Control** |
|---|---|
| Cause of interrupt | Set "1" in R0 bit of delay interrupt request generation/release register (DIRR: R0=1), generating an interrupt request.<br>Set "0" in R0 bit of delay interrupt request generation/release register (DIRR: R0=0), releasing an interrupt request. |
| Interrupt number | #42 (2A$_H$) |
| Interrupt control | No setting of permission register is provided. |
| Interrupt flag | Retained in DIRR: R0 bit |
| EI²OS | Not ready for expanded intelligent I/O service. |

### Delay Interrupt Generation Module Block Diagram
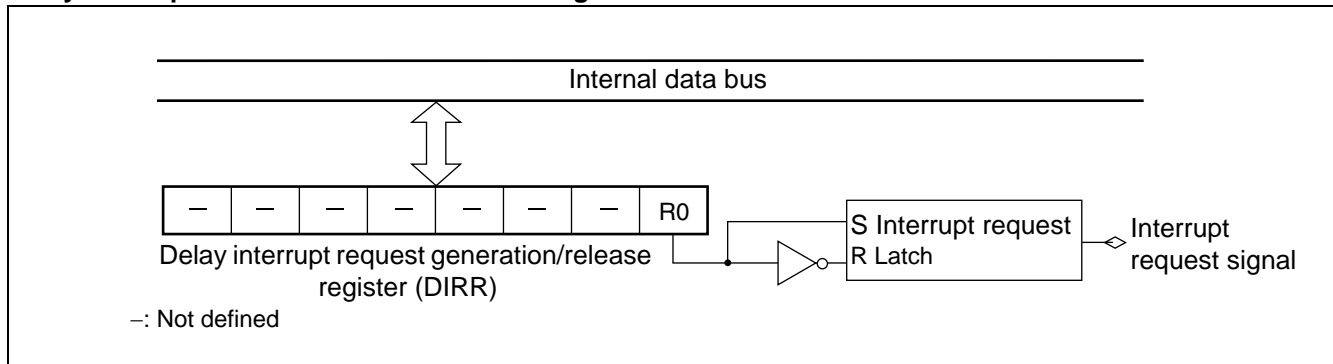


### Interrupt Request Latch

A latch that retains settings on delay interrupt request generation/release register (generation or release of delay interrupt request).

### Delay Interrupt Request Generation/Release Register (DIRR)

Generates or releases delay interrupt request.

### Interrupt Number

An interrupt number used in delay interrupt generation module is as follows:

Interrupt number: #42 (2A$_H$)

### 12.10  8/10-bit A/D Converter

The 8/10-bit A/D converter converts an analog input voltage into 8-bit or 10/bit digital value, using the RC-type successive approximation conversion method.

■ Input signal is selected among 8 channels of analog input pins.

■ Activation trigger is selected among software trigger, internal timer output, and external trigger.

### Functions of 8/10-bit A/D Converter

The 8/10-bit A/D converter converts an analog voltage (input voltage) input to analog input pin into an 8-bit or 10-bit digital value (A/D conversion).

The 8/10-bit A/D converter has the following functions:

■ A/D conversion takes a minimum of 6.12 $\mu$s* for 1 channel, including sampling time. (A/D conversion)

■ Sampling of one channel takes a minimum of 2.0 $\mu$s*.

■ RC-type successive approximation conversion method, with sample & hold circuit is used for conversion.

■ Resolution of either 8 bits or 10 bits is specifiable.

■ A maximum of 8 channels of analog input pins are allowed for use.

■ Generation of interrupt request is allowed, by storing A/D conversion result in A/D data register.

■ Activation of EI2OS is allowed upon occurrence of an interrupt request. With use of EI2OS, data loss is avoided even if A/D conversion is performed successively.

■ An activation trigger is selectable among software trigger, internal timer output, and external trigger (fall edge).

: When operating with 16 MHz machine clock

### 8/10-bit A/D Converter Conversion Mode

| Conversion Mode | Description |
|---|---|
| Singular conversion mode | The A/D conversion is performed form a start channel to an end channel sequentially. Upon completion of A/D conversion on an end channel, A/D conversion function stops. |
| Sequential conversion mode | The A/D conversion is performed form a start channel to an end channel sequentially. Upon completion of A/D conversion on an end channel, A/D conversion function resumes from the start channel. |
| Pausing conversion mode | The A/D conversion is performed by pausing at each channel. Upon completion of A/D conversion on an end channel, A/D conversion and pause functions resume from the start channel. |

**CAN Controller Block Diagram**
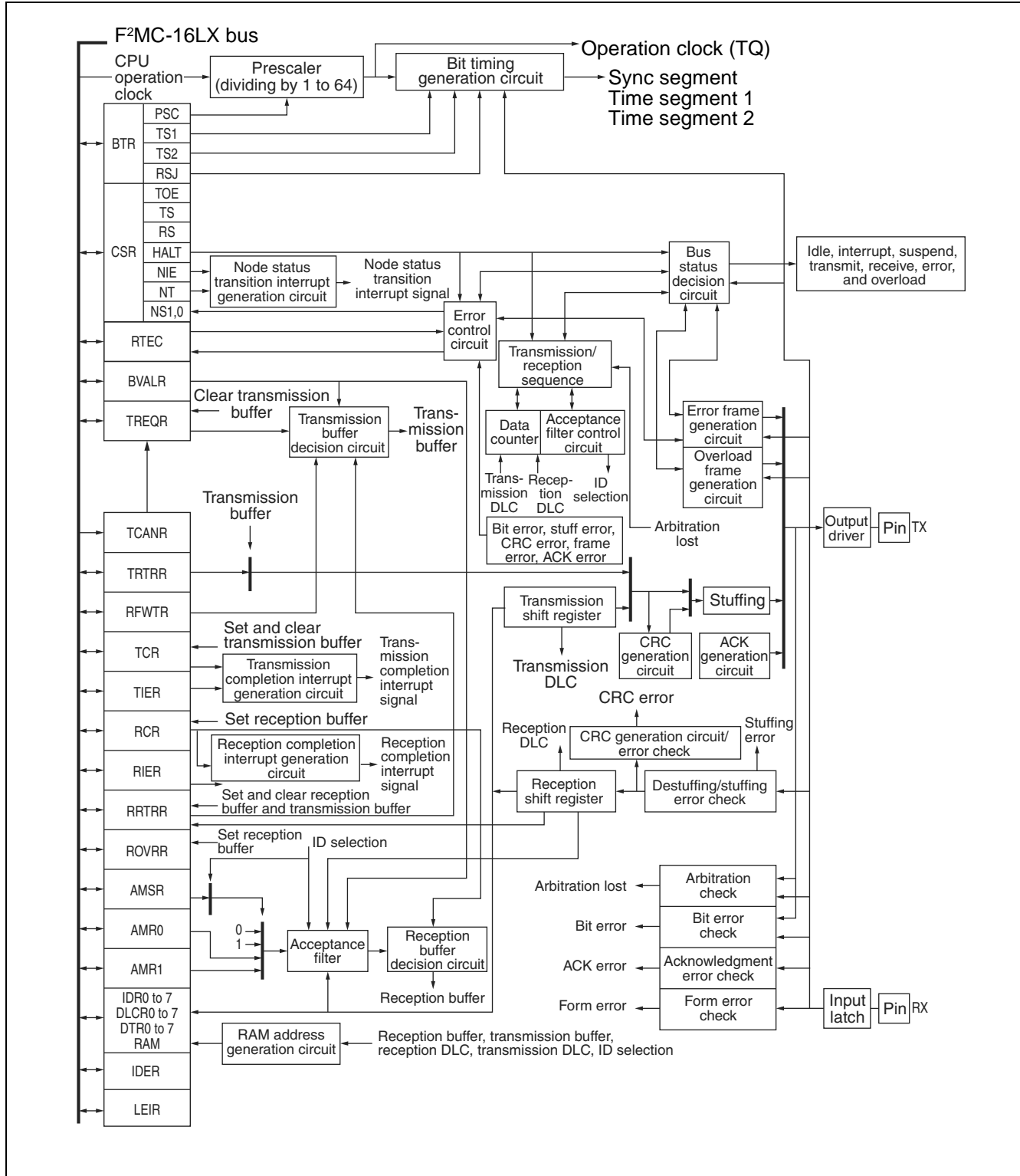
## 12.14  ROM Mirror Function Selection Module Outline

The ROM mirror function selection module sets the data in ROM assigned to FF bank so that the data is read by access to 00 bank.

**ROM Mirror Function Selection Module Block Diagram**
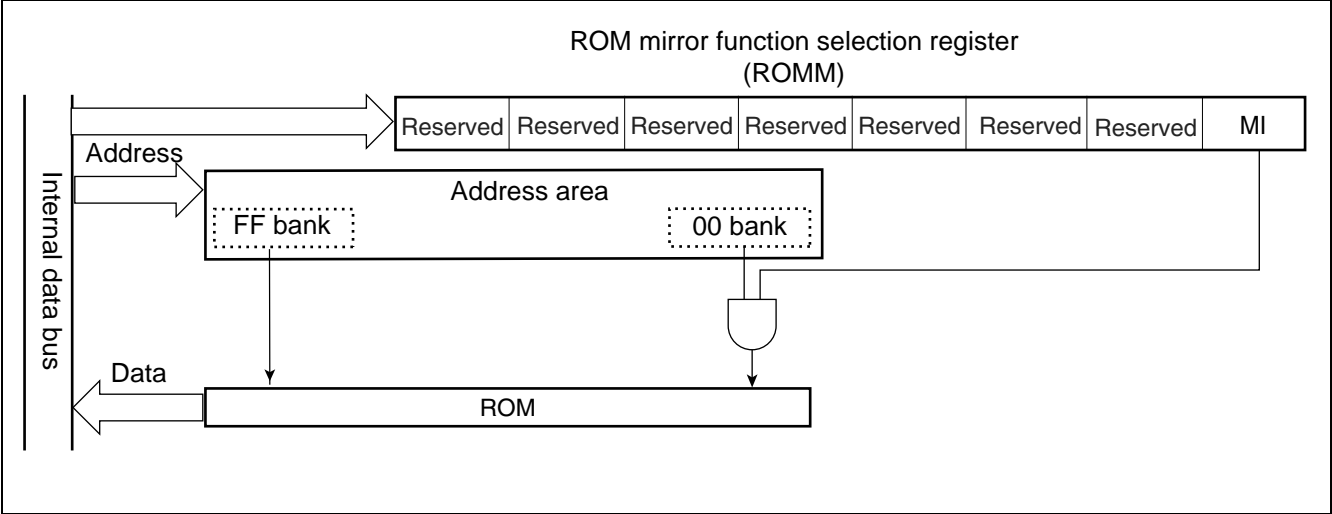


**FF Bank Access by ROM Mirror Function**
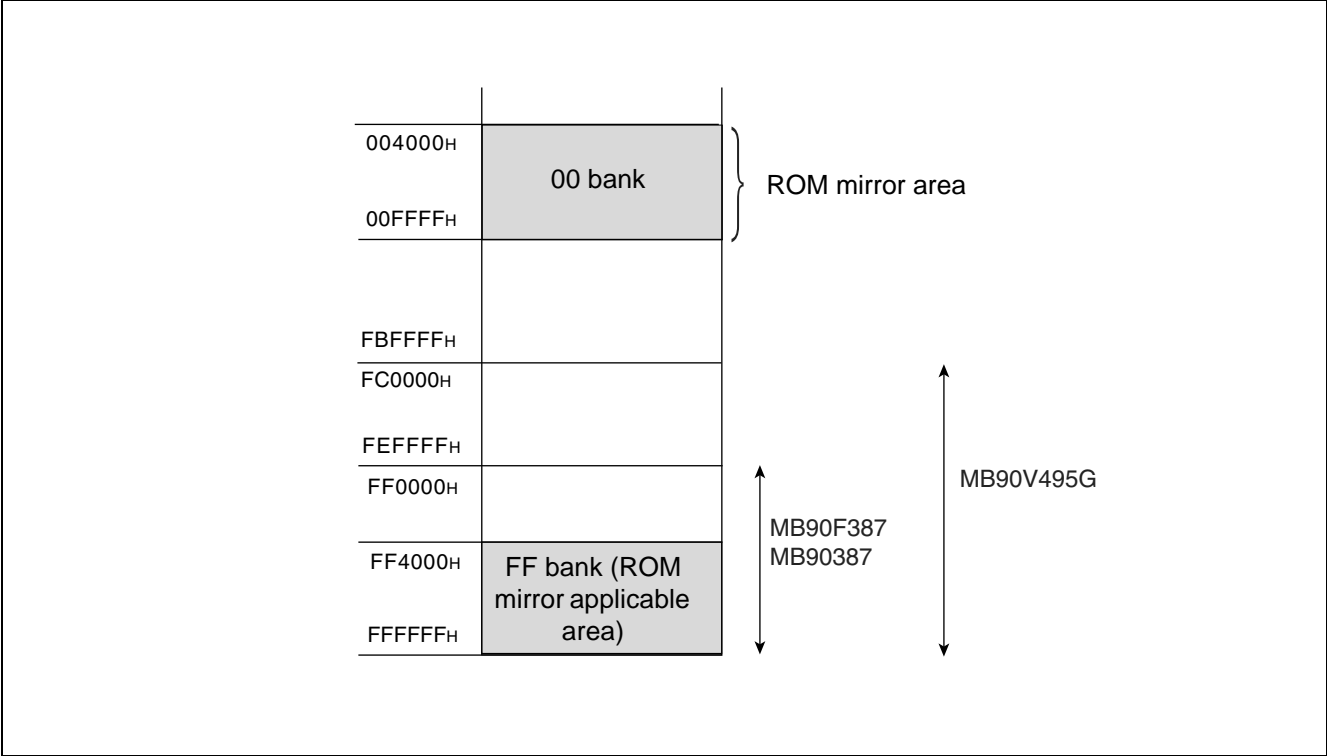
**Sector Configuration of 512 Kbit Flash Memory**

| Flash memory | CPU address | Writer address* |
|---|---|---|
| SA0 (32 Kbytes) | FF0000H<br><br>FF7FFFH | 70000H<br><br>77FFFH |
| SA1 (8 Kbytes) | FF8000H<br><br>FF9FFFH | 78000H<br><br>79FFFH |
| SA2 (8 Kbytes) | FFA000H<br><br>FFBFFFH | 7A000H<br><br>7BFFFH |
| SA3 (16 Kbytes) | FFC000H<br><br>FFFFFFH | 7C000H<br><br>7FFFFH |

\*: "Writer address" is an address equivalent to CPU address, which is used when data is written on Flash memory, using parallel writer. When writing/ deleting data with general-purpose writer, the writer address is used for writing and deleting.

# 13. Electrical Characteristics

## 13.1 Absolute Maximum Rating

| Parameter | Symbol | Rating | | Unit | Remarks |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Power supply voltage[*1] | $V_{CC}$ | $V_{SS} - 0.3$ | $V_{SS} + 6.0$ | V | |
| | $AV_{CC}$ | $V_{SS} - 0.3$ | $V_{SS} + 6.0$ | V | $V_{CC} = AV_{CC}$[*2] |
| | AVR | $V_{SS} - 0.3$ | $V_{SS} + 6.0$ | V | $AV_{CC} \geq AVR$[*2] |
| Input voltage[*1] | $V_I$ | $V_{SS} - 0.3$ | $V_{SS} + 6.0$ | V | [*3] |
| Output voltage[*1] | $V_O$ | $V_{SS} - 0.3$ | $V_{SS} + 6.0$ | V | [*3] |
| Maximum clamp current | $I_{CLAMP}$ | $-2.0$ | $+2.0$ | mA | [*7] |
| Total maximum clamp current | $\Sigma \mid I_{CLAMP} \mid$ | – | 20 | mA | [*7] |
| "L" level maximum output current | $I_{OL1}$ | – | 15 | mA | Normal output[*4] |
| | $I_{OL2}$ | – | 40 | mA | High-current output[*4] |
| "L" level average output current | $I_{OLAV1}$ | – | 4 | mA | Normal output[*5] |
| | $I_{OLAV2}$ | – | 30 | mA | High-current output[*5] |
| "L" level maximum total output current | $\Sigma I_{OL1}$ | – | 125 | mA | Normal output |
| | $\Sigma I_{OL2}$ | – | 160 | mA | High-current output |
| "L" level average total output current | $\Sigma I_{OLAV1}$ | – | 40 | mA | Normal output[*6] |
| | $\Sigma I_{OLAV2}$ | – | 40 | mA | High-current output[*6] |
| "H" level maximum output current | $I_{OH1}$ | – | $-15$ | mA | Normal output[*4] |
| | $I_{OH2}$ | – | $-40$ | mA | High-current output[*4] |
| "H" level average output current | $I_{OHAV1}$ | – | $-4$ | mA | Normal output[*5] |
| | $I_{OHAV2}$ | – | $-30$ | mA | High-current output[*5] |
| "H" level maximum total output current | $\Sigma I_{OH1}$ | – | $-125$ | mA | Normal output |
| | $\Sigma I_{OH2}$ | – | $-160$ | mA | High-current output |
| "H" level average total output current | $\Sigma I_{OHAV1}$ | – | $-40$ | mA | Normal output[*6] |
| | $\Sigma I_{OHAV2}$ | – | $-40$ | mA | High-current output[*6] |
| Power consumption | $P_D$ | – | 245 | mW | |
| Operating temperature | $T_A$ | $-40$ | $+105$ | °C | |
| Storage temperature | Tstg | $-55$ | $+150$ | °C | |

*1: The parameter is based on $V_{SS} = AV_{SS} = 0.0$ V.

*2: AVcc and AVR should not exceed Vcc.

*3: $V_I$ and $V_O$ should not exceed Vcc + 0.3 V. However if the maximum current to/from an input is limited by some means with external components, the $I_{CLAMP}$ rating supersedes the $V_I$ rating.

*4: A peak value of an applicable one pin is specified as a maximum output current.

*5: An average current value of an applicable one pin within 100 ms is specified as an average output current.
  (Average value is found by multiplying operating current by operating rate.)

*6: An average current value of all pins within 100 ms is specified as an average total output current. (Average value is found by multiplying operating current by operating rate.)

*7:

■ Applicable to pins: P10 to P17, P20 to P27, P30 to P33, P35*, P36*, P37, P40 to P44, P50 to P57
  *: P35 and P36 are MB90387S and MB90F387S only.

$(V_{CC} = 5.0 \text{ V} \pm 10\%, V_{SS} = AV_{SS} = 0.0 \text{ V}, T_A = -40 °C \text{ to } +105 °C)$

| Parameter | Symbol | Pin Name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | **Min** | **Typ** | **Max** | | |
| Power supply current* | $I_{CCL}$ | $V_{CC}$ | $V_{CC} = 5.0 \text{ V}$, Internally operating at 8 kHz, subclock operation, $T_A = +25°C$ | — | 0.3 | 1.2 | mA | MB90F387/S |
| | | | | — | 40 | 100 | $\mu$A | MB90387/S |
| | $I_{CCLS}$ | | $V_{CC} = 5.0 \text{ V}$, Internally operating at 8 kHz, subclock, sleep mode, $T_A = +25°C$ | — | 10 | 30 | $\mu$A | |
| | $I_{CCT}$ | | $V_{CC} = 5.0 \text{ V}$, Internally operating at 8 kHz, watch mode, $T_A = +25°C$ | — | 8 | 25 | $\mu$A | |
| | $I_{CCH}$ | | Stopping, $T_A = +25°C$ | — | 5 | 20 | $\mu$A | |
| Input capacity | $C_{IN}$ | Other than $AV_{CC}$, $AV_{SS}$, AVR, C, $V_{CC}$, $V_{SS}$ | – | — | 5 | 15 | pF | |
| Pull-up resistor | $R_{UP}$ | RST | – | 25 | 50 | 100 | k$\Omega$ | |
| Pull-down resistor | $R_{DOWN}$ | MD2 | – | 25 | 50 | 100 | k$\Omega$ | Flash product is not provided with pull-down resistor. |

*: Test conditions of power supply current are based on a device using external clock.

## 13.7  Notes on A/D Converter Section

Use the device with external circuits of the following output impedance for analog inputs:

Recommended output impedance of external circuits are: Approx. 3.9 kΩ or lower (4.5 V ≤ AVcc ≤ 5.5 V) (sampling period=2.00 μs at 16 MHz machine clock), Approx. 11 kΩ or lower (4.0 V ≤ AVcc < 4.5 V) (sampling period=8.0 μs at 16 MHz machine clock).

If an external capacitor is used, in consideration of the effect by tap capacitance caused by external capacitors and on-chip capacitors, capacitance of the external one is recommended to be several thousand times as high as internal capacitor.

If output impedance of an external circuit is too high, a sampling period for an analog voltage may be insufficient.

- Analog input circuit model
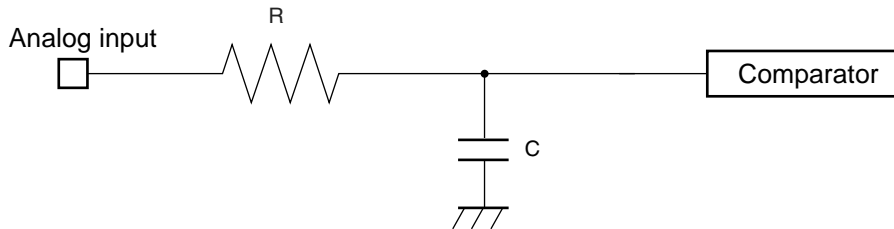


MB90F387/S, MB90387/S
4.5 V ≤ AVcc ≤ 5.5 V        R ≅ 2.35 kΩ, C ≅ 36.4 pF
4.0 V ≤ AVcc < 4.5 V        R ≅ 16.4 kΩ, C ≅ 36.4 pF

Note: Use the values in the figure only as a guideline.

### About errors

As [AVR-AVss] become smaller, values of relative errors grow larger.

## 13.8  Flash Memory Program/Erase Characteristics

| Parameter | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| Sector erase time | $T_A = +25\ °C$ $V_{CC} = 5.0\ V$ | – | 1 | 15 | s | Excludes 00H programming prior to erasure |
| Chip erase time | | – | 4 | – | s | Excludes 00H programming prior to erasure |
| Word (16-bit width) programming time | | – | 16 | 3,600 | μs | Except for the over head time of the system |
| Program/Erase cycle | – | 10,000 | – | – | cycle | |
| Flash Data Retention Time | Average $T_A = +85\ °C$ | 20 | – | – | Year | * |

*: This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at + 85 °C).

**I$_{CCLS}$ − V$_{CC}$**

T$_A$ = +25 °C, In external clock operation
f = Internal operating frequency

f = 8 kHz

**I$_{CCT}$ − V$_{CC}$**

T$_A$ = +25 °C, In external clock operation
f = Internal operating frequency

f = 8 kHz

**I$_{CCH}$ − V$_{CC}$**

Stopping, T$_A$ = +25 °C
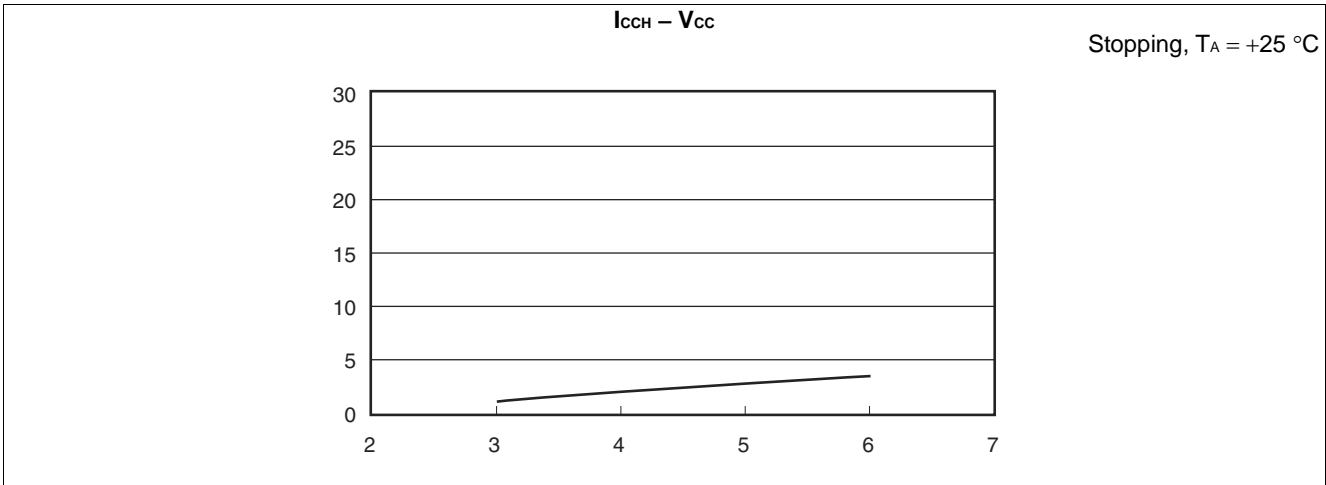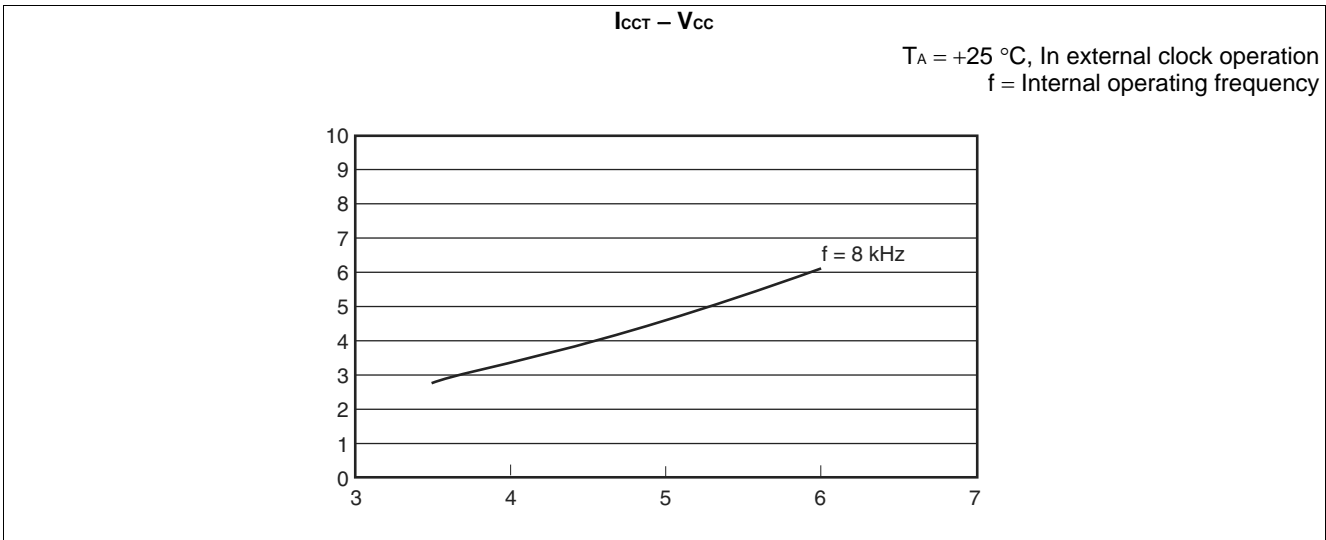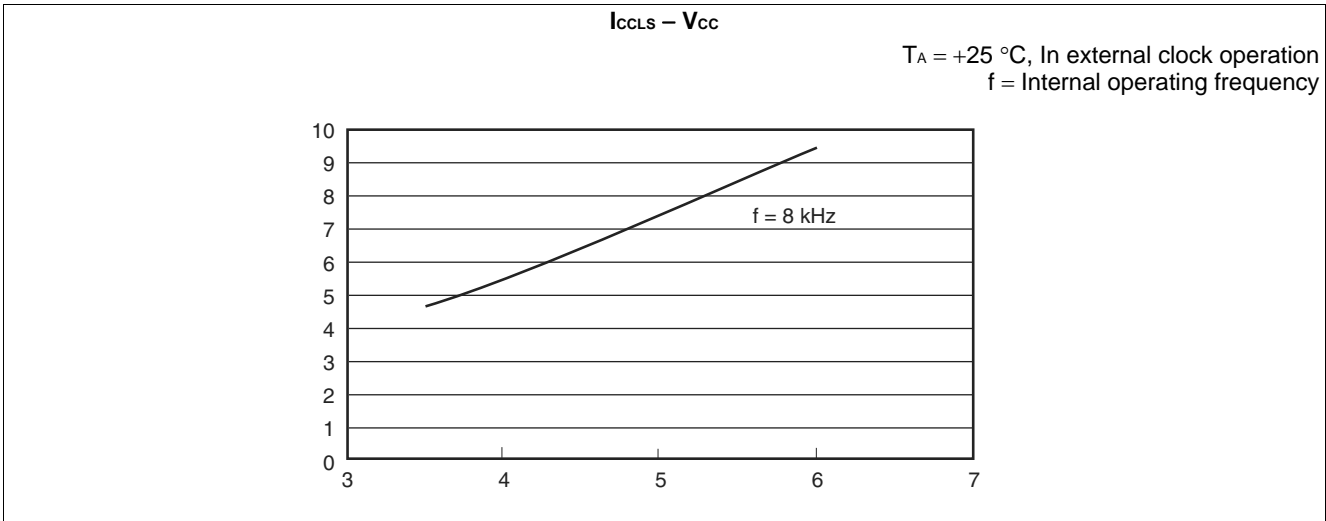
*(Continued)*

## 15. Ordering Information

| Part Number | Package | Remarks |
|---|---|---|
| MB90F387PMT<br>MB90387PMT<br>MB90F387SPMT<br>MB90387SPMT | 48-pin plastic LQFP<br>(LQA048) | |

## 16. Package Dimension



TOP VIEW

BOTTOM VIEW

SIDE VIEW

DETAIL A

SECTION A-A'
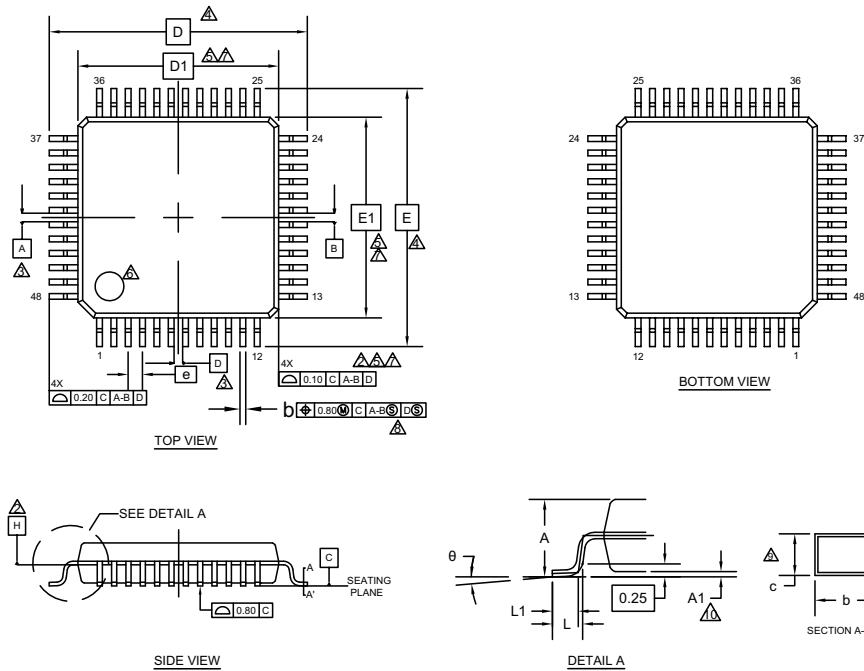
| SYMBOL | DIMENSIONS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | — | — | 1.70 |
| A1 | 0.00 | — | 0.20 |
| b | 0.15 | — | 0.27 |
| c | 0.09 | — | 0.20 |
| D | 9.00 BSC | | |
| D1 | 7.00 BSC | | |
| e | 0.50 BSC | | |
| E | 9.00 BSC | | |
| E1 | 7.00 BSC | | |
| L | 0.45 | 0.60 | 0.75 |
| L1 | 0.30 | 0.50 | 0.70 |
| θ | 0° | — | 8° |

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.

2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.

3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.

4. TO BE DETERMINED AT SEATING PLANE C.

5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.

7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.

8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.

9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.

10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-13731 **

PACKAGE OUTLINE, 48 LEAD LQFP
7.0X7.0X1.7 MM LQA048 REV**

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