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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, SCI, UART/USART
Peripherals	POR, WDT
Number of I/O	34
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90f387pmc-gte1

DTP/External Interrupt: 4 channels, CAN wakeup: 1channel

- Module for activation of expanded intelligent I/O service (EI^2OS), and generation of external interrupt.

Delay Interrupt Generator Module

- Generates interrupt request for task switching.

8/10-bit A/D Converter: 8 channels

- Resolution is selectable between 8-bit and 10-bit.
- Activation by external trigger input is allowed.
- Conversion time: 6.125 μs (at 16 MHz machine clock, including sampling time)

Program Patch Function

- Address matching detection for 2 address pointers.

5. Pin Description

Pin No.	Pin Name	Circuit Type	Function
1	AVcc	–	Vcc power input pin for A/D converter.
2	AVR	–	Power (Vref+) input pin for A/D converter. Use as input for Vcc or lower.
3 to 10	P50 to P57	E	General-purpose input/output ports.
	AN0 to AN7		Functions as analog input pins for A/D converter. Valid when analog input setting is “enabled.”
11	P37	D	General-purpose input/output port.
	ADTG		Function as an external trigger input pin for A/D converter. Use the pin by setting as input port.
12	P20	D	General-purpose input/output port.
	TIN0		Function as an event input pin for reload timer 0. Use the pin by setting as input port.
13	P21	D	General-purpose input/output port.
	TOT0		Function as an event output pin for reload timer 0. Valid only when output setting is “enabled.”
14	P22	D	General-purpose input/output port.
	TIN1		Function as an event input pin for reload timer 1. Use the pin by setting as input port.
15	P23	D	General-purpose input/output port.
	TOT1		Function as an event output pin for reload timer 1. Valid only when output setting is “enabled.”
16 to 19	P24 to P27	D	General-purpose input/output ports.
	INT4 to INT7		Functions as external interrupt input pins. Use the pins by setting as input port.
20	MD2	F	Input pin for specifying operation mode. Connect directly to Vss.
21	MD1	C	Input pin for specifying operation mode. Connect directly to Vcc.
22	MD0	C	Input pin for specifying operation mode. Connect directly to Vcc.
23	RST	B	External reset input pin.
24	Vcc	–	Power source (5 V) input pin.
25	Vss	–	Power source (0 V) input pin.
26	C	–	Capacitor pin for stabilizing power source. Connect a ceramic capacitor of approximately 0.1 μF.
27	X0	A	Pin for high-rate oscillation.
28	X1	A	Pin for high-rate oscillation.
29 to 32	P10 to P13	D	General-purpose input/output ports.
	IN0 to IN3		Functions as trigger input pins of input capture ch.0 to ch.3. Use the pins by setting as input ports.
33 to 36	P14 to P17	G	General-purpose input/output ports. High-current output ports.
	PPG0 to PPG3		Functions as output pins of PPG timers 01 and 23. Valid when output setting is “enabled.”
37	P40	D	General-purpose input/output port.
	SIN1		Serial data input pin for UART. Use the pin by setting as input port.
38	P41	D	General-purpose input/output port.
	SCK1		Serial clock input pin for UART. Valid only when serial clock input/output setting on UART is “enabled.”

Notes When Using No Sub Clock

■ If an oscillator is not connected to X0A and X1A pin, apply pull-down resistor to X0A pin and leave X1A pin open.

About Power Supply Pins

■ If two or more Vcc and Vss pins exist, the pins that should be at the same potential are connected to each other inside the device. For reducing unwanted emissions and preventing malfunction of strobe signals caused by increase of ground level, however, be sure to connect the Vcc and Vss pins to the power source and the ground externally.

■ Pay attention to connect a power supply to Vcc and Vss of MB90385 series device in a lowest-possible impedance.

■ Near pins of MB90385 series device, connecting a bypass capacitor is recommended at 0.1 μF across Vcc pin and Vss pin.

Crystal Oscillator Circuit

■ Noises around X0 and X1 pins cause malfunctions on a MB90385 series device. Design a print circuit so that X0 and X1 pins, an crystal oscillator (or a ceramic oscillator), and bypass capacitor to the ground become as close as possible to each other. Furthermore, avoid wires to X0 and X1 pins crossing each other as much as possible.

■ Print circuit designing that surrounds X0 and X1 pins with grounding wires, which ensures stable operation, is strongly recommended.

Caution on Operations during PLL Clock Mode

■ If the PLL clock mode is selected, the microcontroller attempt to be working with the self-oscillating circuit even when there is no external oscillator or external clock input is stopped. Performance of this operation, however, cannot be guaranteed.

Sequence of Turning on Power of A/D Converter and Applying Analog Input

■ Be sure to turn on digital power (Vcc) before applying signals to the A/D converter and applying analog input signals (AN0 to AN7 pins).

■ Be sure to turn off the power of A/D converter and analog input before turning off the digital power source.

■ Be sure not to apply AVR exceeding AVcc when turning on and off. (No problems occur if analog and digital power is turned on and off simultaneously.)

Handling Pins When A/D Converter is Not Used

■ If the A/D converter is not used, connect the pins under the following conditions: “AVcc=AVR=Vcc,” and “AVss=Vss”

Note on Turning on Power

■ For preventing malfunctions on built-in step-down circuit, maintain a minimum of 50 μs of voltage rising time (between 0.2 V and 2.7V) when turning on the power.

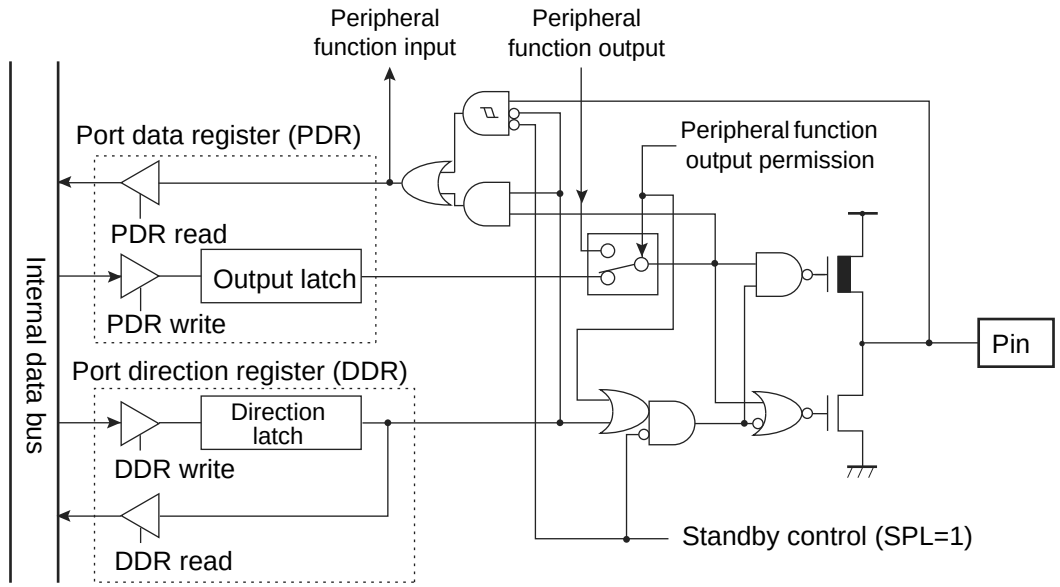
Stabilization of Supply Voltage

■ A sudden change in the supply voltage may cause the device to malfunction even within the specified V_{CC} supply voltage operating range. Therefore, the V_{CC} supply voltage should be stabilized.
For reference, the supply voltage should be controlled so that V_{CC} ripple variations (peak-to-peak values) at commercial frequencies (50 Hz / 60 Hz) fall below 10% of the standard V_{CC} supply voltage and the coefficient of fluctuation does not exceed 0.1 V/ms at instantaneous power switching.

Address	Register Abbreviation	Register	Read/ Write	Resource	Initial Value
003910H	PRLL0	PPG0 reload register L	R/W	8/16-bit PPG timer	XXXXXXXXB
003911H	PRLH0	PPG0 reload register H	R/W		XXXXXXXXB
003912H	PRLL1	PPG1 reload register L	R/W		XXXXXXXXB
003913H	PRLH1	PPG1 reload register H	R/W		XXXXXXXXB
003914H	PRLL2	PPG2 reload register L	R/W		XXXXXXXXB
003915H	PRLH2	PPG2 reload register H	R/W		XXXXXXXXB
003916H	PRLL3	PPG3 reload register L	R/W		XXXXXXXXB
003917H	PRLH3	PPG3 reload register H	R/W		XXXXXXXXB
003918H to 00392FH	(Reserved area) *				
003930H to 003BFFH	(Reserved area) *				
003C00H to 003C0FH	RAM (General-purpose RAM)				
003C10H to 003C13H	IDR0	ID register 0	R/W	CAN controller	XXXXXXXXB to XXXXXXXXB
003C14H to 003C17H	IDR1	ID register 1	R/W		XXXXXXXXB to XXXXXXXXB
003C18H to 003C1BH	IDR2	ID register 2	R/W		XXXXXXXXB to XXXXXXXXB
003C1CH to 003C1FH	IDR3	ID register 3	R/W		XXXXXXXXB to XXXXXXXXB
003C20H to 003C23H	IDR4	ID register 4	R/W		XXXXXXXXB to XXXXXXXXB
003C24H to 003C27H	IDR5	ID register 5	R/W		XXXXXXXXB to XXXXXXXXB
003C28H to 003C2BH	IDR6	ID register 6	R/W		XXXXXXXXB to XXXXXXXXB
003C2CH to 003C2FH	IDR7	ID register 7	R/W		XXXXXXXXB to XXXXXXXXB
003C30H, 003C31H	DLCR0	DLC register 0	R/W		XXXXXXXXB, XXXXXXXXB
003C32H, 003C33H	DLCR1	DLC register 1	R/W		XXXXXXXXB, XXXXXXXXB
003C34H, 003C35H	DLCR2	DLC register 2	R/W		XXXXXXXXB, XXXXXXXXB
003C36H, 003C37H	DLCR3	DLC register 3	R/W		XXXXXXXXB, XXXXXXXXB

Address	Register Abbreviation	Register	Read/ Write	Resource	Initial Value
003C38H, 003C39H	DLCR4	DLC register 4	R/W	CAN controller	XXXXXXXXB, XXXXXXXXB
003C3AH, 003C3BH	DLCR5	DLC register 5	R/W		XXXXXXXXB, XXXXXXXXB
003C3CH, 003C3DH	DLCR6	DLC register 6	R/W		XXXXXXXXB, XXXXXXXXB
003C3EH, 003C3FH	DLCR7	DLC register 7	R/W		XXXXXXXXB, XXXXXXXXB
003C40H to 003C47H	DTR0	Data register 0	R/W		XXXXXXXXB to XXXXXXXXB
003C48H to 003C4FH	DTR1	Data register 1	R/W		XXXXXXXXB to XXXXXXXXB
003C50H to 003C57H	DTR2	Data register 2	R/W		XXXXXXXXB to XXXXXXXXB
003C58H to 003C5FH	DTR3	Data register 3	R/W		XXXXXXXXB to XXXXXXXXB
003C60H to 003C67H	DTR4	Data register 4	R/W		XXXXXXXXB to XXXXXXXXB
003C68H to 003C6FH	DTR5	Data register 5	R/W		XXXXXXXXB to XXXXXXXXB
003C70H to 003C77H	DTR6	Data register 6	R/W		XXXXXXXXB to XXXXXXXXB
003C78H to 003C7FH	DTR7	Data register 7	R/W		XXXXXXXXB to XXXXXXXXB
003C80H to 003CFFH	(Reserved area) *				
003D00H, 003D01H	CSR	Control status register	R/W, R	CAN controller	0XXXX001B, 00XXX000B
003D02H	LEIR	Last event display register	R/W		000XX000B
003D03H	(Reserved area) *				
003D04H, 003D05H	RTEC	Send/receive error counter	R	CAN controller	00000000B, 00000000B
003D06H, 003D07H	BTR	Bit timing register	R/W		11111111B, X1111111B
003D08H	IDER	IDE register	R/W		XXXXXXXXB
003D09H	(Reserved area) *				
003D0AH	TRTRR	Send RTR register	R/W	CAN controller	00000000B
003D0BH	(Reserved area) *				
003D0CH	RFWTR	Remote frame receive wait register	R/W	CAN controller	XXXXXXXXB

Port 4 Pins Block Diagram



Standby control: Control among Stop mode (SPL=1), Time-base timer mode (SPL=1), and watch mode (SPL=1).

Port 4 Registers

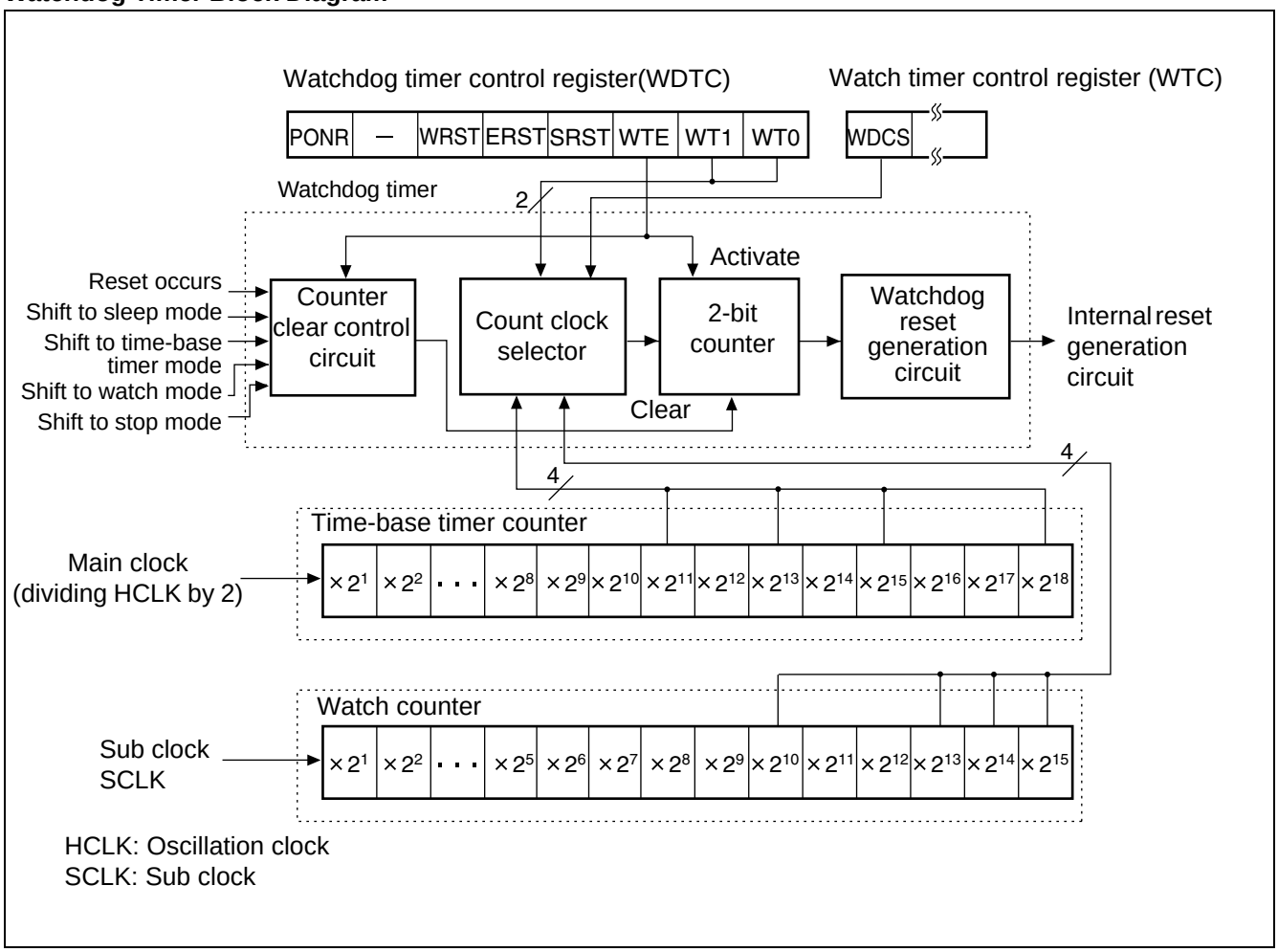
■ Port 4 registers include port 4 data register (PDR4) and port 4 direction register (DDR4).

■ The bits configuring the register correspond to port 4 pins on a one-to-one basis.

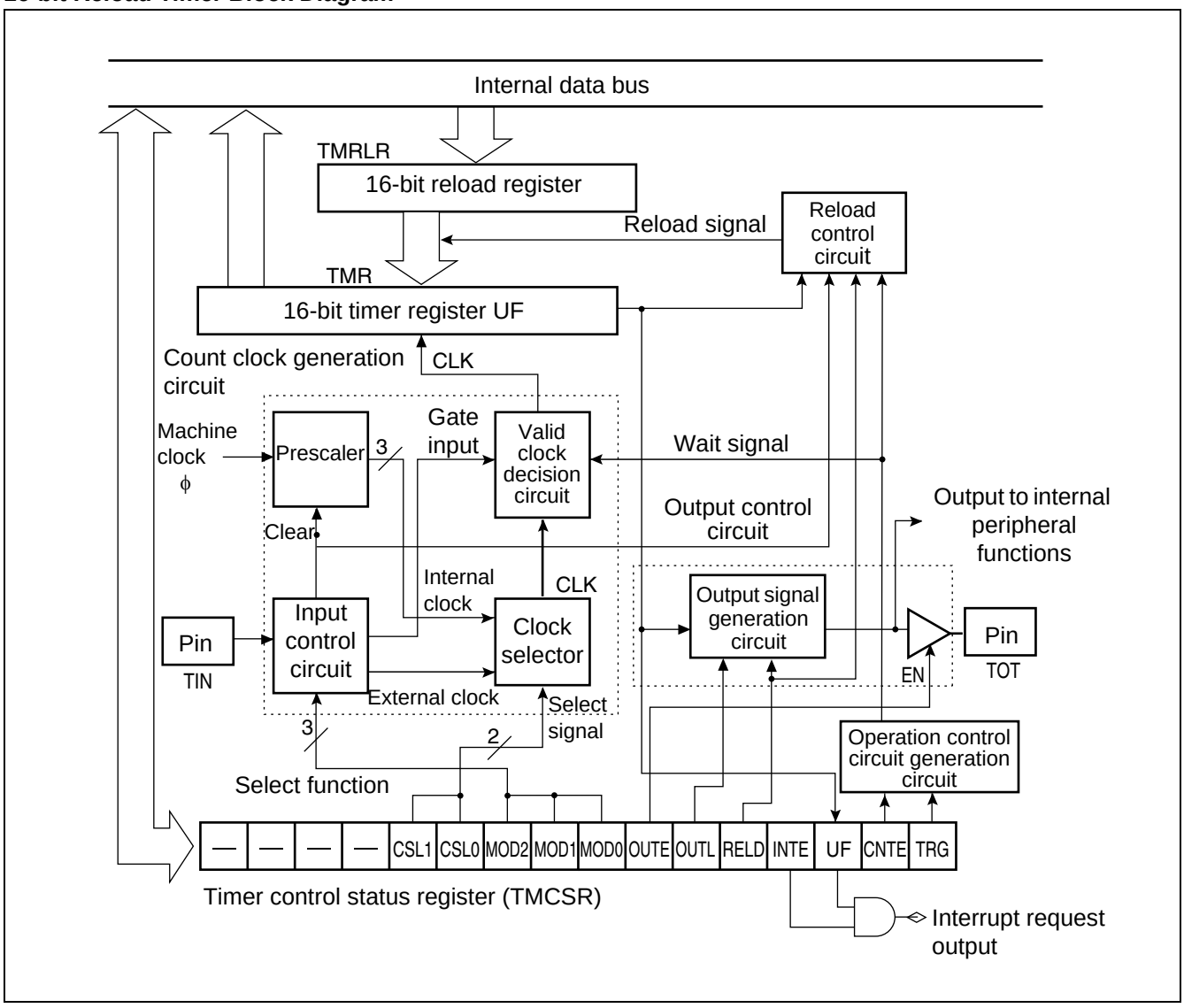
Relation between Port 4 Registers and Pins

Port Name	Bits of Register and Corresponding Pins									
Port 4	PDR4, DDR4	–	–	–	bit4	bit3	bit2	bit1	bit0
	Corresponding pins	–	–	–	P44	P43	P42	P41	P40

Watchdog Timer Block Diagram



16-bit Reload Timer Block Diagram



12.7 8/16-bit PPG Timer Outline

The 8/16-bit PPG timer is a 2-channel reload timer module (PPG0 and PPG1) that allows outputting pulses of arbitrary cycle and duty cycle. Combination of the two channels allows selection among the following operations:

- 8-bit PPG output 2-channel independent operation mode
- 16-bit PPG output operation mode
- 8-bit and 8-bit PPG output operation mode

MB90385 series device has two 8/16-bit built-in PPG timers. This section describes functions of PPG0/1. PPG2/3 have the same functions as those of PPG0/1.

Functions of 8/16-bit PPG Timer

The 8/16-bit PPG timer is composed of four 8-bit reload register (PRLH0/PRLL0, PRLH1/PRLL1) and two PPG down counters (PCNT0, PCNT1).

- Widths of “H” and “L” in output pulse are specifiable independently. Cycle and duty factor of output pulse is specifiable arbitrarily.
- Count clock is selectable among 6 internal clocks.
- The timer is usable as an interval timer, by generating interrupt requests for each interval.
- The time is usable as a D/A converter, with an external circuit.

12.10 8/10-bit A/D Converter

The 8/10-bit A/D converter converts an analog input voltage into 8-bit or 10/bit digital value, using the RC-type successive approximation conversion method.

- Input signal is selected among 8 channels of analog input pins.
- Activation trigger is selected among software trigger, internal timer output, and external trigger.

Functions of 8/10-bit A/D Converter

The 8/10-bit A/D converter converts an analog voltage (input voltage) input to analog input pin into an 8-bit or 10-bit digital value (A/D conversion).

The 8/10-bit A/D converter has the following functions:

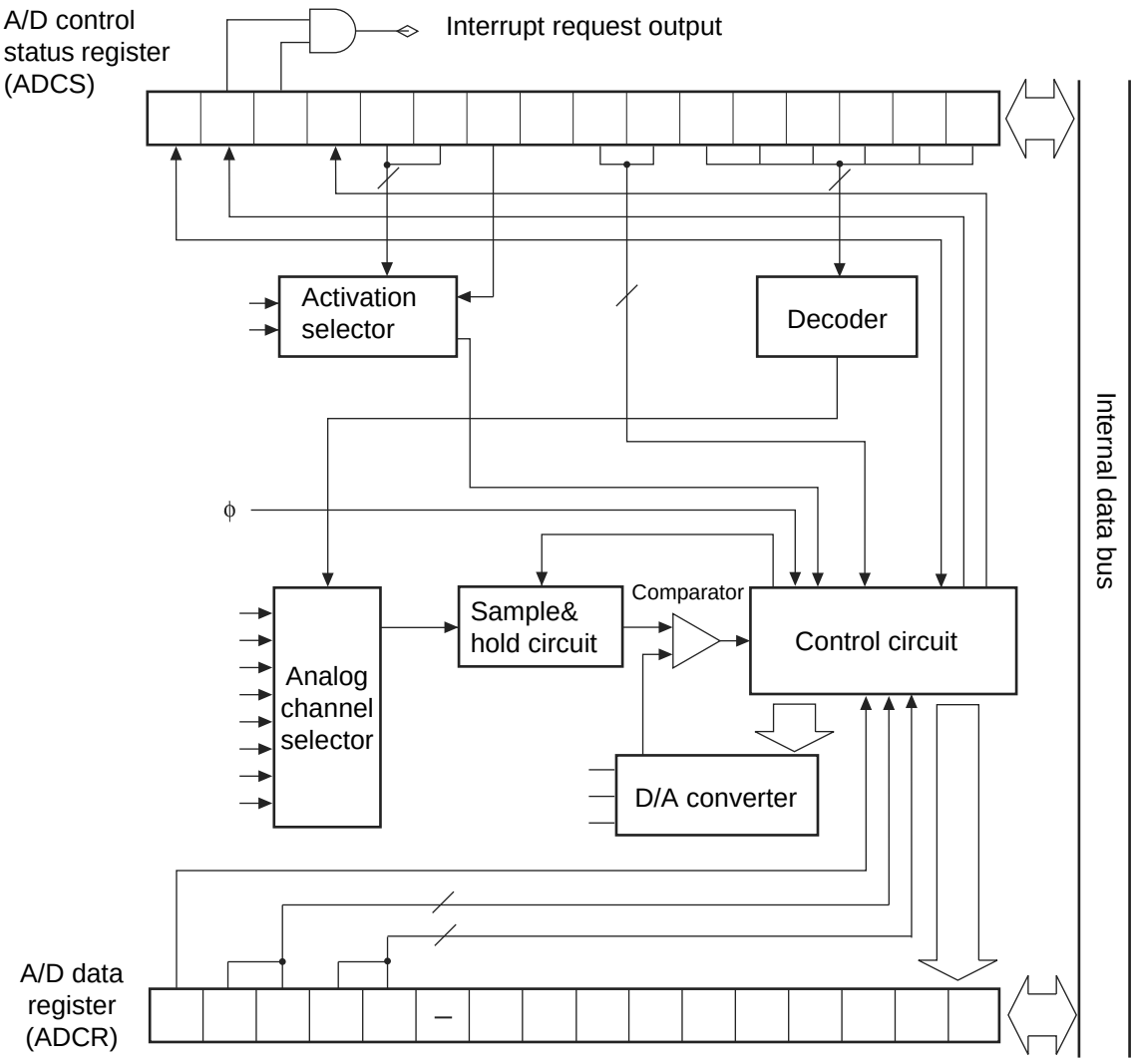
- A/D conversion takes a minimum of 6.12 μs* for 1 channel, including sampling time. (A/D conversion)
- Sampling of one channel takes a minimum of 2.0 μs*.
- RC-type successive approximation conversion method, with sample & hold circuit is used for conversion.
- Resolution of either 8 bits or 10 bits is specifiable.
- A maximum of 8 channels of analog input pins are allowed for use.
- Generation of interrupt request is allowed, by storing A/D conversion result in A/D data register.
- Activation of EI^{2}OS is allowed upon occurrence of an interrupt request. With use of EI^{2}OS, data loss is avoided even if A/D conversion is performed successively.
- An activation trigger is selectable among software trigger, internal timer output, and external trigger (fall edge).

: When operating with 16 MHz machine clock

8/10-bit A/D Converter Conversion Mode

Conversion Mode	Description
Singular conversion mode	The A/D conversion is performed form a start channel to an end channel sequentially. Upon completion of A/D conversion on an end channel, A/D conversion function stops.
Sequential conversion mode	The A/D conversion is performed form a start channel to an end channel sequentially. Upon completion of A/D conversion on an end channel, A/D conversion function resumes from the start channel.
Pausing conversion mode	The A/D conversion is performed by pausing at each channel. Upon completion of A/D conversion on an end channel, A/D conversion and pause functions resume from the start channel.

8/10-bit A/D Converter Block Diagram



TO : Internal timer output
– : Not defined
Reserved: Be sure to set to “0”
ϕ : Machine clock

Sector Configuration of 512 Kbit Flash Memory

Flash memory	CPU address	Writer address*
SA0 (32 Kbytes)	FF0000H FF7FFFH	70000H 77FFFH
SA1 (8 Kbytes)	FF8000H FF9FFFH	78000H 79FFFH
SA2 (8 Kbytes)	FFA000H FFBFFFH	7A000H 7BFFFH
SA3 (16 Kbytes)	FFC000H FFFFFFH	7C000H 7FFFFH

*: “Writer address” is an address equivalent to CPU address, which is used when data is written on Flash memory, using parallel writer. When writing/deleting data with general-purpose writer, the writer address is used for writing and deleting.

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

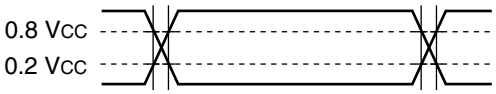
Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current*	I_{CCL}	V_{CC}	V_{CC} = 5.0 V, Internally operating at 8 kHz, subclock operation, T_A = + 25°C	—	0.3	1.2	mA	MB90F387/S
				—	40	100	µA	MB90387/S
	I_{CCLS}		V_{CC} = 5.0 V, Internally operating at 8 kHz, subclock, sleep mode, T_A = + 25°C	—	10	30	µA	
	I_{CCT}		V_{CC} = 5.0 V, Internally operating at 8 kHz, watch mode, T_A = + 25°C	—	8	25	µA	
	I_{CCH}		Stopping, T_A = + 25°C	—	5	20	µA	
Input capacity	C_{IN}	Other than AV_{CC}, AV_{SS}, AVR, C, V_{CC}, V_{SS}	–	—	5	15	pF	
Pull-up resistor	R_{UP}	RST	–	25	50	100	kΩ	
Pull-down resistor	R_{DOWN}	MD2	–	25	50	100	kΩ	Flash product is not provided with pull-down resistor.

*: Test conditions of power supply current are based on a device using external clock.

Rating values of alternating current is defined by the measurement reference voltage values shown below:

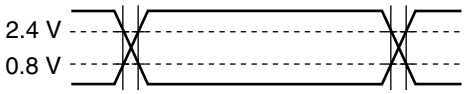
- Input signal waveform

Hysteresis input pin



- Output signal waveform

Output pin



13.4.2 Reset Input Timing

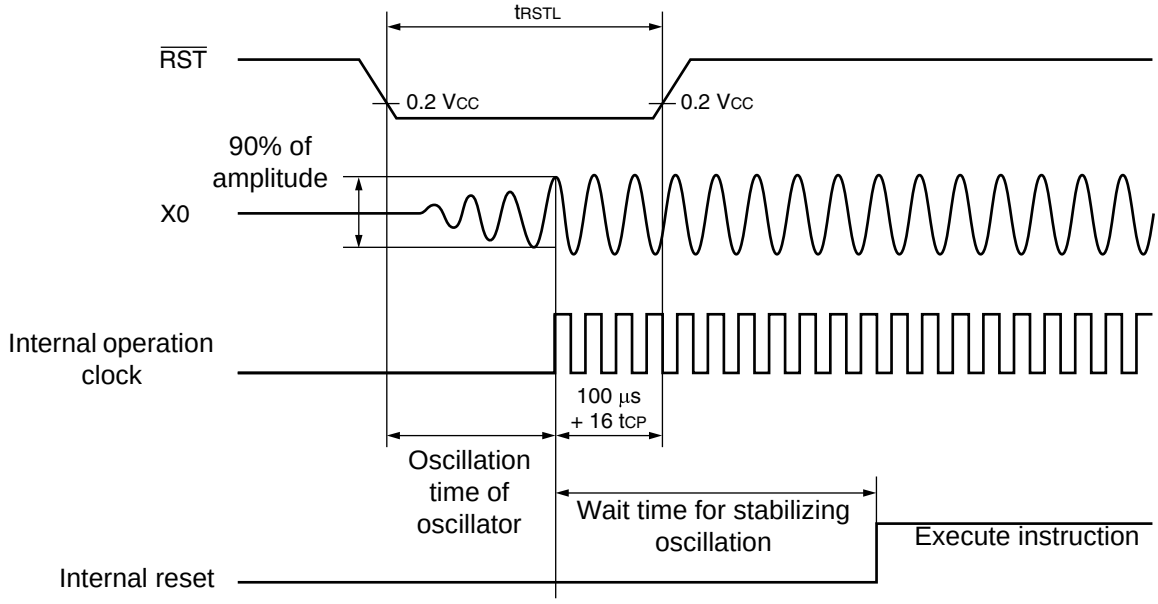
Parameter	Symbol	Pin Name	Value		Unit	Remarks
			Min	Max		
Reset input time	t_{RSTL}	RST	16 t_{CP}*3	–	ns	Normal operation
			Oscillation time of oscillator*1 + 100 μs + 16 t_{CP}*3	–	–	In sub clock*2, sub sleep*2, watch*2 and stop mode
			100	–	μs	In timebase timer

*1: Oscillation time of oscillator is time that the amplitude reached the 90%. In the crystal oscillator, the oscillation time is between several ms to tens of ms. In ceramic oscillator, the oscillation time is between hundreds of μs to several ms. In the external clock, the oscillation time is 0 ms.

*2: Except for MB90F387S and MB90387S.

*3: Refer to "(1) Clock timing" ratings for t_{CP} (internal operation clock cycle time).

- In sub clock, sub sleep, watch and stop mode



13.4.4 UART Timing

(V_{CC} = 4.5 V to 5.5 V, V_{SS} = 0.0 V, T_A = −40 °C to +105 °C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK1	Internal shift clock mode output pin is: CL = 80 pF+1TTL.	4 t_{CP} *	–	ns	
SCK ↓ → SOT delay time	t_{SLOV}	SCK1, SOT1		−80	+80	ns	
Valid SIN → SCK ↑	t_{IVSH}	SCK1, SIN1		100	–	ns	
SCK ↑ → valid SIN hold time	t_{SHIX}	SCK1, SIN1		60	–	ns	
Serial clock “H” pulse width	t_{SHSL}	SCK1	External shift clock mode output pin is: CL = 80 pF+1TTL.	2 t_{CP} *	–	ns	
Serial clock “L” pulse width	t_{SLSH}	SCK1		2 t_{CP} *	–	ns	
SCK ↓ → SOT delay time	t_{SLOV}	SCK1, SOT1		–	150	ns	
Valid SIN → SCK ↑	t_{IVSH}	SCK1, SIN1		60	–	ns	
SCK ↑ → valid SIN hold time	t_{SHIX}	SCK1, SIN1		60	–	ns	

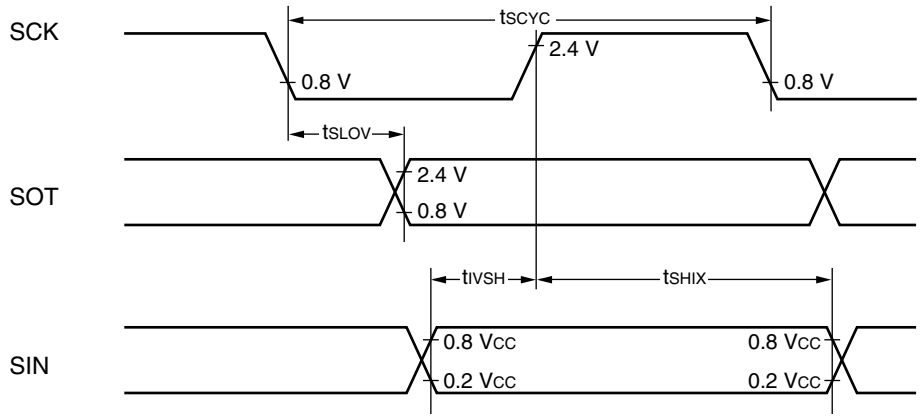
*: Refer to Clock Timing ratings for t_{CP} (internal operation clock cycle time).

Notes:

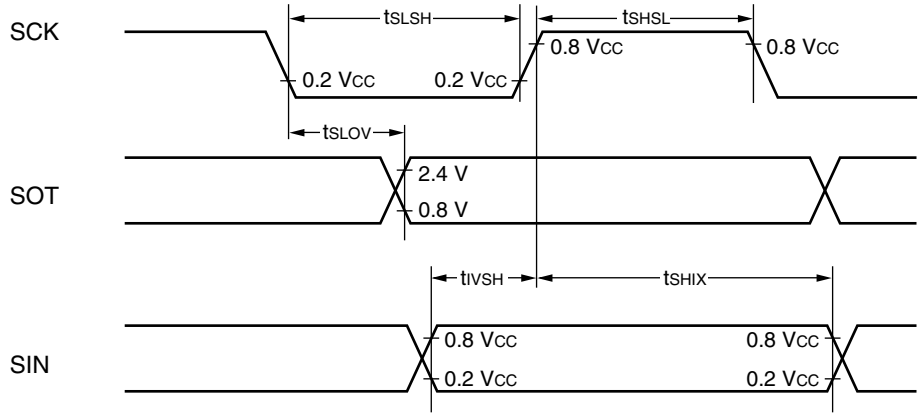
■ AC Characteristics in CLK synchronous mode.

■ C_L is a load capacitance value on pins for testing.

• Internal shift clock mode



• External shift clock mode



13.4.5 Timer Input Timing

(V_{CC} = 4.5 V to 5.5 V, V_{SS} = 0.0 V, T_A = −40 °C to +105 °C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH}	TIN0, TIN1	–	4 t_{CP} *	–	ns	
	t_{TIWL}	IN0 to IN3					

*: Refer to Clock Timing ratings for t_{CP} (internal operation clock cycle time).

13.7 Notes on A/D Converter Section

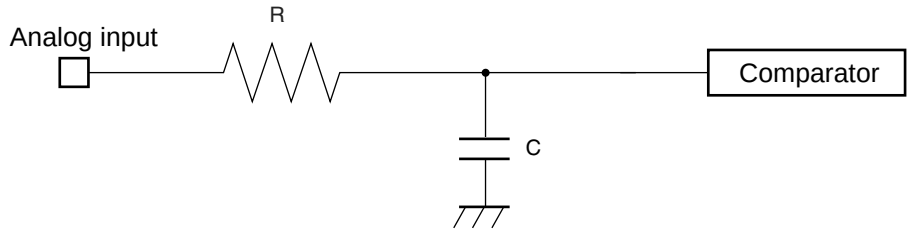
Use the device with external circuits of the following output impedance for analog inputs:

Recommended output impedance of external circuits are: Approx. 3.9 kΩ or lower (4.5 V ≤ AVcc ≤ 5.5 V) (sampling period=2.00 μs at 16 MHz machine clock), Approx. 11 kΩ or lower (4.0 V ≤ AVcc < 4.5 V) (sampling period=8.0 μs at 16 MHz machine clock).

If an external capacitor is used, in consideration of the effect by tap capacitance caused by external capacitors and on-chip capacitors, capacitance of the external one is recommended to be several thousand times as high as internal capacitor.

If output impedance of an external circuit is too high, a sampling period for an analog voltage may be insufficient.

- Analog input circuit model



MB90F387/S, MB90387/S

4.5 V ≤ AV_{CC} ≤ 5.5 V R ≅ 2.35 kΩ, C ≅ 36.4 pF

4.0 V ≤ AV_{CC} < 4.5 V R ≅ 16.4 kΩ, C ≅ 36.4 pF

Note: Use the values in the figure only as a guideline.

About errors

As [AVR-AVss] become smaller, values of relative errors grow larger.

13.8 Flash Memory Program/Erase Characteristics

Parameter	Conditions	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	T_A = + 25 °C V_{CC} = 5.0 V	–	1	15	s	Excludes 00H programming prior to erasure
Chip erase time		–	4	–	s	Excludes 00H programming prior to erasure
Word (16-bit width) programming time		–	16	3,600	μs	Except for the over head time of the system
Program/Erase cycle	–	10,000	–	–	cycle	
Flash Data Retention Time	Average T_A = + 85 °C	20	–	–	Year	*

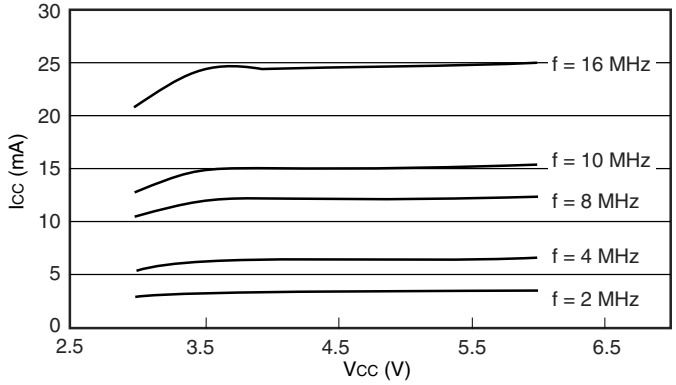
*: This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at + 85 °C).

14. Example Characteristics

MB90F387

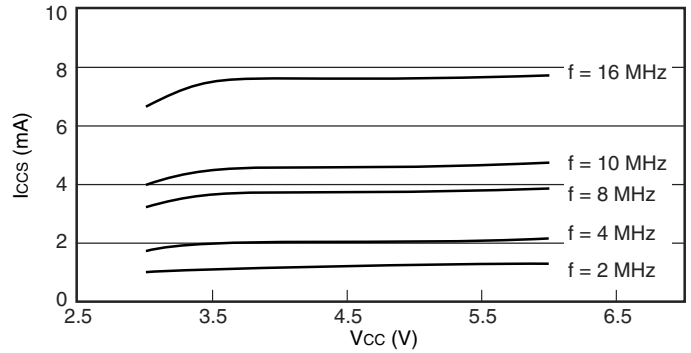
I_{CC} – V_{CC}

T_A = +25 °C, In external clock operation
f = Internal operating frequency



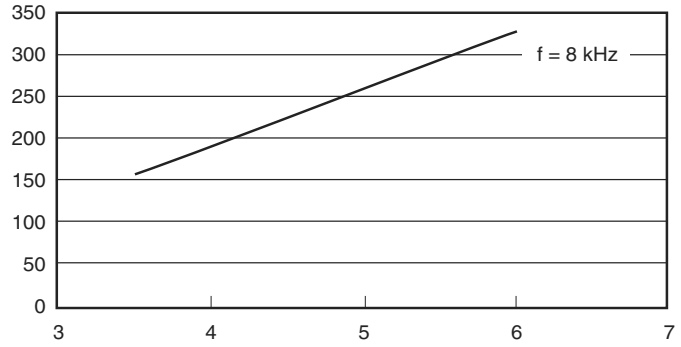
I_{CCS} – V_{CC}

T_A = +25 °C, In external clock operation
f = Internal operating frequency



I_{CCL} – V_{CC}

T_A = +25 °C, In external clock operation
f = Internal operating frequency

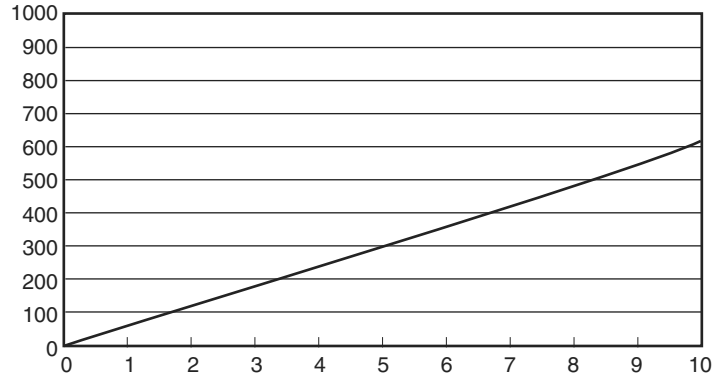


(Continued)

(Continued)

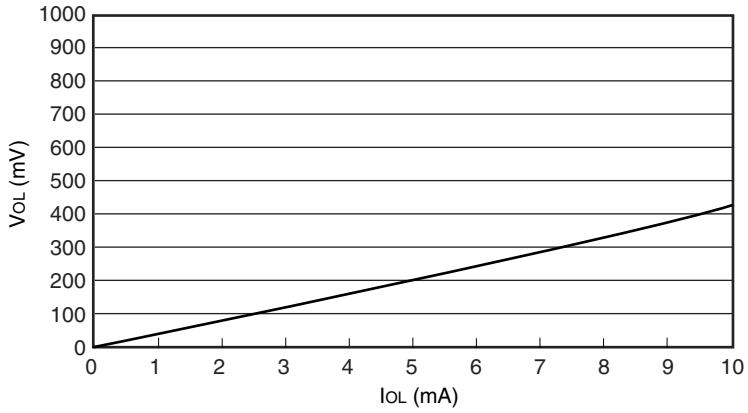
(V_{CC} - V_{OH}) – I_{OH}

T_A = +25 °C, V_{CC} = 4.5 V



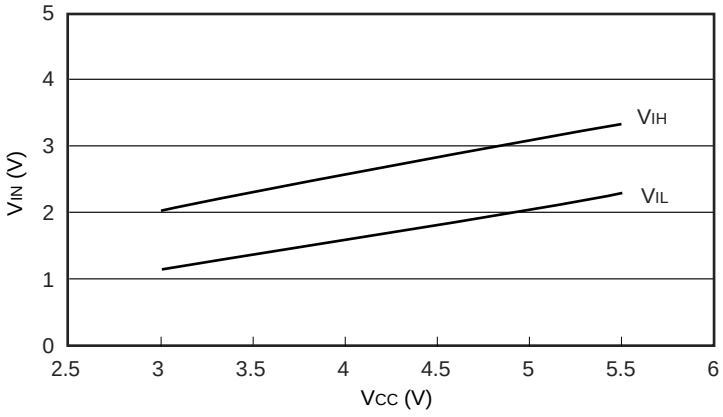
V_{OL} – I_{OL}

T_A = +25 °C, V_{CC} = 4.5 V



H level input voltage/ L level input voltage
V_{IN} – V_{CC}

T_A = +25 °C



Document History

Document Title: MB90387/387S/F387/F387S, MB90V495G, 16-bit Microcontrollers F²MC-16LX MB90385 Series Document Number:002-07765				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	—	AKIH	12/19/2008	Migrated to Cypress and assigned document number 002-07765. No change to document contents or format.
*A	6059071	SSAS	02/05/2018	Updated to Cypress template Package: FPT-48P-M26 --> LQA048