What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, SCI, UART/USART
Peripherals	POR, WDT
Number of I/O	34
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90f387pmt-g-jne1

Part Number / Parameter	MB90F387 MB90F387S	MB90387 MB90387S	MB90V495G
8/10-bit A/D converter	Number of channels: 8 Resolution: Selectable 10-bit or 8-bit. Conversion time: 6.125 μs (at 16 MHz machine clock, including sampling time) Sequential conversion of two or more successive channels is allowed. (Setting a maximum of 8 channels is allowed.) Single conversion mode: Selected channel is converted only once. Sequential conversion mode: Selected channel is converted repetitively. Halt conversion mode: Conversion of selected channel is stopped and activated alternately.		
UART(SCI)	Number of channels: 1 Clock-synchronous transfer: 62.5 kbps to 2 Mbps Clock-asynchronous transfer: 9,615 bps to 500 kbps Communication is allowed by bi-directional serial communication function and master/slave type connection.		
CAN	Compliant with Ver 2.0A and Ver 2.0B CAN specifications. 8 built-in message buffers. Transmission rate of 10 kbps to 1 Mbps (by 16 MHz machine clock) CAN wake-up		

*1: Settings of DIP switch S2 for using emulation pod MB2145-507. For details, see MB2145-507 Hardware Manual
 (2.7 Power Pin solely for Emulator).

*2: MB90387S, MB90F387S

2. Packages And Product Models

Package	MB90F387, MB90F387S	MB90387, MB90387S
LQA048	◯	◯

◯ : Yes ×: No

Note: Refer to Package Dimension for details of the package.
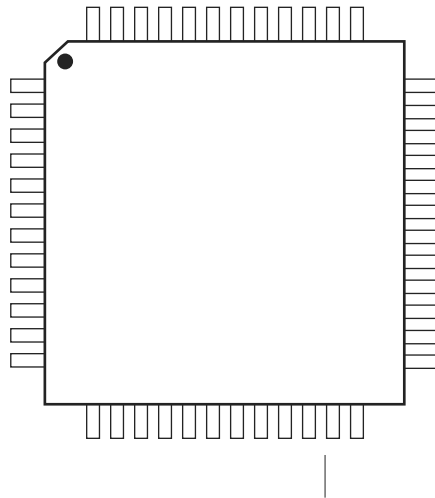
3. Product Comparison

Memory Space

When testing with test product for evaluation, check the differences between the product and a product to be used actually. Pay attention to the following points:

■ The MB90V495G has no built-in ROM. However, a special-purpose development tool allows the operations as those of one with built-in ROM. ROM capacity depends on settings on a development tool.

■ On MB90V495G, an image from FF4000$_H$ to FFFFFF$_H$ is viewed on 00 bank and an image of FE0000$_H$ to FF3FFF$_H$ is viewed only on FE bank and FF bank. (Modified on settings of a development tool.)

■ On MB90F387/F387S/387/387S, an image from FF4000$_H$ to FFFFFF$_H$ is viewed on 00 bank and an image of FE0000$_H$ to FF3FFF$_H$ is viewed only on FF bank.
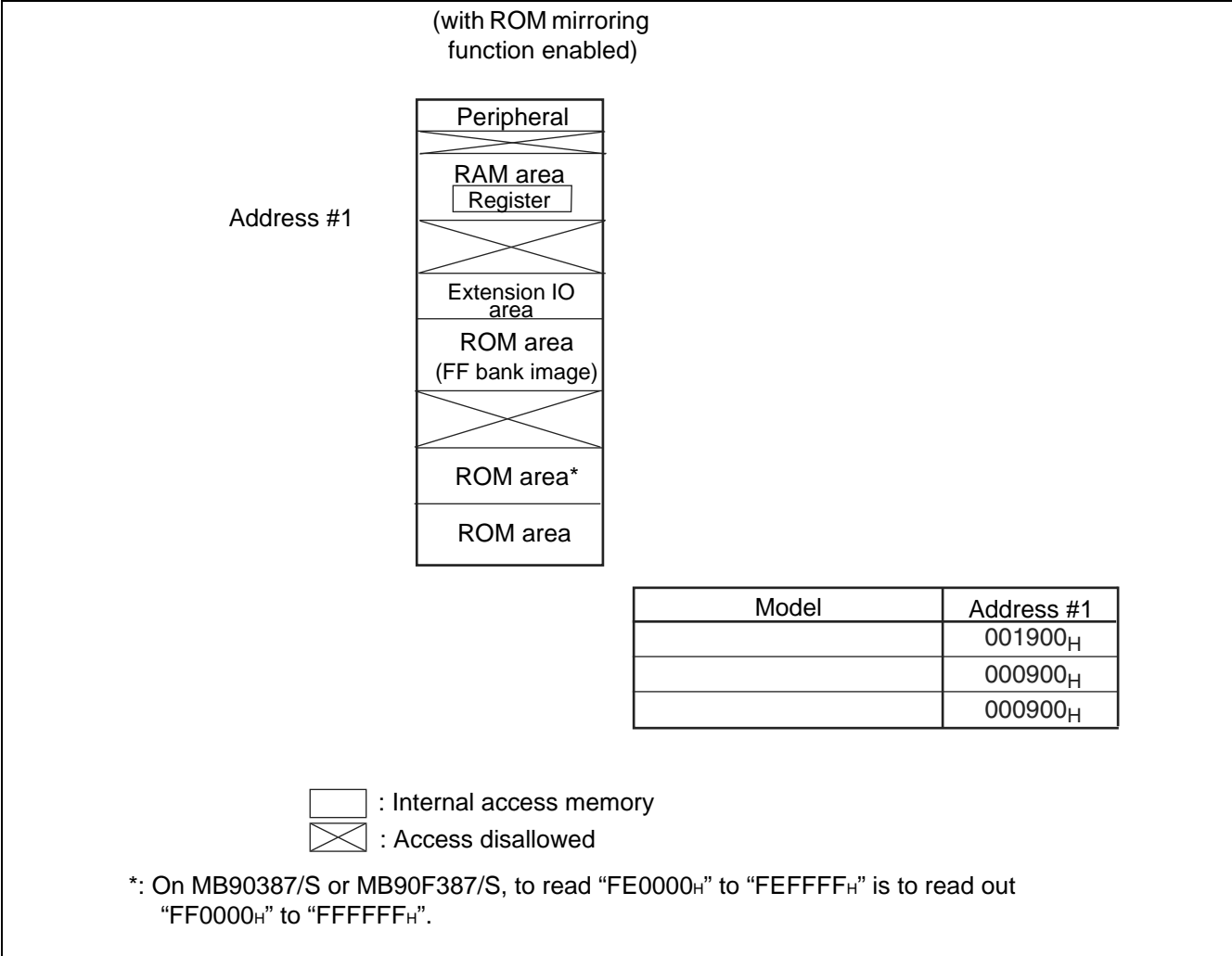
4. Pin Assignment

(Top View)

(LQA048)

*: MB90387, MB90F387   : X1A, X0A
   MB90387S, MB90F387S: P36, P35

9.2 Memory Map

(with ROM mirroring function enabled)

Address #1

| Peripheral |
| RAM area |
| Register |
| Extension IO area |
| ROM area (FF bank image) |
| ROM area* |
| ROM area |

Model	Address #1
	001900$_H$
	000900$_H$
	000900$_H$

☐ : Internal access memory

☒ : Access disallowed

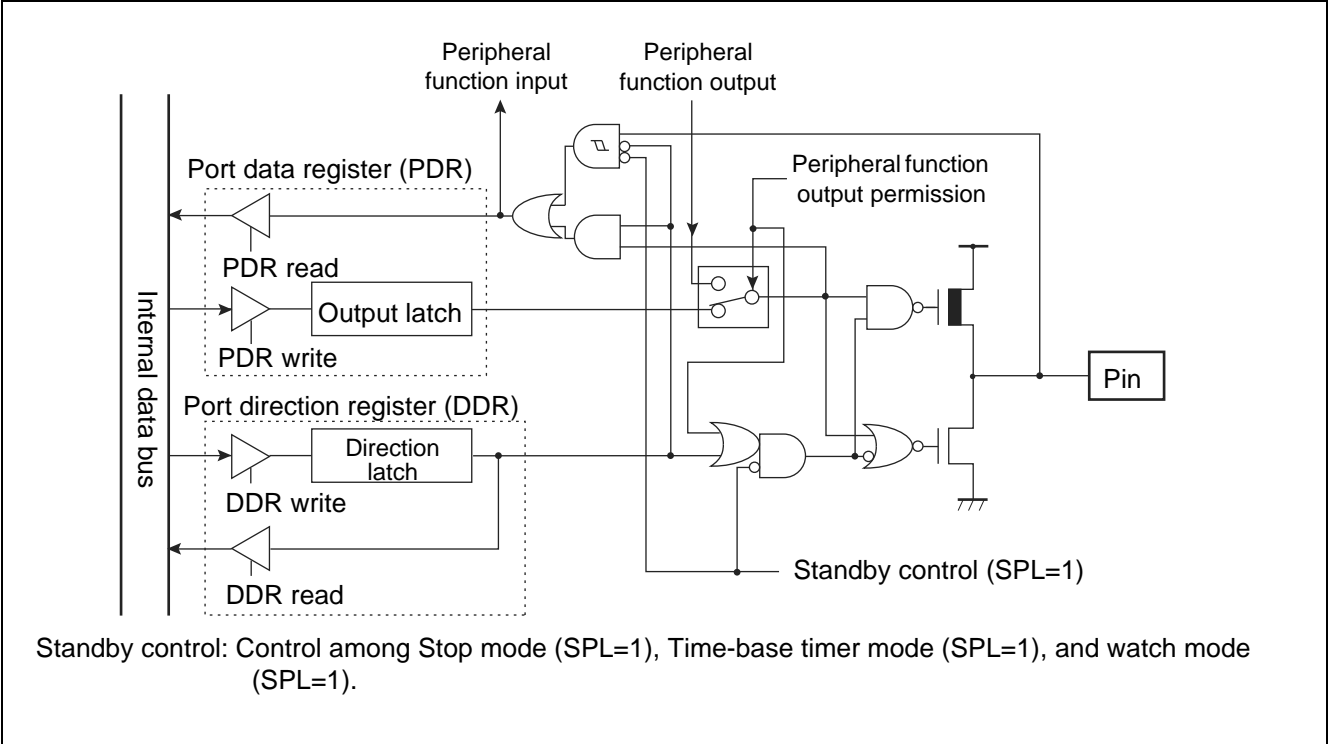*: On MB90387/S or MB90F387/S, to read "FE0000$_H$" to "FEFFFF$_H$" is to read out "FF0000$_H$" to "FFFFFF$_H$".

Note: When internal ROM is operating, F^{2}MC-16LX allows viewing ROM data image on FF bank at upper-level of 00 bank. This function is called "mirroring ROM," which allows effective use of C compiler small model.
F^{2}MC-16LX assigns the same low order 16-bit address to FF bank and 00 bank, which allows referencing table in ROM without specifying "far" using pointer.
For example, when accessing to "00C000$_H$", ROM data at "FFC000$_H$" is accessed actually. However, because ROM area of FF bank exceeds 48 Kbytes, viewing all areas is not possible on 00 bank image. Because ROM data of "FF4000$_H$" to "FFFFFF$_H$" is viewed on "004000$_H$" to "00FFFF$_H$" image, store a ROM data table in area "FF4000$_H$" to "FFFFFF$_H$."

11. Interrupt Sources, Interrupt Vectors, And Interrupt Control Registers

| Interrupt Source | EI²OS Readiness | Interrupt Vector | | Interrupt Control Register | | Priority[*3] |
		Number	Address	ICR	Address	
Reset	×	#08	08H	FFFFDCH	–	–	High
INT 9 instruction	×	#09	09H	FFFFD8H	–	–	↑
Exceptional treatment	×	#10	0AH	FFFFD4H	–	–	
CAN controller reception completed (RX)	´	#11	0BH	FFFFD0H	ICR00	0000B0H[*1]	
CAN controller transmission completed (TX) / Node status transition (NS)	´	#12	0CH	FFFFCCH			
Reserved	×	#13	0DH	FFFFC8H	ICR01	0000B1H	
Reserved	×	#14	0EH	FFFFC4H			
CAN wakeup	Δ	#15	0FH	FFFFC0H	ICR02	0000B2H[*1]	
Time-base timer	×	#16	10H	FFFFBCH			
16-bit reload timer 0	Δ	#17	11H	FFFFB8H	ICR03	0000B3H[*1]	
8/10-bit A/D converter	Δ	#18	12H	FFFFB4H			
16-bit free-run timer overflow	Δ	#19	13H	FFFFB0H	ICR04	0000B4H[*1]	
Reserved	×	#20	14H	FFFFACH			
Reserved	×	#21	15H	FFFFA8H	ICR05	0000B5H[*1]	
PPG timer ch0, ch1 underflow	´	#22	16H	FFFFA4H			
Input capture 0-input	Δ	#23	17H	FFFFA0H	ICR06	0000B6H[*1]	
External interrupt (INT4/INT5)	Δ	#24	18H	FFFF9CH			
Input capture 1-input	Δ	#25	19H	FFFF98H	ICR07	0000B7H[*2]	
PPG timer ch2, ch3 underflow	´	#26	1AH	FFFF94H			
External interrupt (INT6/INT7)	Δ	#27	1BH	FFFF90H	ICR08	0000B8H[*1]	
Watch timer	Δ	#28	1CH	FFFF8CH			
Reserved	×	#29	1DH	FFFF88H	ICR09	0000B9H[*1]	
Input capture 2-input Input capture 3-input	´	#30	1EH	FFFF84H			
Reserved	×	#31	1FH	FFFF80H	ICR10	0000BAH[*1]	
Reserved	×	#32	20H	FFFF7CH			
Reserved	×	#33	21H	FFFF78H	ICR11	0000BBH[*1]	
Reserved	×	#34	22H	FFFF74H			
Reserved	×	#35	23H	FFFF70H	ICR12	0000BCH[*1]	↓
16-bit reload timer 1	○	#36	24H	FFFF6CH			Low

Port 3 Pins Block Diagram (general-purpose input/output port)

Standby control: Control among Stop mode (SPL=1), Time-base timer mode (SPL=1), and watch mode (SPL=1).
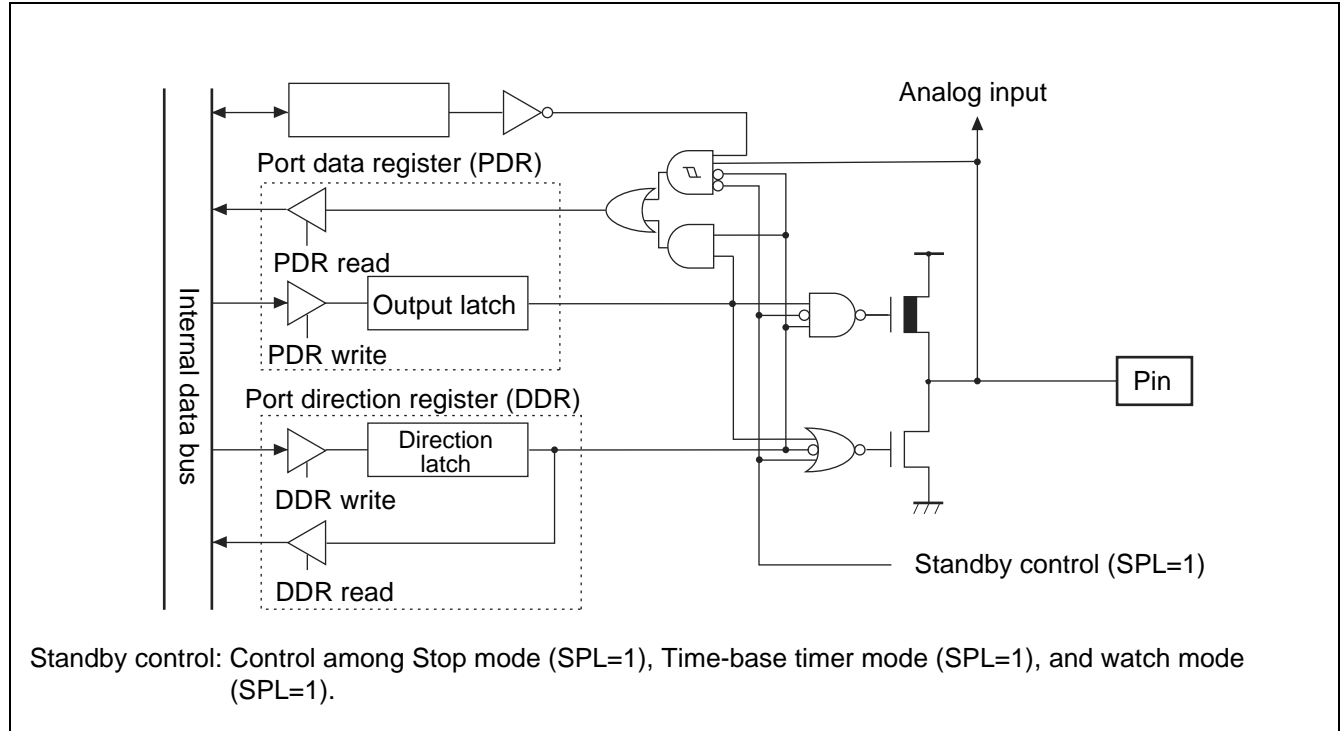
Port 3 Registers

■ Port 3 registers include port 3 data register (PDR3) and port 3 direction register (DDR3).

■ The bits configuring the register correspond to port 3 pins on a one-to-one basis.

Relation between Port 3 Registers and Pins

Port Name	Bits of Register and Corresponding Pins								
Port 3	PDR3, DDR3	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	Corresponding pins	P37	P36*	P35*	–	P33	P32	P31	P30

*: P35 and P36 do not exist on MB90387and MB90F387.

Port 5 Pins Block Diagram

Standby control: Control among Stop mode (SPL=1), Time-base timer mode (SPL=1), and watch mode
(SPL=1).

Port 5 Registers

■ Port 5 registers include port 5 data register (PDR5), port 5 direction register (DDR5), and analog input permission register (ADER).

■ Analog input permission register (ADER) allows or disallows input of analog signal to the analog input pin.

■ The bits configuring the register correspond to port 5 pins on a one-to-one basis.

Relation between Port 5 Registers and Pins

Port Name	Bits of Register and Corresponding Pins								
Port 5	PDR5, DDR5	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	ADER	ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0
	Corresponding pins	P57	P56	P55	P54	P53	P52	P51	P50

12.4 16-bit Input/Output Timer

The 16-bit input/output timer is a compound module composed of 16-bit free-run timer, (1 unit) and input capture (2 units, 4 input pins). The timer, using the 16-bit free-run timer as a basis, enables measurement of clock cycle of an input signal and its pulse width.

Configuration of 16-bit Input/Output Timer

The 16-bit input/output timer is composed of the following modules:

■ 16-bit free-run timer (1 unit)

■ Input capture (2 units, 2 input pins per unit)

Functions of 16-bit Input/Output Timer

Functions of 16-bit Free-run Timer

The 16-bit free-run timer is composed of 16-bit up counter, timer counter control status register, and prescaler. The 16-bit up counter increments in synchronization with dividing ratio of machine clock.

■ Count clock is set among four types of machine clock dividing rates.

■ Generation of interrupt is allowed by counter value overflow.

■ Activation of expanded intelligent I/O service (EI²OS) is allowed by interrupt generation.

■ Counter value of 16-bit free-run timer is cleared to "0000$_H$" by either resetting or software-clearing with timer count clear bit (TCCS: CLR).

■ Counter value of 16-bit free-run timer is output to input capture, which is available as base time for capture operation.

Functions of Input Capture

The input capture, upon detecting an edge of a signal input to the input pin from external device, stores a counter value of 16-bit free-run timer at the time of detection into the input capture data register. The function includes the input capture data registers corresponding to four input pins, input capture control status register, and edge detection circuit.

■ Rising edge, falling edge, and both edges are selectable for detection.

■ Generating interrupt on CPU is allowed by detecting an edge of input signal.

■ Expanded intelligent I/O service (EI²OS) is activated by interrupt generation.

■ The four input capture input pins and input capture data registers allows monitoring of a maximum of four events.

16-bit Input/Output Timer Block Diagram
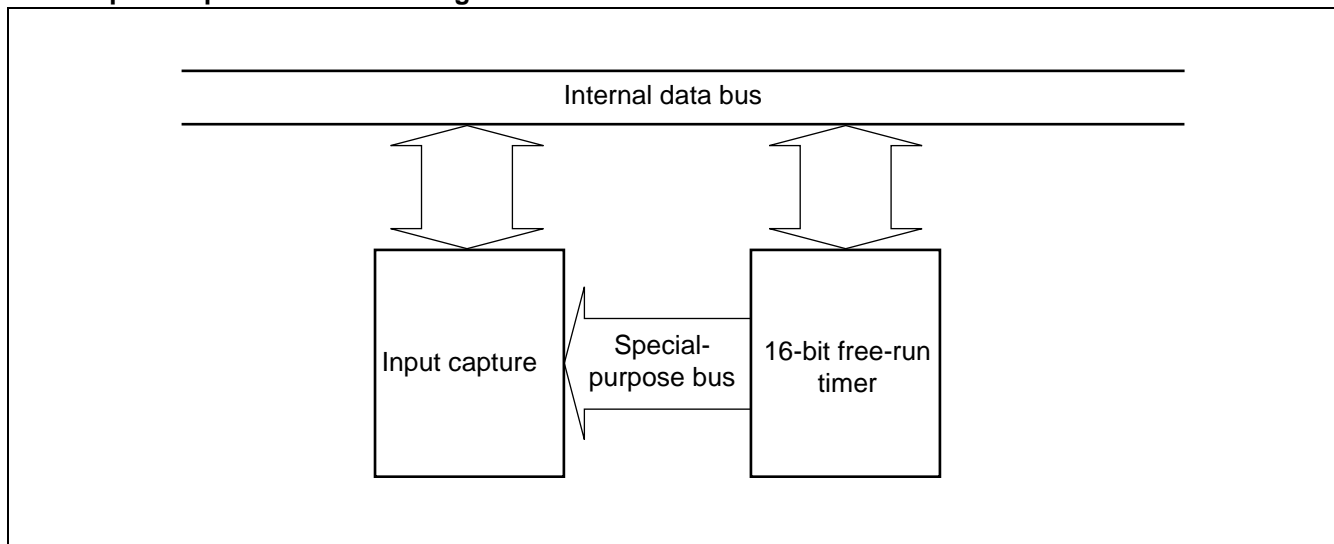
12.8 Delay Interrupt Generation Module Outline

The delay interrupt generation module is a module that generates interrupts for switching tasks. Generation of a hardware interrupt request is performed by software.

Delay Interrupt Generation Module Outline

Using the delay interrupt generation module, hardware interrupt request is generated and released by software.

Table 12-1. Delay Interrupt Generation Module Outline

	Function and Control
Cause of interrupt	Set "1" in R0 bit of delay interrupt request generation/release register (DIRR: R0=1), generating an interrupt request. Set "0" in R0 bit of delay interrupt request generation/release register (DIRR: R0=0), releasing an interrupt request.
Interrupt number	#42 (2A$_H$)
Interrupt control	No setting of permission register is provided.
Interrupt flag	Retained in DIRR: R0 bit
EI^{2}OS	Not ready for expanded intelligent I/O service.

Delay Interrupt Generation Module Block Diagram
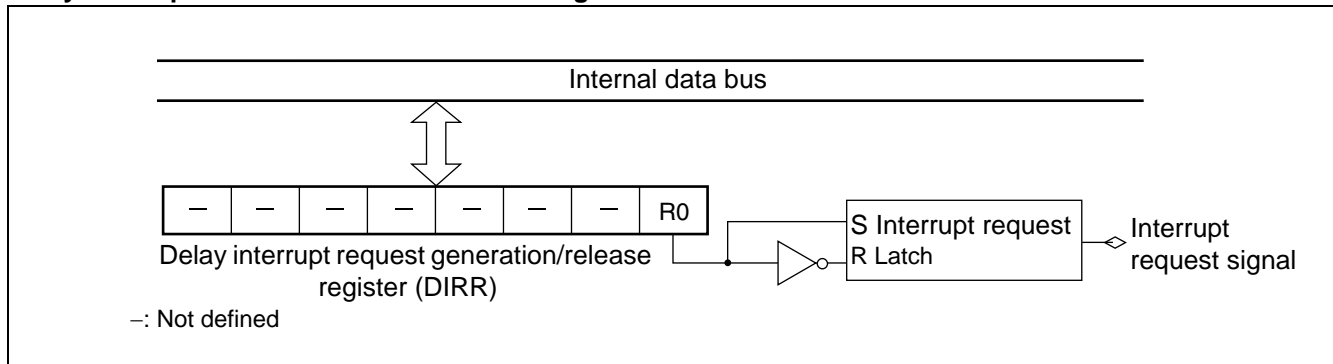
Interrupt Request Latch

A latch that retains settings on delay interrupt request generation/release register (generation or release of delay interrupt request).

Delay Interrupt Request Generation/Release Register (DIRR)

Generates or releases delay interrupt request.

Interrupt Number

An interrupt number used in delay interrupt generation module is as follows:

Interrupt number: #42 (2A$_H$)

12.11 UART Outline

UART is a general-purpose serial data communication interface for synchronous and asynchronous communication using external devices.

■ Provided with bi-directional communication function for both clock-synchronous and clock-asynchronous modes.

■ Provided with master/slave communication function (multi-processor mode). (Only master side is available.)

■ Interrupt request is generated upon completion of reception, completion of transmission and detection of reception error.

■ Ready for expanded intelligent service, EI²OS.

Table 12-3. UART Functions

	Description
Data buffer	Full-duplex double buffer
Transmission mode	Clock synchronous (No start/stop bit, no parity bit) Clock asynchronous (start-stop synchronous)
Baud rate	Built-in special-purpose baud-rate generator. Setting is selectable among 8 values. Input of external values is allowed. Use of clock from external timer (16-bit reload timer 0) is allowed.
Data length	7 bits (only asynchronous normal mode) 8 bits
Signaling system	Non Return to Zero (NRZ) system
Reception error detection	Framing error Overrun error Parity error (not detectable in operation mode 1 (multi-processor mode))
Interrupt request	Receive interrupt (reception completed, reception error detected) Transmission interrupt (transmission completed) Ready for expanded intelligent I/O service (EI²OS) in both transmission and reception
Master/slave communication function (asynchronous, multi-processor mode)	Communication between 1 (master) and n (slaves) are available (usable as master only).

Note: Start/stop bit is not added upon clock-synchronous transmission. Data only is transmitted.

Table 12-4. UART Operation Modes

Operation Mode		Data Length		Synchronization	Stop Bit Length
		With Parity	Without Parity		
0	Asynchronous mode (normal mode)	7-bit or 8-bit		Asynchronous	1- bit or 2-bit *2
1	Multi processor mode	8+1*1	–	Asynchronous	
2	Synchronous mode	8	–	Synchronous	No

−: Disallowed

1: "+1" is an address/data selection bit used for communication control (bit 11 of SCR1 register: A/D).

2: Only 1 bit is detected as a stop bit on data reception.

12.13 Address Matching Detection Function Outline

The address matching detection function checks if an address of an instruction to be processed next to a currently-processed instruction is identical with an address specified in the detection address register. If the addresses match with each other, an instruction to be processed next in program is forcibly replaced with INT9 instruction, and process branches to the interrupt process program. Using INT9 interrupt, this function is available for correcting program by batch processing.

Address Matching Detection Function Outline

■ An address of an instruction to be processed next to a currently-processed instruction of the program is always retained in an address latch via internal data bus. By the address matching detection function, the address value retained in the address latch is always compared with an address specified in detection address setting register. If the compared address values match with each other, an instruction to be processed next by CPU is forcibly replaced with INT9 instruction, and an interrupt process program is executed.

■ Two detection address setting registers are provided (PADR0 and PADR1), and each register is provided with interrupt permission bit. Generation of interrupt, which is caused by address matching between the address retained in address latch and the address specified in address setting register, is permitted and prohibited on a register-by-register basis.

Address Matching Detection Function Block Diagram
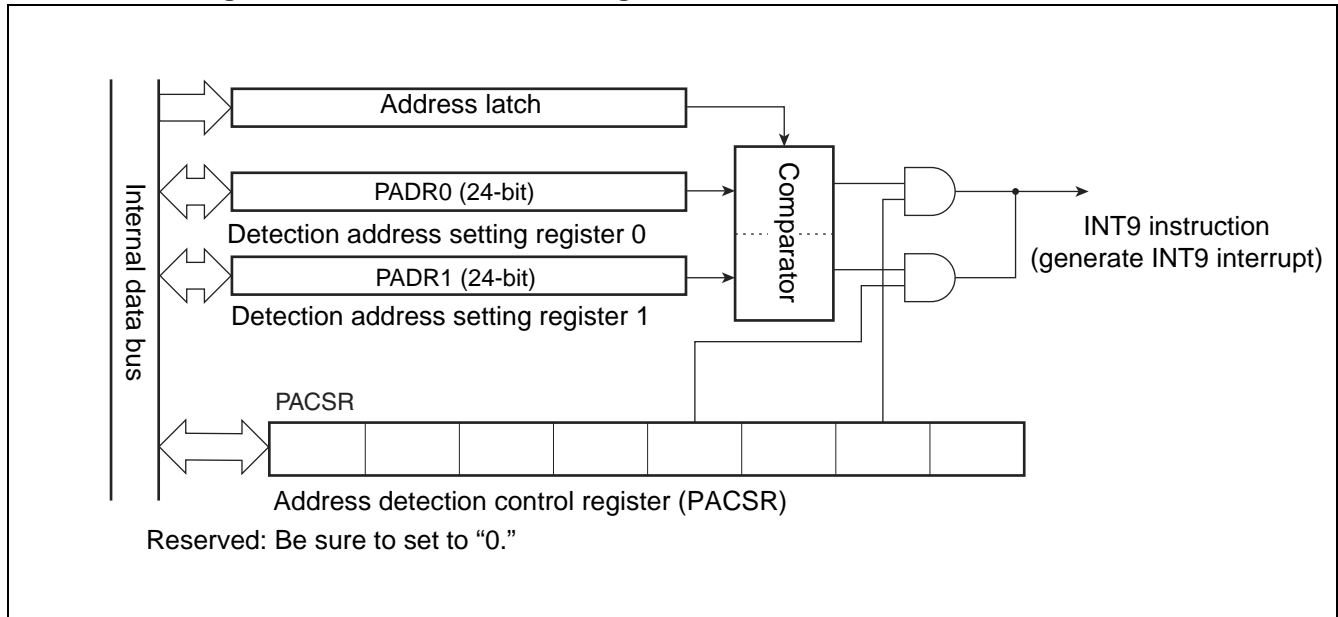
■ Address latch

　Retains address value output to internal data bus.

■ Address detection control register (PACSR)

　Specifies if interrupt is permitted or prohibited when addresses match with each other.

■ Detection address setting (PADR0, PADR1)

　Specifies addresses to be compared with values in address latch.

Sector Configuration of 512 Kbit Flash Memory

Flash memory	CPU address	Writer address*
SA0 (32 Kbytes)	FF0000H ... FF7FFFH	70000H ... 77FFFH
SA1 (8 Kbytes)	FF8000H ... FF9FFFH	78000H ... 79FFFH
SA2 (8 Kbytes)	FFA000H ... FFBFFFH	7A000H ... 7BFFFH
SA3 (16 Kbytes)	FFC000H ... FFFFFFH	7C000H ... 7FFFFH

*: "Writer address" is an address equivalent to CPU address, which is used
when data is written on Flash memory, using parallel writer. When writing/
deleting data with general-purpose writer, the writer address is used for
writing and deleting.

13. Electrical Characteristics

13.1 Absolute Maximum Rating

Parameter	Symbol	Rating		Unit	Remarks
		Min	**Max**		
Power supply voltage[1]	V_{CC}	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	
	AV_{CC}	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$V_{CC} = AV_{CC}$[2]
	AVR	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$AV_{CC} \geq AVR$[2]
Input voltage[1]	V_I	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	[3]
Output voltage[1]	V_O	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	[3]
Maximum clamp current	I_{CLAMP}	-2.0	$+2.0$	mA	[7]
Total maximum clamp current	$\Sigma \mid I_{CLAMP} \mid$	–	20	mA	[7]
"L" level maximum output current	I_{OL1}	–	15	mA	Normal output[4]
	I_{OL2}	–	40	mA	High-current output[4]
"L" level average output current	I_{OLAV1}	–	4	mA	Normal output[5]
	I_{OLAV2}	–	30	mA	High-current output[5]
"L" level maximum total output current	ΣI_{OL1}	–	125	mA	Normal output
	ΣI_{OL2}	–	160	mA	High-current output
"L" level average total output current	ΣI_{OLAV1}	–	40	mA	Normal output[6]
	ΣI_{OLAV2}	–	40	mA	High-current output[6]
"H" level maximum output current	I_{OH1}	–	-15	mA	Normal output[4]
	I_{OH2}	–	-40	mA	High-current output[4]
"H" level average output current	I_{OHAV1}	–	-4	mA	Normal output[5]
	I_{OHAV2}	–	-30	mA	High-current output[5]
"H" level maximum total output current	ΣI_{OH1}	–	-125	mA	Normal output
	ΣI_{OH2}	–	-160	mA	High-current output
"H" level average total output current	ΣI_{OHAV1}	–	-40	mA	Normal output[6]
	ΣI_{OHAV2}	–	-40	mA	High-current output[6]
Power consumption	P_D	–	245	mW	
Operating temperature	T_A	-40	$+105$	°C	
Storage temperature	Tstg	-55	$+150$	°C	

[1]: The parameter is based on $V_{SS} = AV_{SS} = 0.0$ V.

[2]: AVcc and AVR should not exceed Vcc.

[3]: V_I and V_O should not exceed Vcc + 0.3 V. However if the maximum current to/from an input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating.

[4]: A peak value of an applicable one pin is specified as a maximum output current.

[5]: An average current value of an applicable one pin within 100 ms is specified as an average output current.
   (Average value is found by multiplying operating current by operating rate.)

[6]: An average current value of all pins within 100 ms is specified as an average total output current. (Average value is found by multiplying operating current by operating rate.)

[7]:

■ Applicable to pins: P10 to P17, P20 to P27, P30 to P33, P35*, P36*, P37, P40 to P44, P50 to P57
   *: P35 and P36 are MB90387S and MB90F387S only.

■ Use within recommended operating conditions.

■ Use at DC voltage (current).

■ The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.

■ The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.

■ Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.

■ Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.

■ Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on reset.

■ Care must be taken not to leave the +B input pin open.

■ Note that analog system input/output pins other than the A/D input pins (LCD drive pins, comparator input pins, etc.) cannot accept +B signal input.

■ Sample recommended circuits:

• Input/Output Equivalent circuits
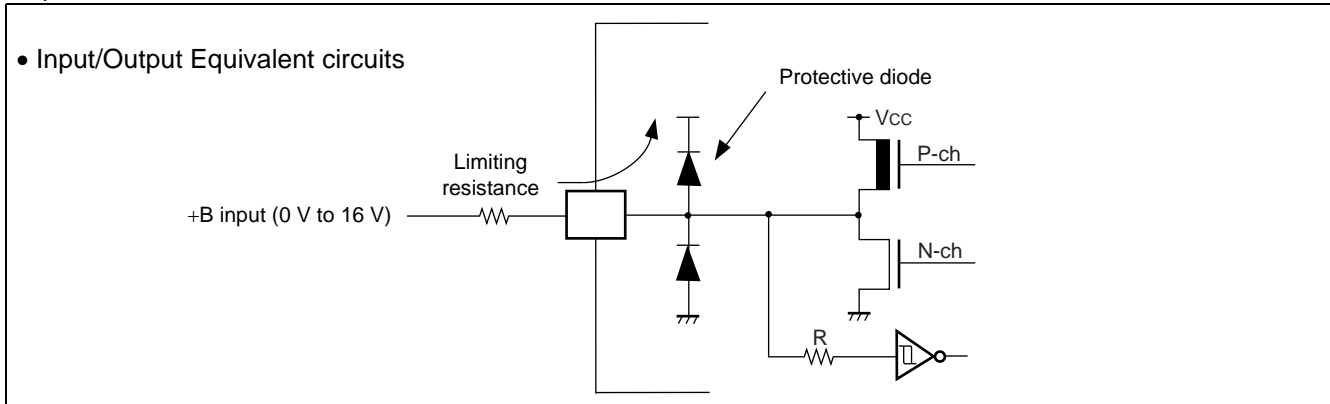
WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.
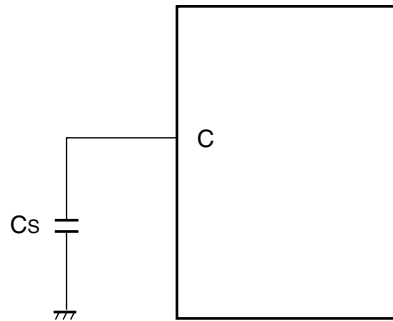
13.2 Recommended Operating Conditions

(Vss = AVss = 0.0V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	Vcc	3.5	5.0	5.5	V	Under normal operation
		3.0	–	5.5	V	Retain status of stop operation
	AVcc	4.0	–	5.5	V	*2
Smoothing capacitor	Cs	0.1	–	1.0	μF	*1
Operating temperature	TA	−40	–	+105	°C	

*1: Use a ceramic capacitor, or a capacitor of similar frequency characteristics. On the Vcc pin, use a bypass capacitor that has a larger capacity than that of Cs.
    Refer to the following figure for connection of smoothing capacitor Cs.

*2: AVcc is a voltage at which accuracy is guaranteed. AVcc should not exceed Vcc.

- C pin connection diagram

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

(Vcc = 5.0 V±10%, Vss = AVss = 0.0 V, TA = −40 °C to +105 °C)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current*	ICCL	Vcc	Vcc = 5.0 V, Internally operating at 8 kHz, subclock operation, TA = + 25°C	—	0.3	1.2	mA	MB90F387/S
				—	40	100	µA	MB90387/S
	ICCLS		Vcc = 5.0 V, Internally operating at 8 kHz, subclock, sleep mode, TA = + 25°C	—	10	30	µA	
	ICCT		Vcc = 5.0 V, Internally operating at 8 kHz, watch mode, TA = + 25°C	—	8	25	µA	
	ICCH		Stopping, TA = + 25°C	—	5	20	µA	
Input capacity	CIN	Other than AVcc, AVss, AVR, C, Vcc, Vss	–	—	5	15	pF	
Pull-up resistor	RUP	RST	–	25	50	100	kΩ	
Pull-down resistor	RDOWN	MD2	–	25	50	100	kΩ	Flash product is not provided with pull-down resistor.

*: Test conditions of power supply current are based on a device using external clock.

## 13.4 AC Characteristics

13.4.1 Clock Timing

(Vcc = 5.0 V±10%, Vss = AVss = 0.0 V, TA = −40 °C to +105 °C)

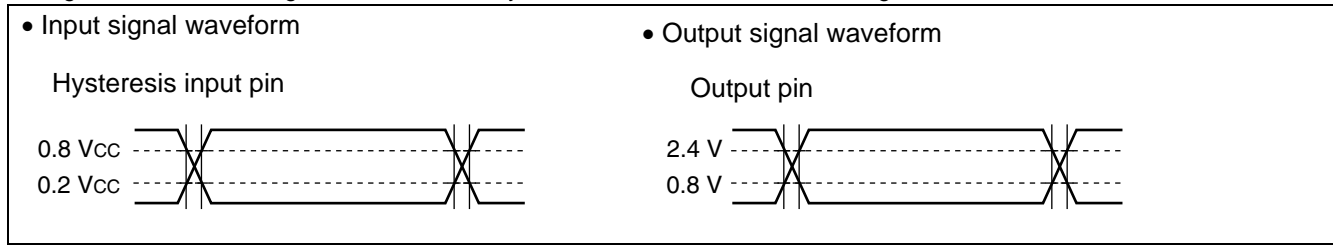| Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_C	X0, X1	3	—	8	MHz	When crystal or ceramic resonator is used[2]
			3	—	16	MHz	External clock input[1, 2]
			4	—	16	MHz	PLL Multiply by 1 [2]
			4	—	8	MHz	PLL Multiply by 2 [2]
			4	—	5.33	MHz	PLL Multiply by 3 [2]
			4	—	4	MHz	PLL Multiply by 4 [2]
	f_{CL}	X0A, X1A	—	32.768	—	kHz	
Clock cycle time	t_{HCYL}	X0, X1	125	—	333	ns	
	t_{LCYL}	X0A, X1A	—	30.5	—	μs	
Input clock pulse width	P_{WH}, P_{WL}	X0	10	—	—	ns	Set duty factor at 30% to 70% as a guideline.
	P_{WLH}, P_{WLL}	X0A	—	15.2	—	μs	
Input clock rise time and fall time	t_{CR}, t_{CF}	X0	—	—	5	ns	When external clock is used
Internal operation clock frequency	f_{CP}	—	1.5	—	16	MHz	When main clock is used
	f_{LCP}	—	—	8.192	—	kHz	When sub clock is used
Internal operation clock cycle time	t_{CP}	—	62.5	—	666	ns	When main clock is used
	t_{LCP}	—	—	122.1	—	μs	When sub clock is used

*1: Internal operation clock frequency should not exceed 16 MHz.

*2: When selecting the PLL clock, the range of clock frequency is limited. Use this product within range as mentioned in "Relation among external clock frequency and internal clock frequency".

• Clock timing
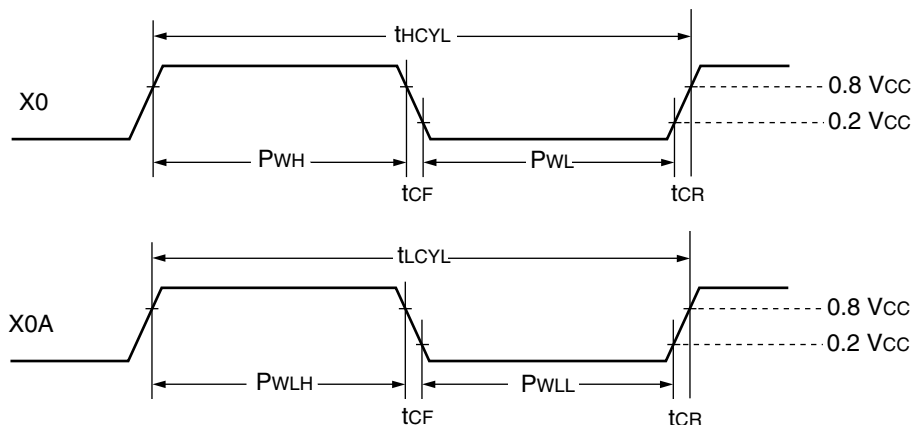
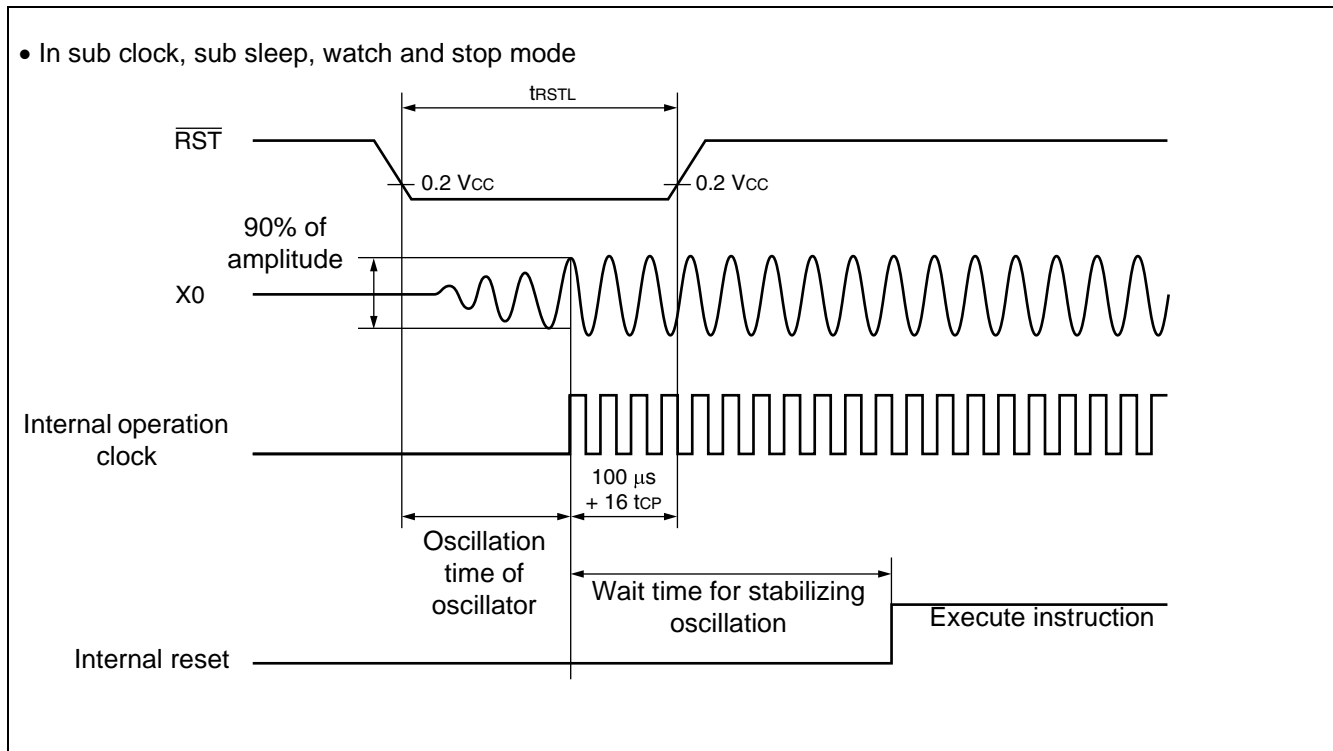Rating values of alternating current is defined by the measurement reference voltage values shown below:

• Input signal waveform	• Output signal waveform
Hysteresis input pin	Output pin

13.4.2 Reset Input Timing

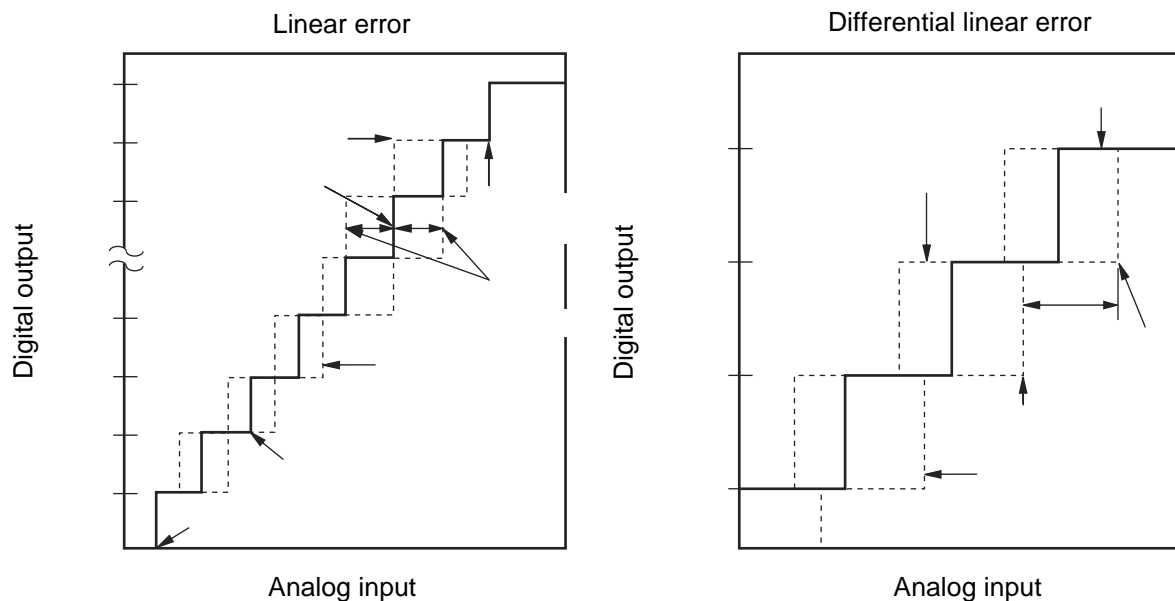| Parameter	Symbol	Pin Name	Value		Unit	Remarks
			Min	**Max**		
Reset input time	t_{RSTL}	RST	16 t_{CP}*3	–	ns	Normal operation
			Oscillation time of oscillator*1 + 100 µs + 16 t_{CP}*3	–	–	In sub clock*2, sub sleep*2, watch*2 and stop mode
			100	–	µs	In timebase timer

*1: Oscillation time of oscillator is time that the amplitude reached the 90%. In the crystal oscillator, the oscillation time is between several ms to tens of ms. In ceramic oscillator, the oscillation time is between hundreds of µs to several ms. In the external clock, the oscillation time is 0 ms.

*2: Except for MB90F387S and MB90387S.

*3: Refer to "(1) Clock timing" ratings for t_{CP} (internal operation clock cycle time).

• In sub clock, sub sleep, watch and stop mode

(Continued)

Linear error

Digital output

Analog input

Differential linear error

Digital output

Analog input

$$\text{Linear error of digital output N} = \frac{V_{NT} - \{1\ LSB \times (N-1) + V_{OT}\}}{1\ LSB}\ [LSB]$$

$$\text{Differential linear error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ LSB} - 1LSB\ [LSB]$$

$$1\ LSB = \frac{V_{FST} - V_{OT}}{1022}\ [V]$$

V_{OT}: Voltage at which digital output transits from "000$_H$" to "001$_H$."
V_{FST}: Voltage at which digital output transits from "3FE$_H$" to "3FF$_H$."

15. Ordering Information

Part Number	Package	Remarks
MB90F387PMT MB90387PMT MB90F387SPMT MB90387SPMT	48-pin plastic LQFP (LQA048)	

17. Major Changes

Spansion Publication Number: DS07-13717-5E

Page	Section	Change Results
4	■ PRODUCT LINEUP	Changed the number of channel of 8/16 bit PPG timer. or one 16-bit channel $\rightarrow$ or two 16-bit channels
13	■ BLOCK DIAGRAM	Changed the direction of arrow of TIN0, TIN1 signals of 16-bit reload timer. right arrow (output) $\rightarrow$ left arrow (input)
67	■ ELECTRIC CHARACTERISTICS 4. AC Characteristics (4) UART timing	Changed the value of Serial clock. Serial clock "H" pulse width: $4t_{CP} \rightarrow 2t_{CP}$ Serial clock "L" pulse width: $4t_{CP} \rightarrow 2t_{CP}$

NOTE: Please see "Document History" about later revised information.