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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	F ² MC-16LX
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, SCI, UART/USART
Peripherals	POR, WDT
Number of I/O	34
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90f387pmt-gs-n2e1

**DTP/External Interrupt: 4 channels, CAN wakeup:
1 channel**

- Module for activation of expanded intelligent I/O service (EI²OS), and generation of external interrupt.

Delay Interrupt Generator Module

- Generates interrupt request for task switching.

8/10-bit A/D Converter: 8 channels

- Resolution is selectable between 8-bit and 10-bit.
- Activation by external trigger input is allowed.
- Conversion time: 6.125 μ s (at 16 MHz machine clock, including sampling time)

Program Patch Function

- Address matching detection for 2 address pointers.

1. Product Lineup

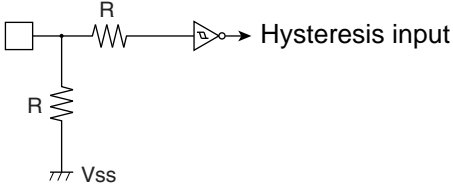
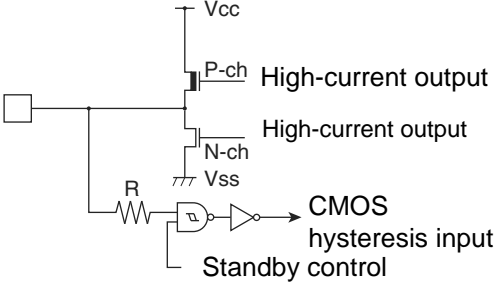
Part Number		MB90F387 MB90F387S	MB90387 MB90387S	MB90V495G
Parameter				
Classification		Flash ROM	Mask ROM	Evaluation product
ROM capacity		64 Kbytes		–
RAM capacity		2 Kbytes		6 Kbytes
Process		CMOS		
Package		LQFP-48 (pin pitch 0.50 mm)		PGA-256
Operating power supply voltage		3.5 V to 5.5 V		4.5 V to 5.5 V
Special power supply for emulator*1		–		None
CPU functions		Number of basic instructions : 351 instructions		
		Instruction bit length : 8 bits and 16 bits		
		Instruction length : 1 byte to 7 bytes		
		Data bit length : 1 bit, 8 bits, 16 bits		
		Minimum instruction execution time: 62.5 ns (at 16 MHz machine clock)		
		Interrupt processing time: 1.5 μ s at minimum (at 16 MHz machine clock)		
Low power consumption (standby) mode		Sleep mode / Watch mode / Time-base timer mode / Stop mode / CPU intermittent		
I/O port		General-purpose input/output ports (CMOS output): 34 ports (36 ports*2) including 4 high-current output ports (P14 to P17)		
Time-base timer		18-bit free-run counter Interrupt cycle: 1.024 ms, 4.096 ms, 16.834 ms, 131.072 ms (with oscillation clock frequency at 4 MHz)		
Watchdog timer		Reset generation cycle: 3.58 ms, 14.33 ms, 57.23 ms, 458.75 ms (with oscillation clock frequency at 4 MHz)		
16-bit input/output timer	16-bit free-run timer	Number of channels: 1 Interrupt upon occurrence of overflow		
	Input capture	Number of channels: 4 Retaining free-run timer value set by pin input (rising edge, falling edge, and both edges)		
16-bit reload timer		Number of channels: 2 16-bit reload timer operation Count clock cycle: 0.25 μ s, 0.5 μ s, 2.0 μ s (at 16-MHz machine clock frequency) External event count is allowed.		
Watch timer		15-bit free-run counter Interrupt cycle: 31.25 ms, 62.5 ms, 12 ms, 250 ms, 500 ms, 1.0 s, 2.0 s (with 8.192 kHz sub clock)		
8/16-bit PPG timer		Number of channels: 2 (four 8-bit channels are available also.) PPG operation is allowed with four 8-bit channels or two 16-bit channels. Outputting pulse wave of arbitrary cycle or arbitrary duty is allowed. Count clock: 62.5 ns to 1 μ s (with 16 MHz machine clock)		
Delay interrupt generator module		Interrupt generator module for task switching. Used for realtime OS.		
DTP/External interrupt		Number of inputs: 4 Activated by rising edge, falling edge, "H" level or "L" level input. External interrupt or expanded intelligent I/O service (EI ² OS) is available.		

5. Pin Description

Pin No.	Pin Name	Circuit Type	Function
1	AVcc	–	Vcc power input pin for A/D converter.
2	AVR	–	Power (Vref+) input pin for A/D converter. Use as input for Vcc or lower.
3 to 10	P50 to P57	E	General-purpose input/output ports.
	AN0 to AN7		Functions as analog input pins for A/D converter. Valid when analog input setting is "enabled."
11	P37	D	General-purpose input/output port.
	ADTG		Function as an external trigger input pin for A/D converter. Use the pin by setting as input port.
12	P20	D	General-purpose input/output port.
	TIN0		Function as an event input pin for reload timer 0. Use the pin by setting as input port.
13	P21	D	General-purpose input/output port.
	TOT0		Function as an event output pin for reload timer 0. Valid only when output setting is "enabled."
14	P22	D	General-purpose input/output port.
	TIN1		Function as an event input pin for reload timer 1. Use the pin by setting as input port.
15	P23	D	General-purpose input/output port.
	TOT1		Function as an event output pin for reload timer 1. Valid only when output setting is "enabled."
16 to 19	P24 to P27	D	General-purpose input/output ports.
	INT4 to INT7		Functions as external interrupt input pins. Use the pins by setting as input port.
20	MD2	F	Input pin for specifying operation mode. Connect directly to Vss.
21	MD1	C	Input pin for specifying operation mode. Connect directly to Vcc.
22	MD0	C	Input pin for specifying operation mode. Connect directly to Vcc.
23	RST	B	External reset input pin.
24	Vcc	–	Power source (5 V) input pin.
25	Vss	–	Power source (0 V) input pin.
26	C	–	Capacitor pin for stabilizing power source. Connect a ceramic capacitor of approximately 0.1 μ F.
27	X0	A	Pin for high-rate oscillation.
28	X1	A	Pin for high-rate oscillation.
29 to 32	P10 to P13	D	General-purpose input/output ports.
	IN0 to IN3		Functions as trigger input pins of input capture ch.0 to ch.3. Use the pins by setting as input ports.
33 to 36	P14 to P17	G	General-purpose input/output ports. High-current output ports.
	PPG0 to PPG3		Functions as output pins of PPG timers 01 and 23. Valid when output setting is "enabled."
37	P40	D	General-purpose input/output port.
	SIN1		Serial data input pin for UART. Use the pin by setting as input port.
38	P41	D	General-purpose input/output port.
	SCK1		Serial clock input pin for UART. Valid only when serial clock input/output setting on UART is "enabled."

6. I/O Circuit Type

Type	Circuit	Remarks
A		<ul style="list-style-type: none"> ■ High-rate oscillation feedback resistor, approx.1 MΩ ■ Low-rate oscillation feedback resistor, approx.10 MΩ
B		<ul style="list-style-type: none"> ■ Hysteresis input with pull-up resistor. ■ Pull-up resistor, approx.50 kΩ
C		<ul style="list-style-type: none"> ■ Hysteresis input
D		<ul style="list-style-type: none"> ■ CMOS hysteresis input ■ CMOS level output ■ Standby control provided
E		<ul style="list-style-type: none"> ■ CMOS hysteresis input ■ CMOS level output ■ Shared for analog input pin ■ Standby control provided

Type	Circuit	Remarks
F		<ul style="list-style-type: none"> ■ Hysteresis input with pull-down resistor ■ Pull-down resistor, approx. 50 kΩ ■ Flash product is not provided with pull-down resistor.
G		<ul style="list-style-type: none"> ■ CMOS hysteresis input ■ CMOS level output (high-current output) ■ Standby control provided

7. Handling Devices

Do Not Exceed Maximum Rating (preventing “latch up”)

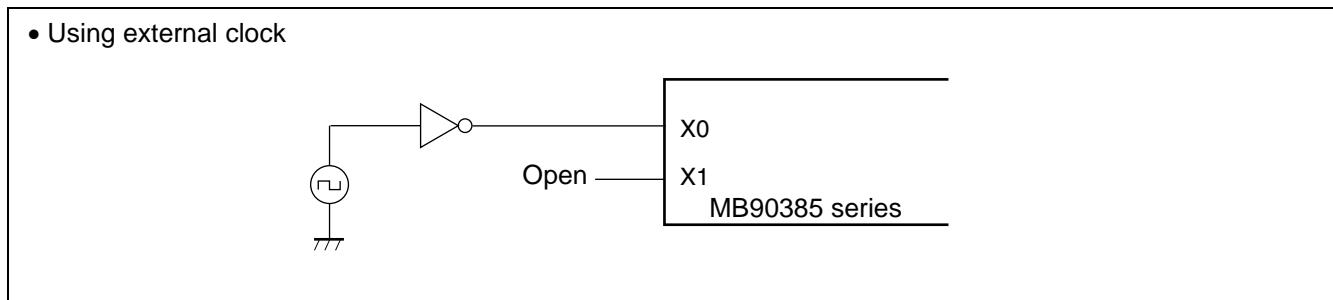
- On a CMOS IC, latch-up may occur when applying a voltage higher than Vcc or a voltage lower than Vss to input or output pin, which has no middle or high withstand voltage. Latch-up may also occur when a voltage exceeding maximum rating is applied across Vcc pin and Vss pin.
- Latch-up causes drastic increase of power current, which may lead to destruction of elements by heat. Extreme caution must be taken not to exceed maximum rating.
- When turning on and off analog power source, take extra care not to apply an analog power voltages (AVcc and AVR) and analog input voltage that are higher than digital power voltage (Vcc).

Handling Unused Pins

- Leaving unused input pins open may cause permanent destruction by malfunction or latch-up. Apply pull-up or pull-down process to the unused pins using resistors of 2 k Ω or higher. Leave unused input/output pins open under output status, or process as input pins if they are under input status.

Using External Clock

- When using an external clock, drive only X0 pin and leave X1 pin open. An example of using an external clock is shown below.



Notes When Using No Sub Clock

- If an oscillator is not connected to X0A and X1A pin, apply pull-down resistor to X0A pin and leave X1A pin open.

About Power Supply Pins

- If two or more Vcc and Vss pins exist, the pins that should be at the same potential are connected to each other inside the device. For reducing unwanted emissions and preventing malfunction of strobe signals caused by increase of ground level, however, be sure to connect the Vcc and Vss pins to the power source and the ground externally.
- Pay attention to connect a power supply to Vcc and Vss of MB90385 series device in a lowest-possible impedance.
- Near pins of MB90385 series device, connecting a bypass capacitor is recommended at 0.1 μ F across Vcc pin and Vss pin.

Crystal Oscillator Circuit

- Noises around X0 and X1 pins cause malfunctions on a MB90385 series device. Design a print circuit so that X0 and X1 pins, an crystal oscillator (or a ceramic oscillator), and bypass capacitor to the ground become as close as possible to each other. Furthermore, avoid wires to X0 and X1 pins crossing each other as much as possible.
- Print circuit designing that surrounds X0 and X1 pins with grounding wires, which ensures stable operation, is strongly recommended.

Caution on Operations during PLL Clock Mode

- If the PLL clock mode is selected, the microcontroller attempt to be working with the self-oscillating circuit even when there is no external oscillator or external clock input is stopped. Performance of this operation, however, cannot be guaranteed.

Sequence of Turning on Power of A/D Converter and Applying Analog Input

- Be sure to turn on digital power (Vcc) before applying signals to the A/D converter and applying analog input signals (AN0 to AN7 pins).
- Be sure to turn off the power of A/D converter and analog input before turning off the digital power source.
- Be sure not to apply AVR exceeding AVcc when turning on and off. (No problems occur if analog and digital power is turned on and off simultaneously.)

Handling Pins When A/D Converter is Not Used

- If the A/D converter is not used, connect the pins under the following conditions: "AVcc=AVR=Vcc," and "AVss=Vss"

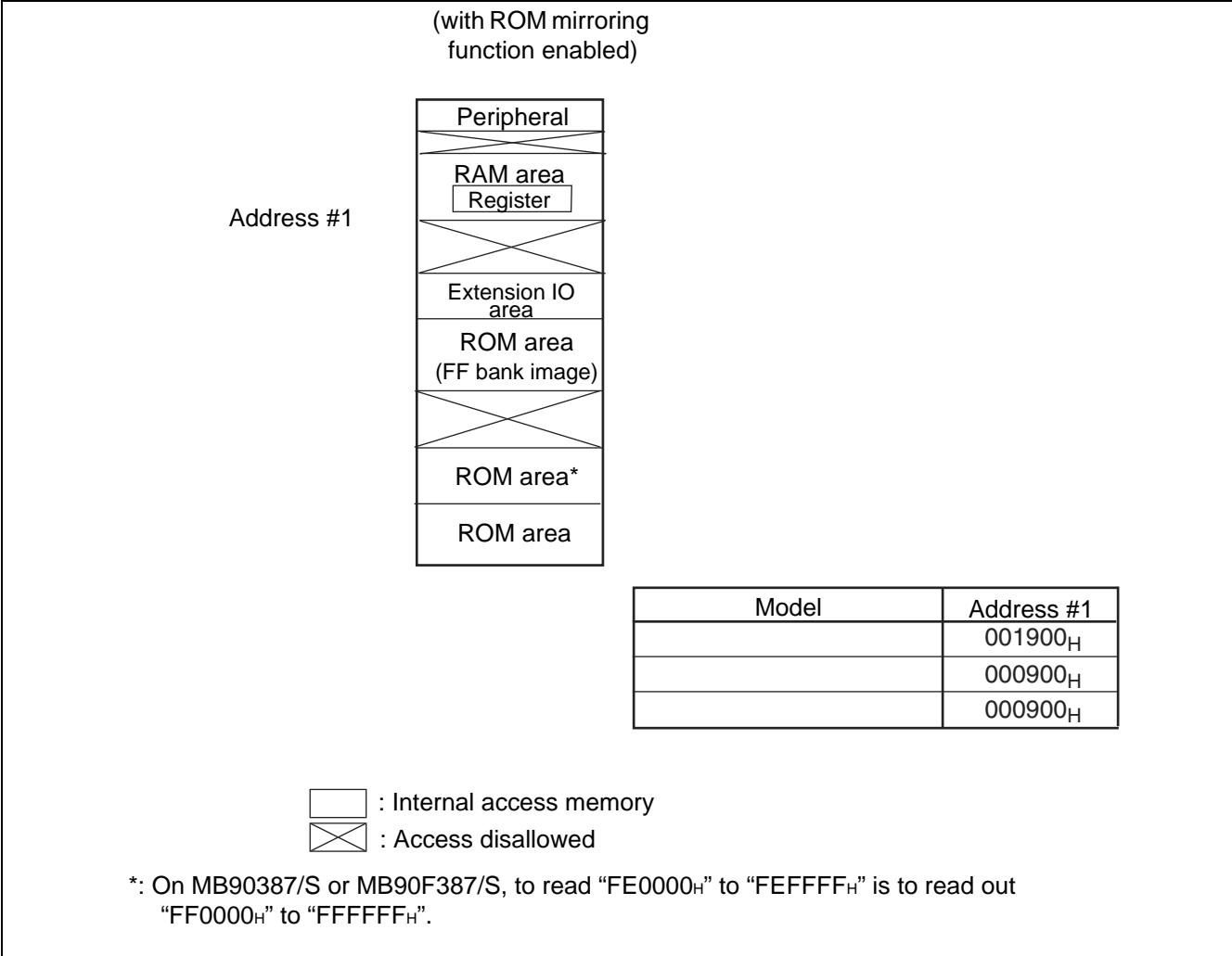
Note on Turning on Power

- For preventing malfunctions on built-in step-down circuit, maintain a minimum of 50 μ s of voltage rising time (between 0.2 V and 2.7V) when turning on the power.

Stabilization of Supply Voltage

- A sudden change in the supply voltage may cause the device to malfunction even within the specified Vcc supply voltage operating range. Therefore, the Vcc supply voltage should be stabilized.
For reference, the supply voltage should be controlled so that Vcc ripple variations (peak-to-peak values) at commercial frequencies (50 Hz / 60 Hz) fall below 10% of the standard Vcc supply voltage and the coefficient of fluctuation does not exceed 0.1 V/ms at instantaneous power switching.

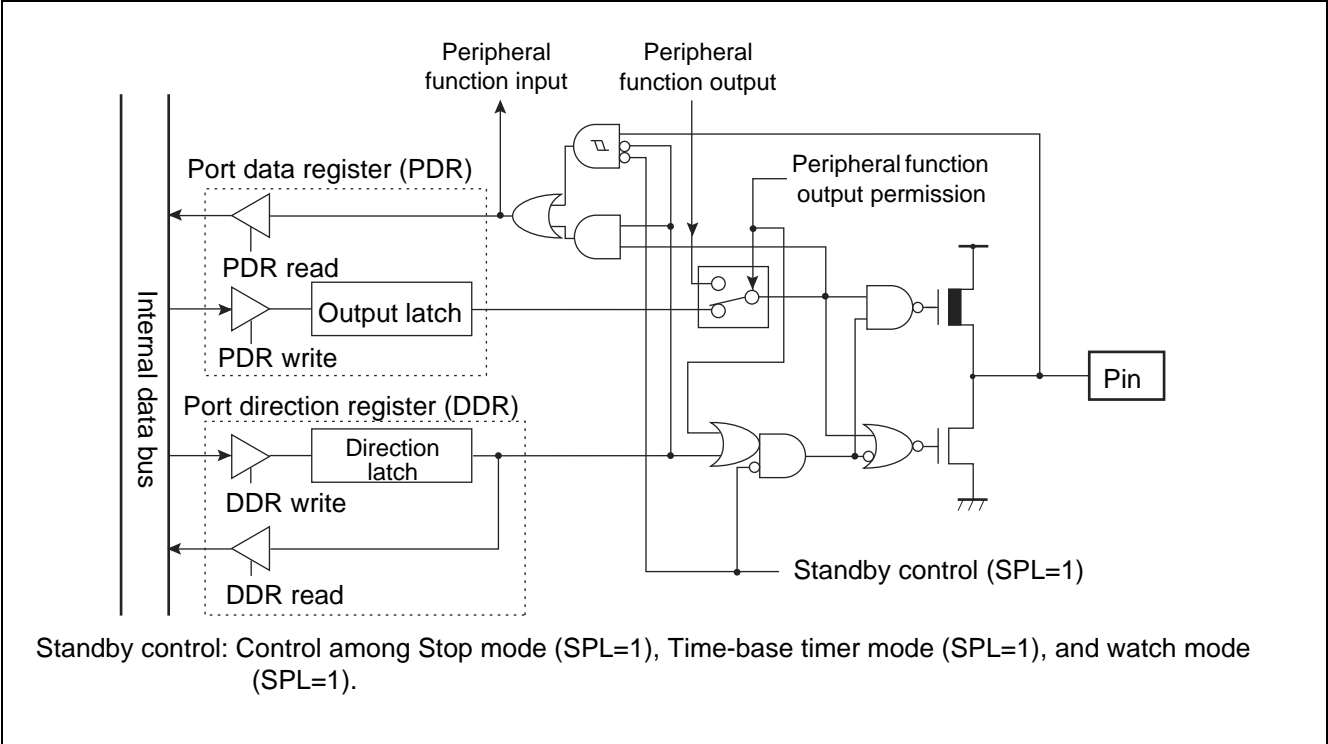
9.2 Memory Map



Note: When internal ROM is operating, F²MC-16LX allows viewing ROM data image on FF bank at upper-level of 00 bank. This function is called “mirroring ROM,” which allows effective use of C compiler small model. F²MC-16LX assigns the same low order 16-bit address to FF bank and 00 bank, which allows referencing table in ROM without specifying “far” using pointer. For example, when accessing to “00C000_H”, ROM data at “FFC000_H” is accessed actually. However, because ROM area of FF bank exceeds 48 Kbytes, viewing all areas is not possible on 00 bank image. Because ROM data of “FF4000_H” to “FFFFFF_H” is viewed on “004000_H” to “00FFFF_H” image, store a ROM data table in area “FF4000_H” to “FFFFFF_H”.

Address	Register Abbreviation	Register	Read/Write	Resource	Initial Value
003C38 _H , 003C39 _H	DLCR4	DLC register 4	R/W	CAN controller	XXXXXXXX _B , XXXXXXXX _B
003C3A _H , 003C3B _H	DLCR5	DLC register 5	R/W		XXXXXXXX _B , XXXXXXXX _B
003C3C _H , 003C3D _H	DLCR6	DLC register 6	R/W		XXXXXXXX _B , XXXXXXXX _B
003C3E _H , 003C3F _H	DLCR7	DLC register 7	R/W		XXXXXXXX _B , XXXXXXXX _B
003C40 _H to 003C47 _H	DTR0	Data register 0	R/W		XXXXXXXX _B to XXXXXXXX _B
003C48 _H to 003C4F _H	DTR1	Data register 1	R/W		XXXXXXXX _B to XXXXXXXX _B
003C50 _H to 003C57 _H	DTR2	Data register 2	R/W		XXXXXXXX _B to XXXXXXXX _B
003C58 _H to 003C5F _H	DTR3	Data register 3	R/W		XXXXXXXX _B to XXXXXXXX _B
003C60 _H to 003C67 _H	DTR4	Data register 4	R/W		XXXXXXXX _B to XXXXXXXX _B
003C68 _H to 003C6F _H	DTR5	Data register 5	R/W		XXXXXXXX _B to XXXXXXXX _B
003C70 _H to 003C77 _H	DTR6	Data register 6	R/W		XXXXXXXX _B to XXXXXXXX _B
003C78 _H to 003C7F _H	DTR7	Data register 7	R/W		XXXXXXXX _B to XXXXXXXX _B
003C80 _H to 003CFF _H	(Reserved area) *				
003D00 _H , 003D01 _H	CSR	Control status register	R/W, R	CAN controller	0XXXX001 _B , 00XXX000 _B
003D02 _H	LEIR	Last event display register	R/W		000XX000 _B
003D03 _H	(Reserved area) *				
003D04 _H , 003D05 _H	RTEC	Send/receive error counter	R	CAN controller	00000000 _B , 00000000 _B
003D06 _H , 003D07 _H	BTR	Bit timing register	R/W		11111111 _B , X1111111 _B
003D08 _H	IDER	IDE register	R/W		XXXXXXXX _B
003D09 _H	(Reserved area) *				
003D0A _H	TRTRR	Send RTR register	R/W	CAN controller	00000000 _B
003D0B _H	(Reserved area) *				
003D0C _H	RFWTR	Remote frame receive wait register	R/W	CAN controller	XXXXXXXX _B

Port 3 Pins Block Diagram (general-purpose input/output port)



Port 3 Registers

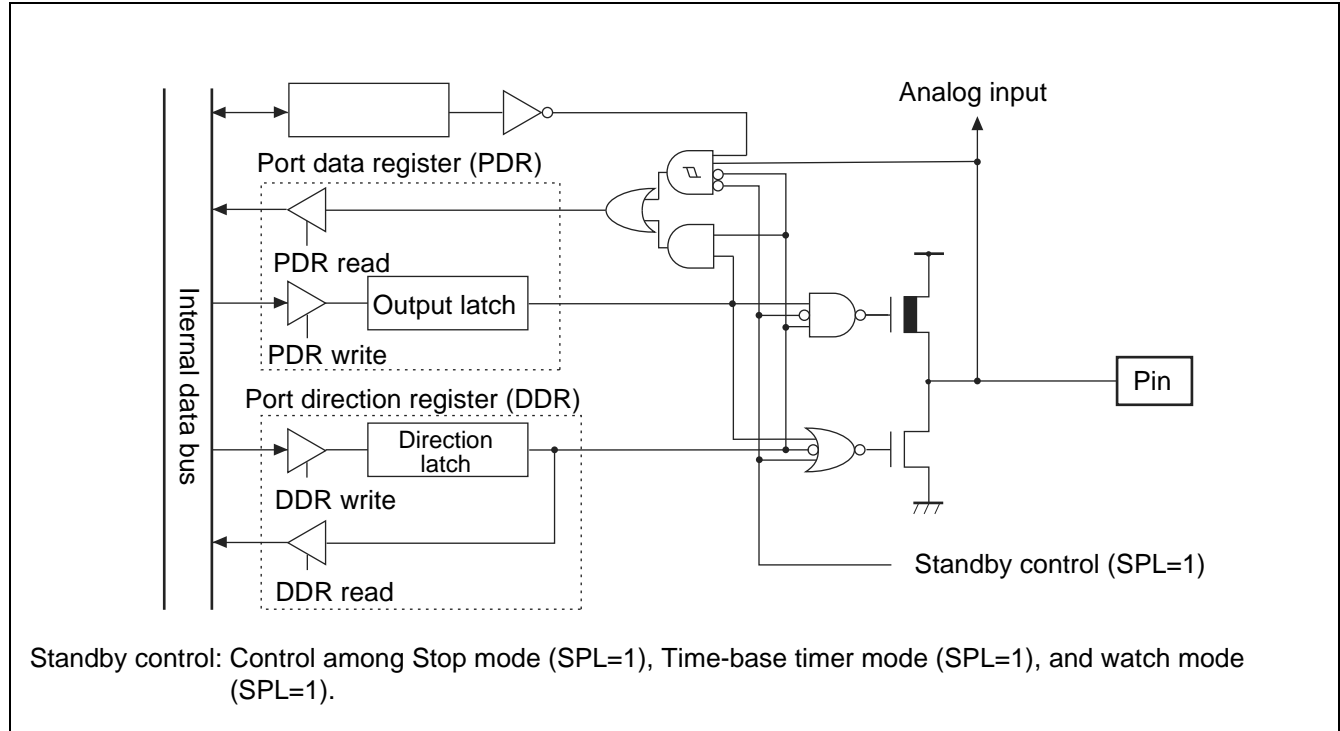
- Port 3 registers include port 3 data register (PDR3) and port 3 direction register (DDR3).
- The bits configuring the register correspond to port 3 pins on a one-to-one basis.

Relation between Port 3 Registers and Pins

Port Name	Bits of Register and Corresponding Pins								
Port 3	PDR3, DDR3	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	Corresponding pins	P37	P36*	P35*	–	P33	P32	P31	P30

*: P35 and P36 do not exist on MB90387and MB90F387.

Port 5 Pins Block Diagram



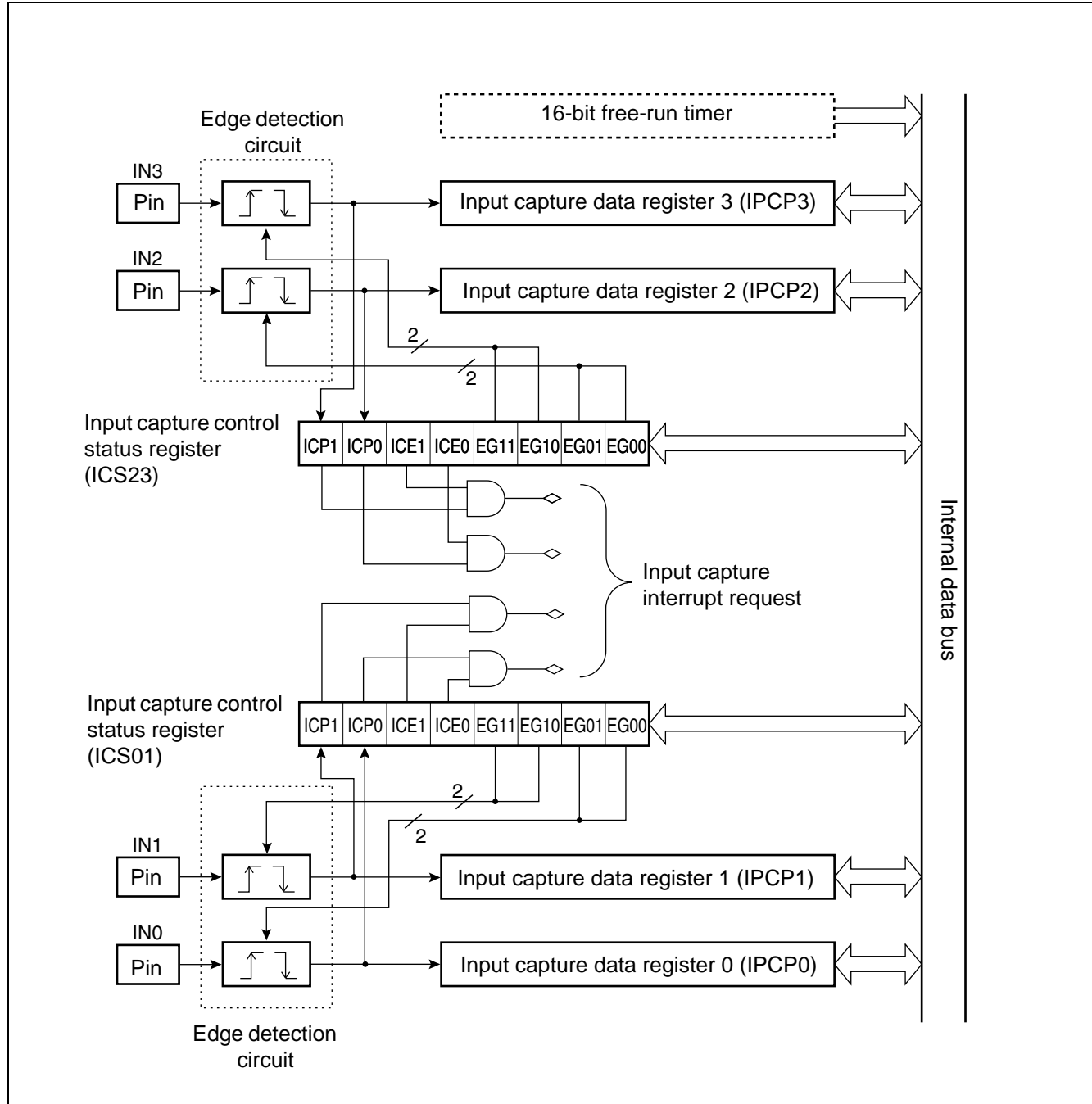
Port 5 Registers

- Port 5 registers include port 5 data register (PDR5), port 5 direction register (DDR5), and analog input permission register (ADER).
- Analog input permission register (ADER) allows or disallows input of analog signal to the analog input pin.
- The bits configuring the register correspond to port 5 pins on a one-to-one basis.

Relation between Port 5 Registers and Pins

Port Name	Bits of Register and Corresponding Pins								
Port 5	PDR5, DDR5	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	ADER	ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0
	Corresponding pins	P57	P56	P55	P54	P53	P52	P51	P50

Input Capture Block Diagram



12.6 Watch Timer Outline

The watch timer is a 15-bit free-run counter that increments in synchronization with sub clock.

- Interval time is selectable among 7 choices, and generation of interrupt request is allowed for each interval.
- Provides operation clock to the subclock oscillation stabilizing wait timer and watchdog timer.
- Always uses subclock as a count clock regardless of settings of clock selection register (CKSCR).

Interval Timer Function

- In the watch timer, a bit corresponding to the interval time overflows (carry-over) when an interval time, which is specified by interval time selection bit, is reached. Then overflow flag bit is set (WTC: WTOF=1).
- If an interrupt by overflow is permitted (WTC: WTIE=1), an interrupt request is generated upon setting an overflow flag bit.
- Interval time of watch timer is selectable among the following seven choices:

Interval Time of Watch Timer

Sub Clock Cycle	Interval Time
1/SCLK (122 μ s)	2^8 /SCLK (31.25 ms)
	2^9 /SCLK (62.5 ms)
	2^{10} /SCLK (125 ms)
	2^{11} /SCLK (250 ms)
	2^{12} /SCLK (500 ms)
	2^{13} /SCLK (1.0 s)
	2^{14} /SCLK (2.0 s)

SCLK: Sub clock frequency

Values in parentheses “()” are calculation when operating with 8.192 kHz clock.

12.11 UART Outline

UART is a general-purpose serial data communication interface for synchronous and asynchronous communication using external devices.

- Provided with bi-directional communication function for both clock-synchronous and clock-asynchronous modes.
- Provided with master/slave communication function (multi-processor mode). (Only master side is available.)
- Interrupt request is generated upon completion of reception, completion of transmission and detection of reception error.
- Ready for expanded intelligent service, EI²OS.

Table 12-3. UART Functions

	Description
Data buffer	Full-duplex double buffer
Transmission mode	Clock synchronous (No start/stop bit, no parity bit) Clock asynchronous (start-stop synchronous)
Baud rate	Built-in special-purpose baud-rate generator. Setting is selectable among 8 values. Input of external values is allowed. Use of clock from external timer (16-bit reload timer 0) is allowed.
Data length	7 bits (only asynchronous normal mode) 8 bits
Signaling system	Non Return to Zero (NRZ) system
Reception error detection	Framing error Overrun error Parity error (not detectable in operation mode 1 (multi-processor mode))
Interrupt request	Receive interrupt (reception completed, reception error detected) Transmission interrupt (transmission completed) Ready for expanded intelligent I/O service (EI ² OS) in both transmission and reception
Master/slave communication function (asynchronous, multi-processor mode)	Communication between 1 (master) and n (slaves) are available (usable as master only).

Note: Start/stop bit is not added upon clock-synchronous transmission. Data only is transmitted.

Table 12-4. UART Operation Modes

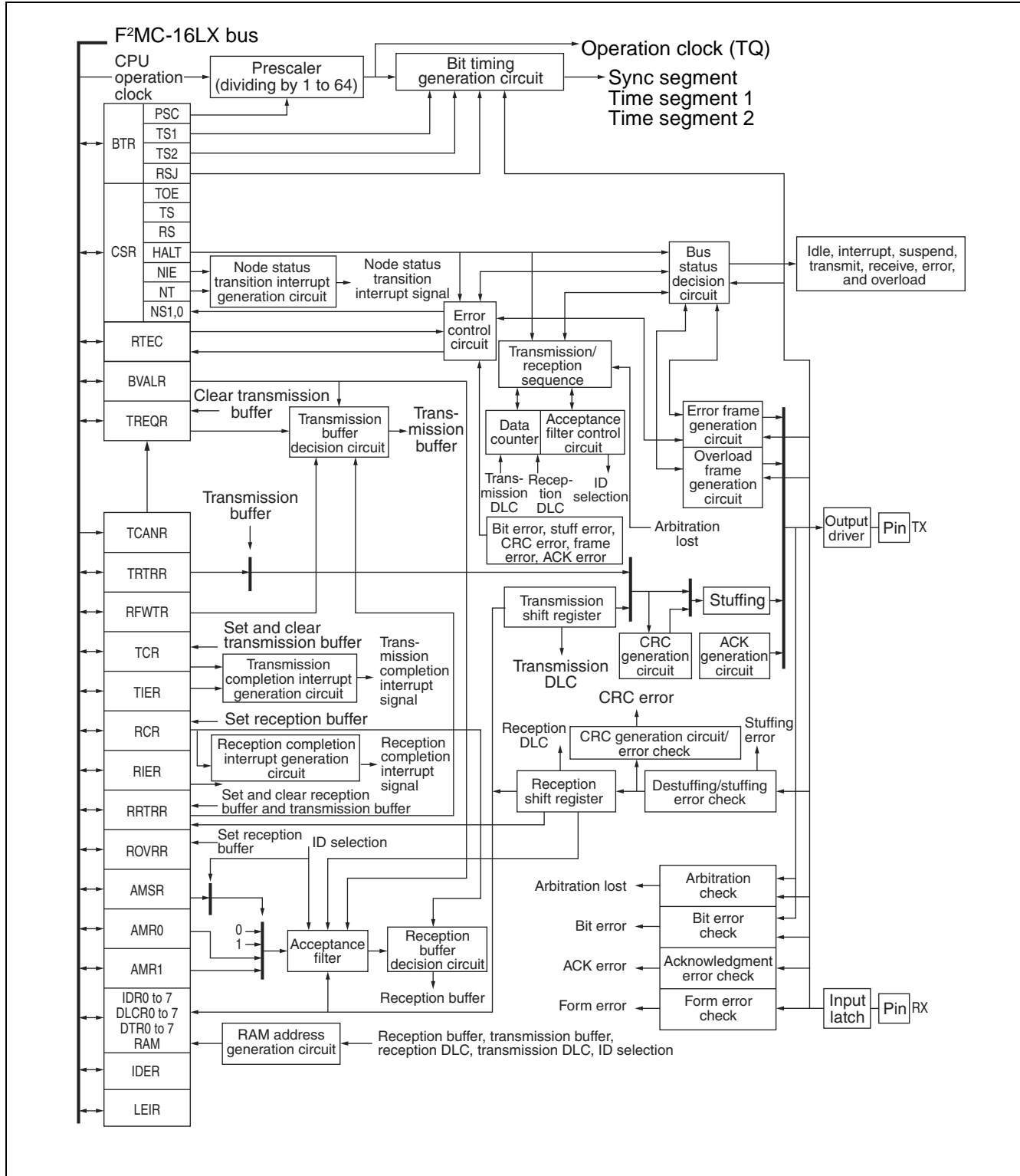
Operation Mode		Data Length		Synchronization	Stop Bit Length
		With Parity	Without Parity		
0	Asynchronous mode (normal mode)	7-bit or 8-bit		Asynchronous	1- bit or 2-bit *2
1	Multi processor mode	8+1 *1	—	Asynchronous	
2	Synchronous mode	8	—	Synchronous	No

—: Disallowed

1: "+1" is an address/data selection bit used for communication control (bit 11 of SCR1 register: A/D).

2: Only 1 bit is detected as a stop bit on data reception.

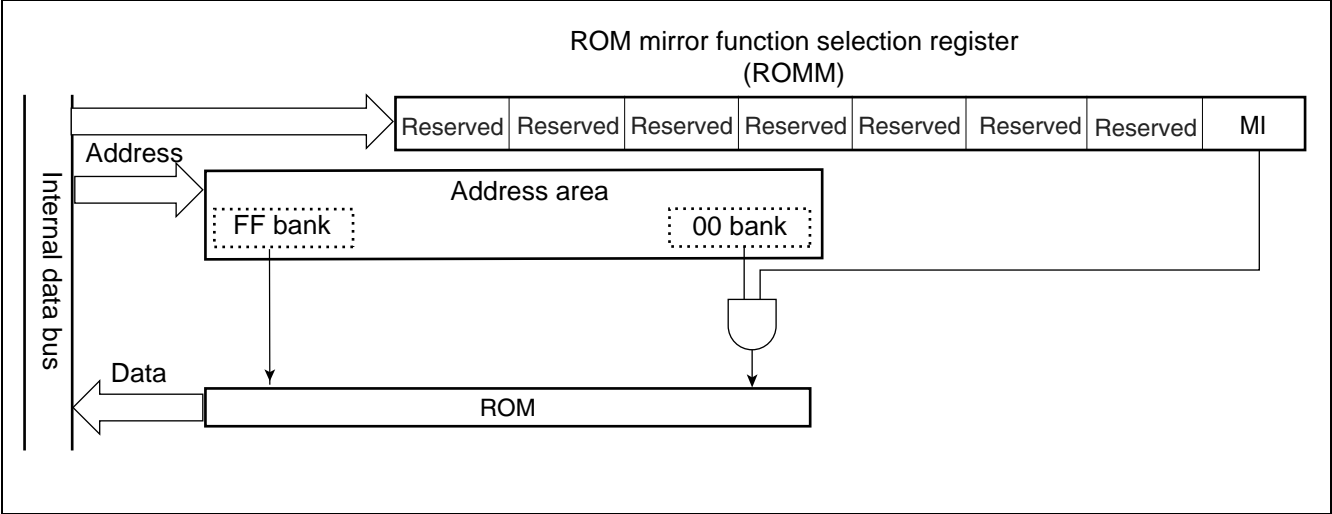
CAN Controller Block Diagram



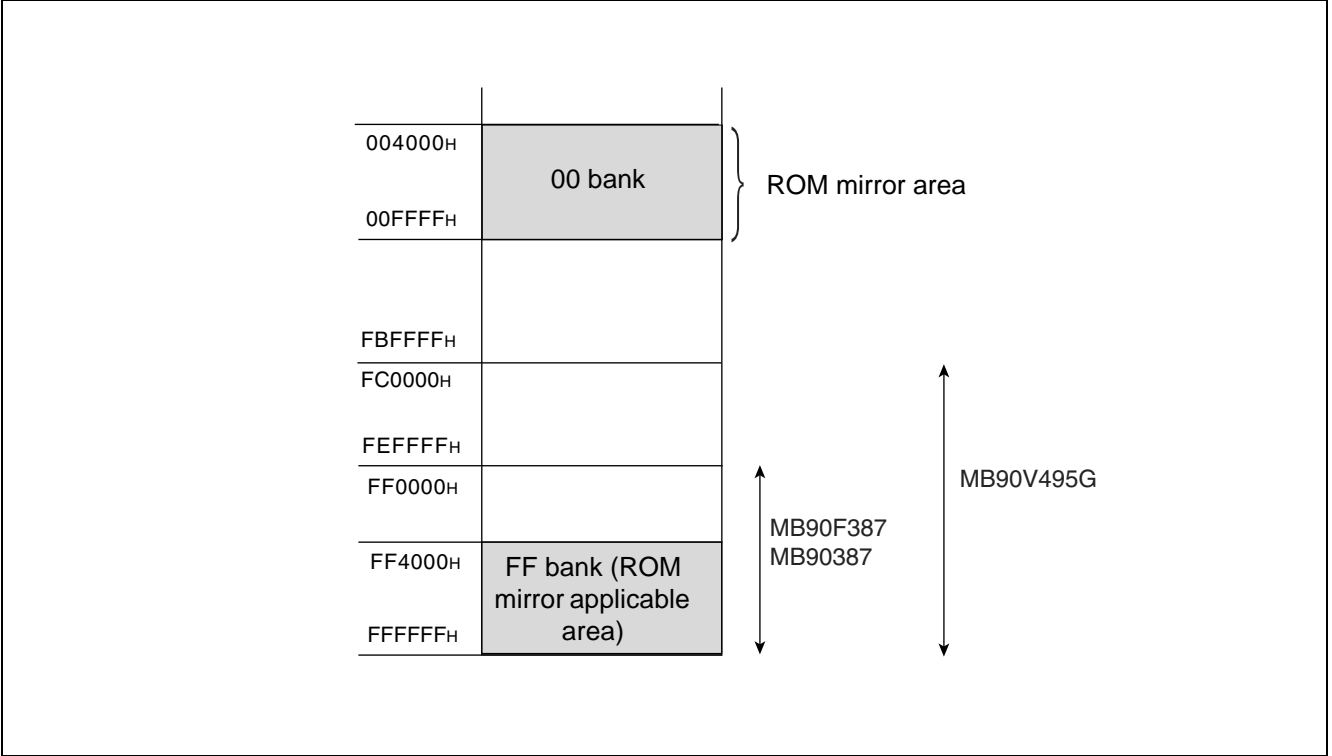
12.14 ROM Mirror Function Selection Module Outline

The ROM mirror function selection module sets the data in ROM assigned to FF bank so that the data is read by access to 00 bank.

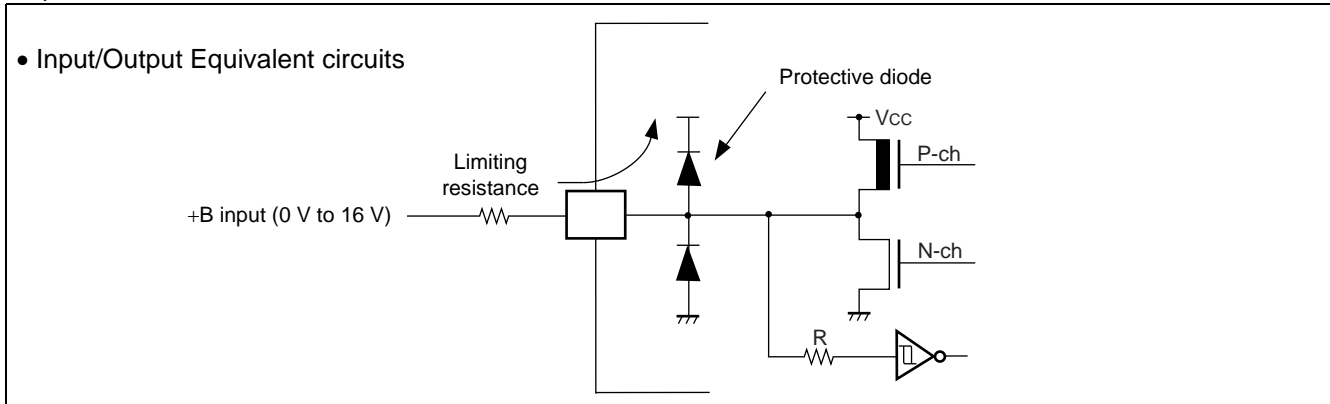
ROM Mirror Function Selection Module Block Diagram



FF Bank Access by ROM Mirror Function

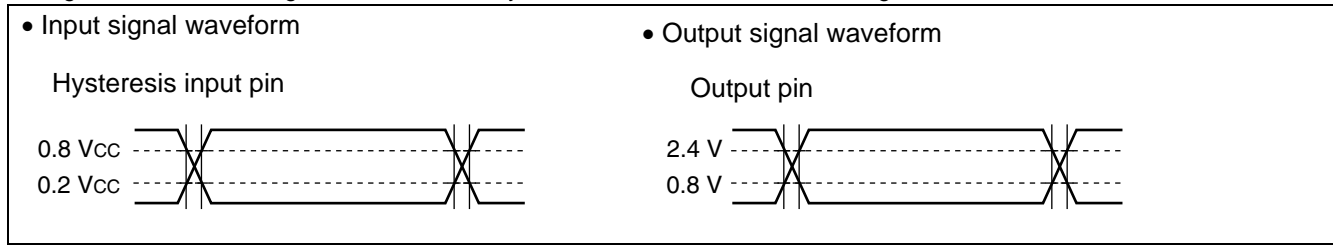


- Use within recommended operating conditions.
- Use at DC voltage (current).
- The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on reset.
- Care must be taken not to leave the +B input pin open.
- Note that analog system input/output pins other than the A/D input pins (LCD drive pins, comparator input pins, etc.) cannot accept +B signal input.
- Sample recommended circuits:



WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

Rating values of alternating current is defined by the measurement reference voltage values shown below:



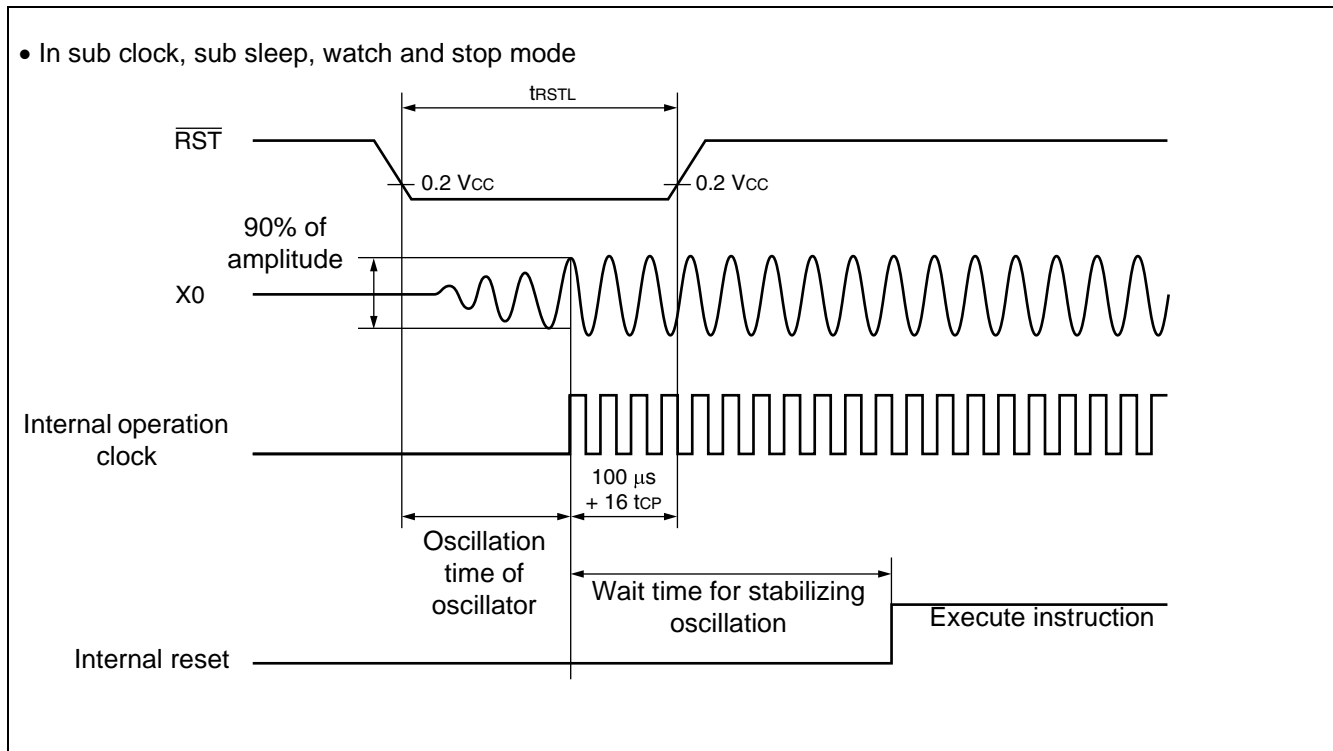
13.4.2 Reset Input Timing

Parameter	Symbol	Pin Name	Value		Unit	Remarks
			Min	Max		
Reset input time	trSTL	RST	16 tCP*3	—	ns	Normal operation
			Oscillation time of oscillator*1 + 100 μs + 16 tCP*3	—	—	In sub clock*2, sub sleep*2, watch*2 and stop mode
			100	—	μs	In timebase timer

*1: Oscillation time of oscillator is time that the amplitude reached the 90%. In the crystal oscillator, the oscillation time is between several ms to tens of ms. In ceramic oscillator, the oscillation time is between hundreds of μs to several ms. In the external clock, the oscillation time is 0 ms.

*2: Except for MB90F387S and MB90387S.

*3: Refer to "(1) Clock timing" ratings for tCP (internal operation clock cycle time).



13.4.4 UART Timing

($V_{CC} = 4.5\text{ V to }5.5\text{ V}$, $V_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK1	Internal shift clock mode output pin is: CL = 80 pF+1TTL.	$4\ t_{CP}^*$	—	ns	
SCK ↓ → SOT delay time	t_{SLOV}	SCK1, SOT1		−80	+80	ns	
Valid SIN → SCK ↑	t_{IVSH}	SCK1, SIN1		100	—	ns	
SCK ↑ → valid SIN hold time	t_{SHIX}	SCK1, SIN1		60	—	ns	
Serial clock “H” pulse width	t_{SHSL}	SCK1	External shift clock mode output pin is: CL = 80 pF+1TTL.	$2\ t_{CP}^*$	—	ns	
Serial clock “L” pulse width	t_{SLSH}	SCK1		$2\ t_{CP}^*$	—	ns	
SCK ↓ → SOT delay time	t_{SLOV}	SCK1, SOT1		—	150	ns	
Valid SIN → SCK ↑	t_{IVSH}	SCK1, SIN1		60	—	ns	
SCK ↑ → valid SIN hold time	t_{SHIX}	SCK1, SIN1		60	—	ns	

*: Refer to Clock Timing ratings for t_{CP} (internal operation clock cycle time).

Notes:

- AC Characteristics in CLK synchronous mode.
- C_L is a load capacitance value on pins for testing.

13.7 Notes on A/D Converter Section

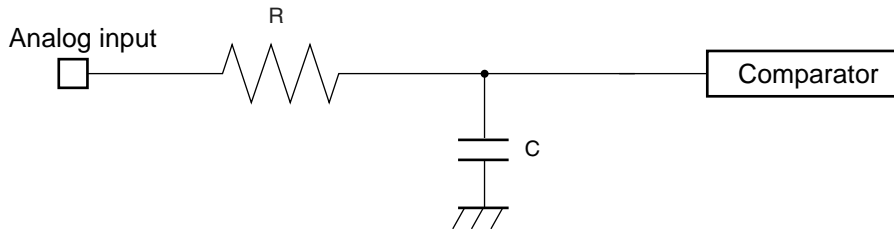
Use the device with external circuits of the following output impedance for analog inputs:

Recommended output impedance of external circuits are: Approx. 3.9 kΩ or lower ($4.5\text{ V} \leq AV_{CC} \leq 5.5\text{ V}$) (sampling period=2.00 μs at 16 MHz machine clock), Approx. 11 kΩ or lower ($4.0\text{ V} \leq AV_{CC} < 4.5\text{ V}$) (sampling period=8.0 μs at 16 MHz machine clock).

If an external capacitor is used, in consideration of the effect by tap capacitance caused by external capacitors and on-chip capacitors, capacitance of the external one is recommended to be several thousand times as high as internal capacitor.

If output impedance of an external circuit is too high, a sampling period for an analog voltage may be insufficient.

- Analog input circuit model



MB90F387/S, MB90387/S

$4.5\text{ V} \leq AV_{CC} \leq 5.5\text{ V}$

$R \cong 2.35\text{ k}\Omega$, $C \cong 36.4\text{ pF}$

$4.0\text{ V} \leq AV_{CC} < 4.5\text{ V}$

$R \cong 16.4\text{ k}\Omega$, $C \cong 36.4\text{ pF}$

Note: Use the values in the figure only as a guideline.

About errors

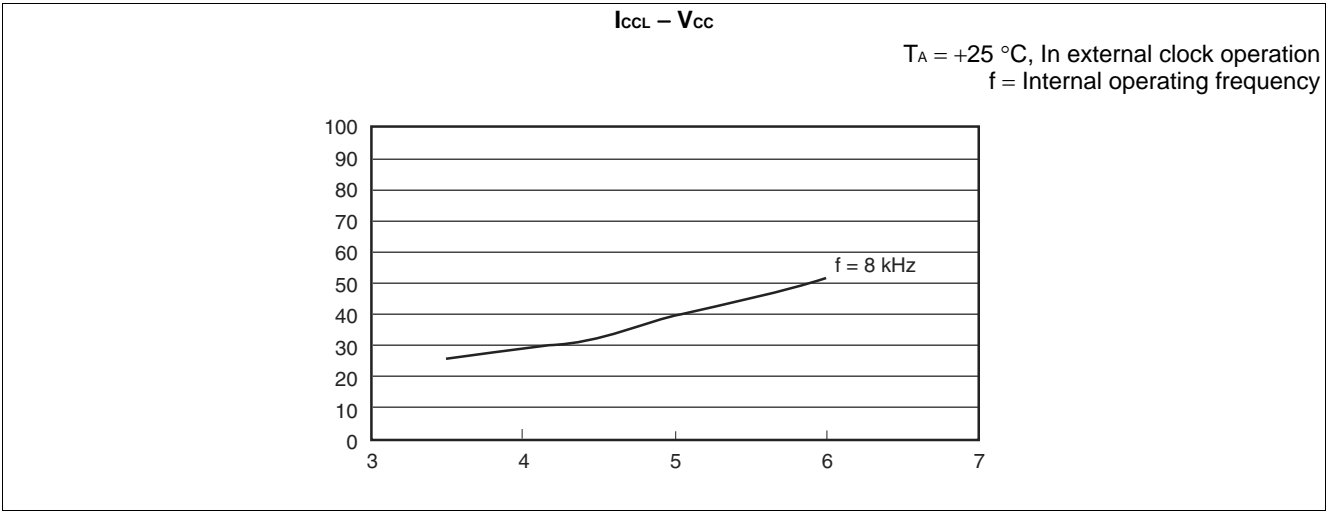
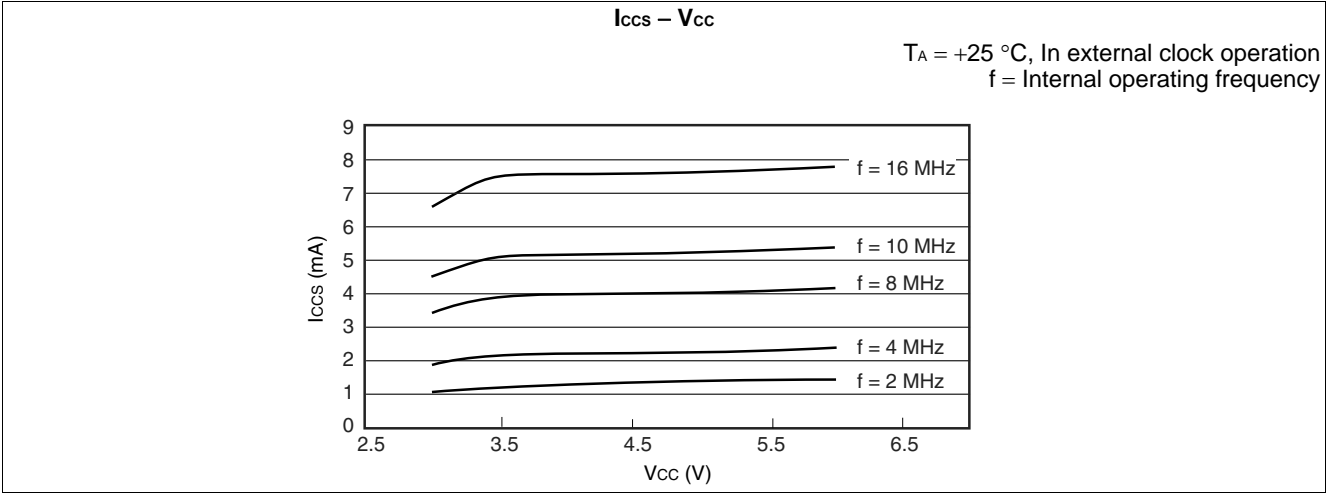
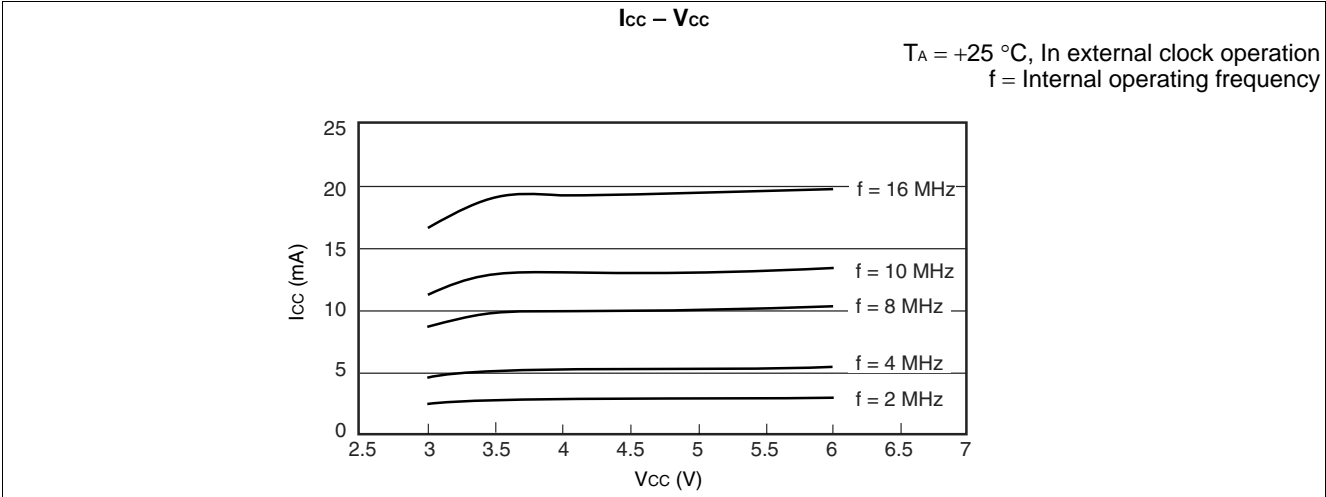
As [AVR-AVss] become smaller, values of relative errors grow larger.

13.8 Flash Memory Program/Erase Characteristics

Parameter	Conditions	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	$T_A = +25\text{ }^\circ\text{C}$ $V_{CC} = 5.0\text{ V}$	—	1	15	s	Excludes 00H programming prior to erasure
Chip erase time		—	4	—	s	Excludes 00H programming prior to erasure
Word (16-bit width) programming time		—	16	3,600	μs	Except for the over head time of the system
Program/Erase cycle	—	10,000	—	—	cycle	
Flash Data Retention Time	Average $T_A = +85\text{ }^\circ\text{C}$	20	—	—	Year	*

*: This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at +85 °C).

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(Continued)