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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, SCI, UART/USART
Peripherals	POR, WDT
Number of I/O	34
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90f387pmt-gte1

Contents

Notes When Using No Sub Clock

■ If an oscillator is not connected to X0A and X1A pin, apply pull-down resistor to X0A pin and leave X1A pin open.

About Power Supply Pins

■ If two or more Vcc and Vss pins exist, the pins that should be at the same potential are connected to each other inside the device. For reducing unwanted emissions and preventing malfunction of strobe signals caused by increase of ground level, however, be sure to connect the Vcc and Vss pins to the power source and the ground externally.

■ Pay attention to connect a power supply to Vcc and Vss of MB90385 series device in a lowest-possible impedance.

■ Near pins of MB90385 series device, connecting a bypass capacitor is recommended at 0.1 μF across Vcc pin and Vss pin.

Crystal Oscillator Circuit

■ Noises around X0 and X1 pins cause malfunctions on a MB90385 series device. Design a print circuit so that X0 and X1 pins, an crystal oscillator (or a ceramic oscillator), and bypass capacitor to the ground become as close as possible to each other. Furthermore, avoid wires to X0 and X1 pins crossing each other as much as possible.

■ Print circuit designing that surrounds X0 and X1 pins with grounding wires, which ensures stable operation, is strongly recommended.

Caution on Operations during PLL Clock Mode

■ If the PLL clock mode is selected, the microcontroller attempt to be working with the self-oscillating circuit even when there is no external oscillator or external clock input is stopped. Performance of this operation, however, cannot be guaranteed.

Sequence of Turning on Power of A/D Converter and Applying Analog Input

■ Be sure to turn on digital power (Vcc) before applying signals to the A/D converter and applying analog input signals (AN0 to AN7 pins).

■ Be sure to turn off the power of A/D converter and analog input before turning off the digital power source.

■ Be sure not to apply AVR exceeding AVcc when turning on and off. (No problems occur if analog and digital power is turned on and off simultaneously.)

Handling Pins When A/D Converter is Not Used

■ If the A/D converter is not used, connect the pins under the following conditions: “AVcc=AVR=Vcc,” and “AVss=Vss”

Note on Turning on Power

■ For preventing malfunctions on built-in step-down circuit, maintain a minimum of 50 μs of voltage rising time (between 0.2 V and 2.7V) when turning on the power.

Stabilization of Supply Voltage

■ A sudden change in the supply voltage may cause the device to malfunction even within the specified V_{CC} supply voltage operating range. Therefore, the V_{CC} supply voltage should be stabilized.
For reference, the supply voltage should be controlled so that V_{CC} ripple variations (peak-to-peak values) at commercial frequencies (50 Hz / 60 Hz) fall below 10% of the standard V_{CC} supply voltage and the coefficient of fluctuation does not exceed 0.1 V/ms at instantaneous power switching.

Address	Register Abbreviation	Register	Read/ Write	Resource	Initial Value
000083H	(Reserved area) *				
000084H	TCANR	Send cancel register	W	CAN controller	00000000B
000085H	(Reserved area) *				
000086H	TCR	Send completion register	R/W	CAN controller	00000000B
000087H	(Reserved area) *				
000088H	RCR	Receive completion register	R/W	CAN controller	00000000B
000089H	(Reserved area) *				
00008AH	RRTRR	Receive RTR register	R/W	CAN controller	00000000B
00008BH	(Reserved area) *				
00008CH	ROVRR	Receive overrun register	R/W	CAN controller	00000000B
00008DH	(Reserved area) *				
00008EH	RIER	Receive completion interrupt permission register	R/W	CAN controller	00000000B
00008FH to 00009DH	(Reserved area) *				
00009EH	PACSR	Address detection control register	R/W	Address matching detection function	00000000B
00009FH	DIRR	Delay interrupt request generation/ release register	R/W	Delay interrupt generation module	XXXXXXX0B
0000A0H	LPMCR	Lower power consumption mode control register	W,R/W	Lower power consumption mode	00011000B
0000A1H	CKSCR	Clock selection register	R,R/W	Clock	11111100B
0000A2H to 0000A7H	(Reserved area) *				
0000A8H	WDTC	Watchdog timer control register	R,W	Watchdog timer	XXXXX111B
0000A9H	TBTC	Time-base timer control register	R/W,W	Time-base timer	1XX00100B
0000AAH	WTC	Watch timer control register	R,R/W	Watch timer	1X001000B
0000ABH to 0000ADH	(Reserved area) *				
0000AEH	FMCS	Flash memory control status register	R,W,R/W	512k-bit Flash memory	000X0000B
0000AFH	(Reserved area) *				

Address	Register Abbreviation	Register	Read/ Write	Resource	Initial Value
003910H	PRLL0	PPG0 reload register L	R/W	8/16-bit PPG timer	XXXXXXXXB
003911H	PRLH0	PPG0 reload register H	R/W		XXXXXXXXB
003912H	PRLL1	PPG1 reload register L	R/W		XXXXXXXXB
003913H	PRLH1	PPG1 reload register H	R/W		XXXXXXXXB
003914H	PRLL2	PPG2 reload register L	R/W		XXXXXXXXB
003915H	PRLH2	PPG2 reload register H	R/W		XXXXXXXXB
003916H	PRLL3	PPG3 reload register L	R/W		XXXXXXXXB
003917H	PRLH3	PPG3 reload register H	R/W		XXXXXXXXB
003918H to 00392FH	(Reserved area) *				
003930H to 003BFFH	(Reserved area) *				
003C00H to 003C0FH	RAM (General-purpose RAM)				
003C10H to 003C13H	IDR0	ID register 0	R/W	CAN controller	XXXXXXXXB to XXXXXXXXB
003C14H to 003C17H	IDR1	ID register 1	R/W		XXXXXXXXB to XXXXXXXXB
003C18H to 003C1BH	IDR2	ID register 2	R/W		XXXXXXXXB to XXXXXXXXB
003C1CH to 003C1FH	IDR3	ID register 3	R/W		XXXXXXXXB to XXXXXXXXB
003C20H to 003C23H	IDR4	ID register 4	R/W		XXXXXXXXB to XXXXXXXXB
003C24H to 003C27H	IDR5	ID register 5	R/W		XXXXXXXXB to XXXXXXXXB
003C28H to 003C2BH	IDR6	ID register 6	R/W		XXXXXXXXB to XXXXXXXXB
003C2CH to 003C2FH	IDR7	ID register 7	R/W		XXXXXXXXB to XXXXXXXXB
003C30H, 003C31H	DLCR0	DLC register 0	R/W		XXXXXXXXB, XXXXXXXXB
003C32H, 003C33H	DLCR1	DLC register 1	R/W		XXXXXXXXB, XXXXXXXXB
003C34H, 003C35H	DLCR2	DLC register 2	R/W		XXXXXXXXB, XXXXXXXXB
003C36H, 003C37H	DLCR3	DLC register 3	R/W		XXXXXXXXB, XXXXXXXXB

Address	Register Abbreviation	Register	Read/ Write	Resource	Initial Value
003C38H, 003C39H	DLCR4	DLC register 4	R/W	CAN controller	XXXXXXXXB, XXXXXXXXB
003C3AH, 003C3BH	DLCR5	DLC register 5	R/W		XXXXXXXXB, XXXXXXXXB
003C3CH, 003C3DH	DLCR6	DLC register 6	R/W		XXXXXXXXB, XXXXXXXXB
003C3EH, 003C3FH	DLCR7	DLC register 7	R/W		XXXXXXXXB, XXXXXXXXB
003C40H to 003C47H	DTR0	Data register 0	R/W		XXXXXXXXB to XXXXXXXXB
003C48H to 003C4FH	DTR1	Data register 1	R/W		XXXXXXXXB to XXXXXXXXB
003C50H to 003C57H	DTR2	Data register 2	R/W		XXXXXXXXB to XXXXXXXXB
003C58H to 003C5FH	DTR3	Data register 3	R/W		XXXXXXXXB to XXXXXXXXB
003C60H to 003C67H	DTR4	Data register 4	R/W		XXXXXXXXB to XXXXXXXXB
003C68H to 003C6FH	DTR5	Data register 5	R/W		XXXXXXXXB to XXXXXXXXB
003C70H to 003C77H	DTR6	Data register 6	R/W		XXXXXXXXB to XXXXXXXXB
003C78H to 003C7FH	DTR7	Data register 7	R/W		XXXXXXXXB to XXXXXXXXB
003C80H to 003CFFH	(Reserved area) *				
003D00H, 003D01H	CSR	Control status register	R/W, R	CAN controller	0XXXX001B, 00XXX000B
003D02H	LEIR	Last event display register	R/W		000XX000B
003D03H	(Reserved area) *				
003D04H, 003D05H	RTEC	Send/receive error counter	R	CAN controller	00000000B, 00000000B
003D06H, 003D07H	BTR	Bit timing register	R/W		11111111B, X1111111B
003D08H	IDER	IDE register	R/W		XXXXXXXXB
003D09H	(Reserved area) *				
003D0AH	TRTRR	Send RTR register	R/W	CAN controller	00000000B
003D0BH	(Reserved area) *				
003D0CH	RFWTR	Remote frame receive wait register	R/W	CAN controller	XXXXXXXXB

11. Interrupt Sources, Interrupt Vectors, And Interrupt Control Registers

Interrupt Source	EI²OS Readiness	Interrupt Vector			Interrupt Control Register		Priority*3
		Number		Address	ICR	Address	
Reset	×	#08	08H	FFFFDCH	–	–	High
INT 9 instruction	×	#09	09H	FFFFD8H	–	–	↑
Exceptional treatment	×	#10	0AH	FFFFD4H	–	–	
CAN controller reception completed (RX)	´	#11	0BH	FFFFD0H	ICR00	0000B0H*1	
CAN controller transmission completed (TX) / Node status transition (NS)	´	#12	0CH	FFFFCCH			
Reserved	×	#13	0DH	FFFFC8H	ICR01	0000B1H	
Reserved	×	#14	0EH	FFFFC4H			
CAN wakeup	Δ	#15	0FH	FFFFC0H	ICR02	0000B2H*1	
Time-base timer	×	#16	10H	FFFFBCH			
16-bit reload timer 0	Δ	#17	11H	FFFFB8H	ICR03	0000B3H*1	
8/10-bit A/D converter	Δ	#18	12H	FFFFB4H			
16-bit free-run timer overflow	Δ	#19	13H	FFFFB0H	ICR04	0000B4H*1	
Reserved	×	#20	14H	FFFFACH			
Reserved	×	#21	15H	FFFFA8H	ICR05	0000B5H*1	
PPG timer ch0, ch1 underflow	´	#22	16H	FFFFA4H			
Input capture 0-input	Δ	#23	17H	FFFFA0H	ICR06	0000B6H*1	
External interrupt (INT4/INT5)	Δ	#24	18H	FFFF9CH			
Input capture 1-input	Δ	#25	19H	FFFF98H	ICR07	0000B7H*2	
PPG timer ch2, ch3 underflow	´	#26	1AH	FFFF94H			
External interrupt (INT6/INT7)	Δ	#27	1BH	FFFF90H	ICR08	0000B8H*1	
Watch timer	Δ	#28	1CH	FFFF8CH			
Reserved	×	#29	1DH	FFFF88H	ICR09	0000B9H*1	
Input capture 2-input Input capture 3-input	´	#30	1EH	FFFF84H			
Reserved	×	#31	1FH	FFFF80H	ICR10	0000BAH*1	
Reserved	×	#32	20H	FFFF7CH			
Reserved	×	#33	21H	FFFF78H	ICR11	0000BBH*1	
Reserved	×	#34	22H	FFFF74H			
Reserved	×	#35	23H	FFFF70H	ICR12	0000BCH*1	↓
16-bit reload timer 1	○	#36	24H	FFFF6CH			Low

Interrupt Source	EI²OS Readiness	Interrupt Vector			Interrupt Control Register		Priority*3
		Number		Address	ICR	Address	
UART1 reception completed	◎	#37	25H	FFFF68H	ICR13	0000BDH*1	High
UART1 transmission completed	Δ	#38	26H	FFFF64H			↑
Reserved	×	#39	27H	FFFF60H	ICR14	0000BEH*1	
Reserved	×	#40	28H	FFFF5CH			
Flash memory	×	#41	29H	FFFF58H	ICR15	0000BFH*1	↓
Delay interrupt generation module	×	#42	2AH	FFFF54H			Low

○ : Available

× : Unavailable

◎ : Available EI²OS function is provided.

Δ: Available when a cause of interrupt sharing a same ICR is not used.

*1:

- ❒ Peripheral functions sharing an ICR register have the same interrupt level.
- ❒ If peripheral functions share an ICR register, only one function is available when using expanded intelligent I/O service.
- ❒ If peripheral functions share an ICR register, a function using expanded intelligent I/O service does not allow interrupt by another function.

*2: Input capture 1 corresponds to EI²OS, however, PPG does not. When using EI²OS by input capture 1, interrupt should be disabled for PPG.

*3:Priority when two or more interrupts of a same level occur simultaneously.

12. Peripheral Resources

12.1 I/O Ports

The I/O ports are used as general-purpose input/output ports (parallel I/O ports). The MB60385 series model is provided with 5 ports (34 inputs). The ports function as input/output pins for peripheral functions also.

I/O Port Functions

An I/O port, using port data resister (PDR), outputs the output data to I/O pin and input a signal input to I/O port. The port direction register (DDR) specifies direction of input/output of I/O pins on a bit-by-bit basis.

The following summarizes functions of the ports and sharing peripheral functions:

■ Port 1: General-purpose input/output port, used also for PPG timer output and input capture inputs.

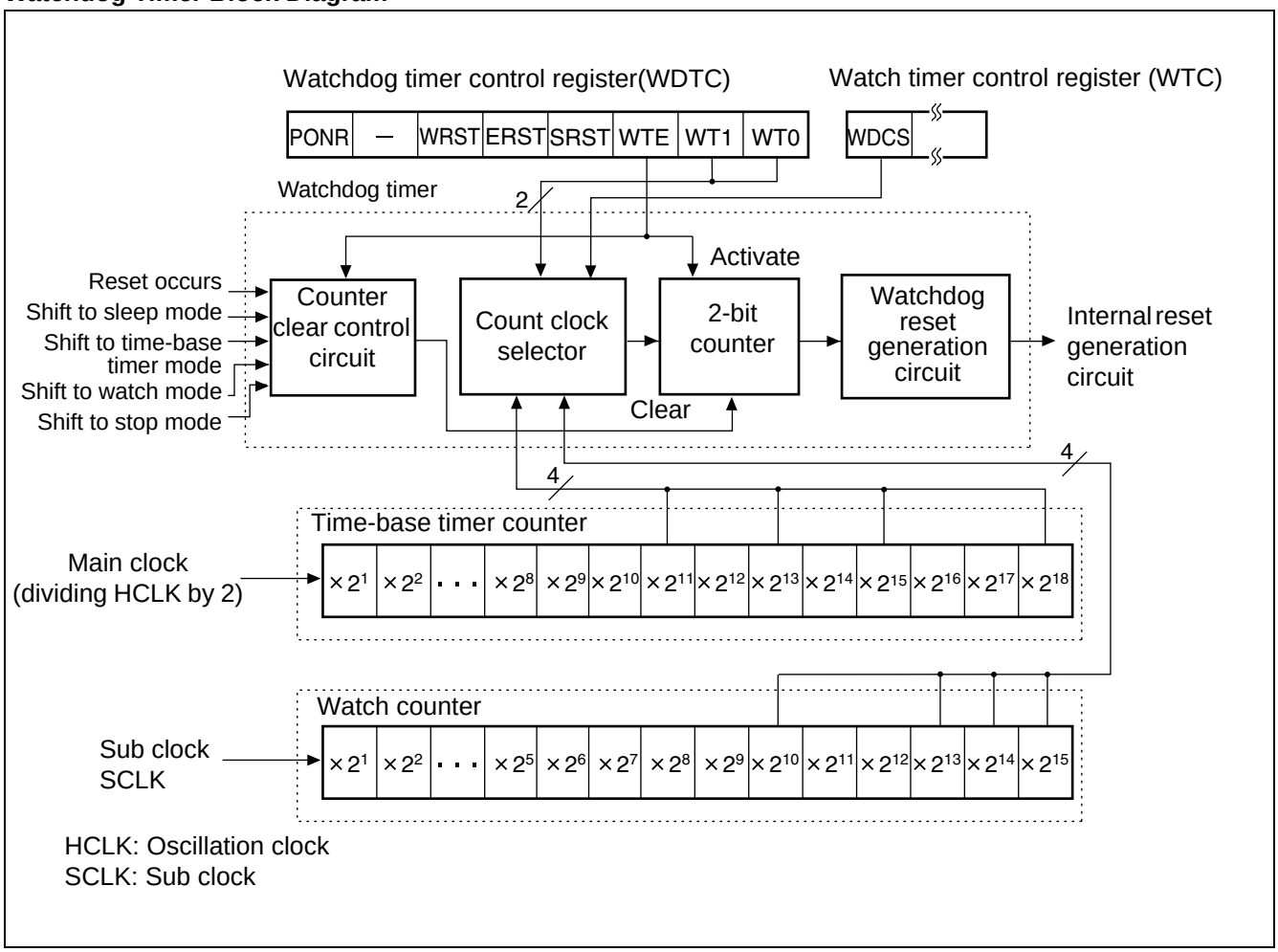
■ Port 2: General-purpose input/output port, used also for reload timer input/output and external interrupt input.

■ Port 3: General-purpose input/output port, used also for A/D converter activation trigger pin.

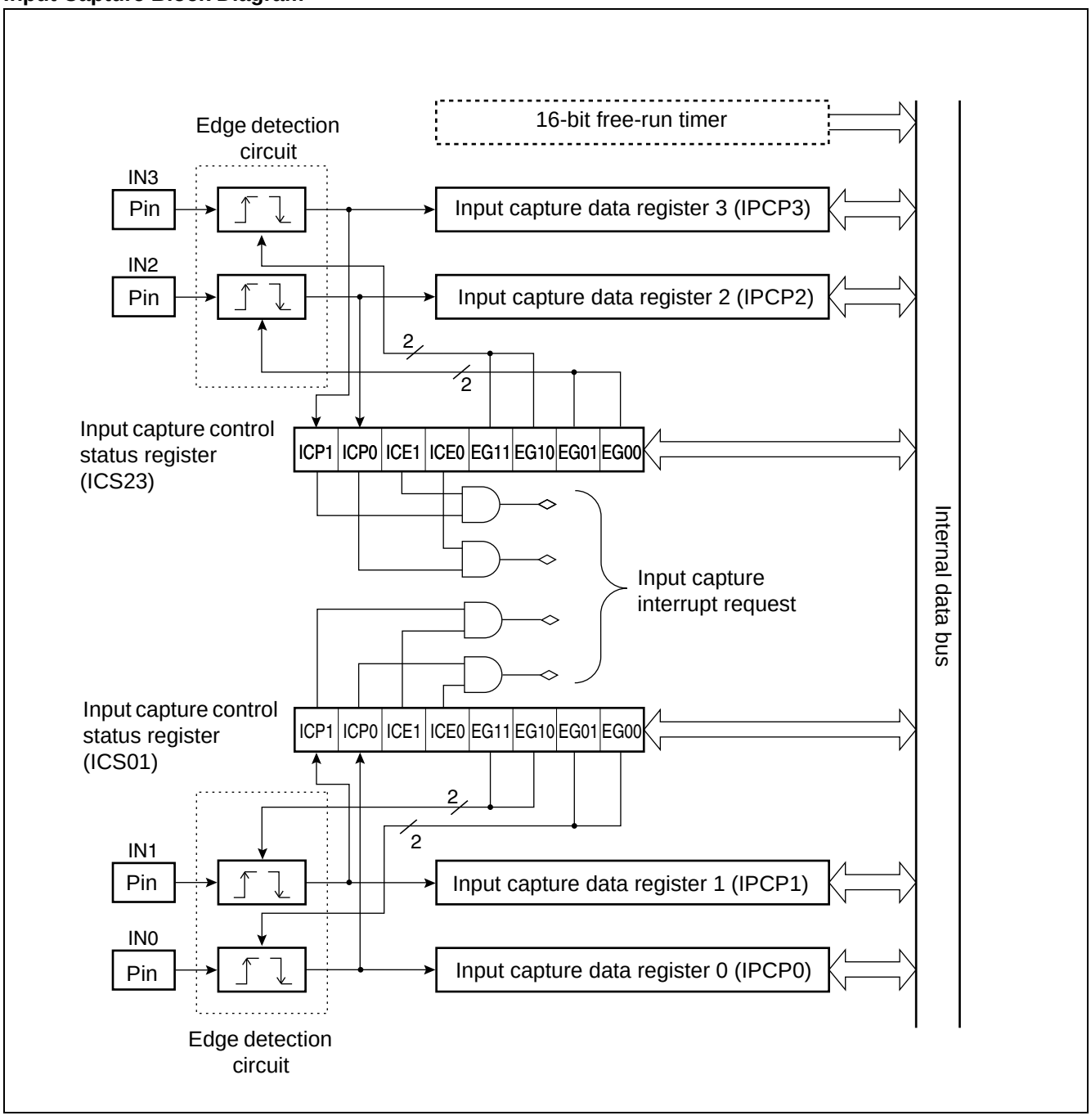
■ Port 4: General-purpose input/output port, used also for UART input/output and CAN controller send/receive pin.

■ Port 5: General-purpose input/output port, used also analog input pin.

Watchdog Timer Block Diagram



Input Capture Block Diagram



12.6 Watch Timer Outline

The watch timer is a 15-bit free-run counter that increments in synchronization with sub clock.

- Interval time is selectable among 7 choices, and generation of interrupt request is allowed for each interval.
- Provides operation clock to the subclock oscillation stabilizing wait timer and watchdog timer.
- Always uses subclock as a count clock regardless of settings of clock selection register (CKSCR).

Interval Timer Function

- In the watch timer, a bit corresponding to the interval time overflows (carry-over) when an interval time, which is specified by interval time selection bit, is reached. Then overflow flag bit is set (WTC: WTOF=1).
- If an interrupt by overflow is permitted (WTC: WTIE=1), an interrupt request is generated upon setting an overflow flag bit.
- Interval time of watch timer is selectable among the following seven choices:

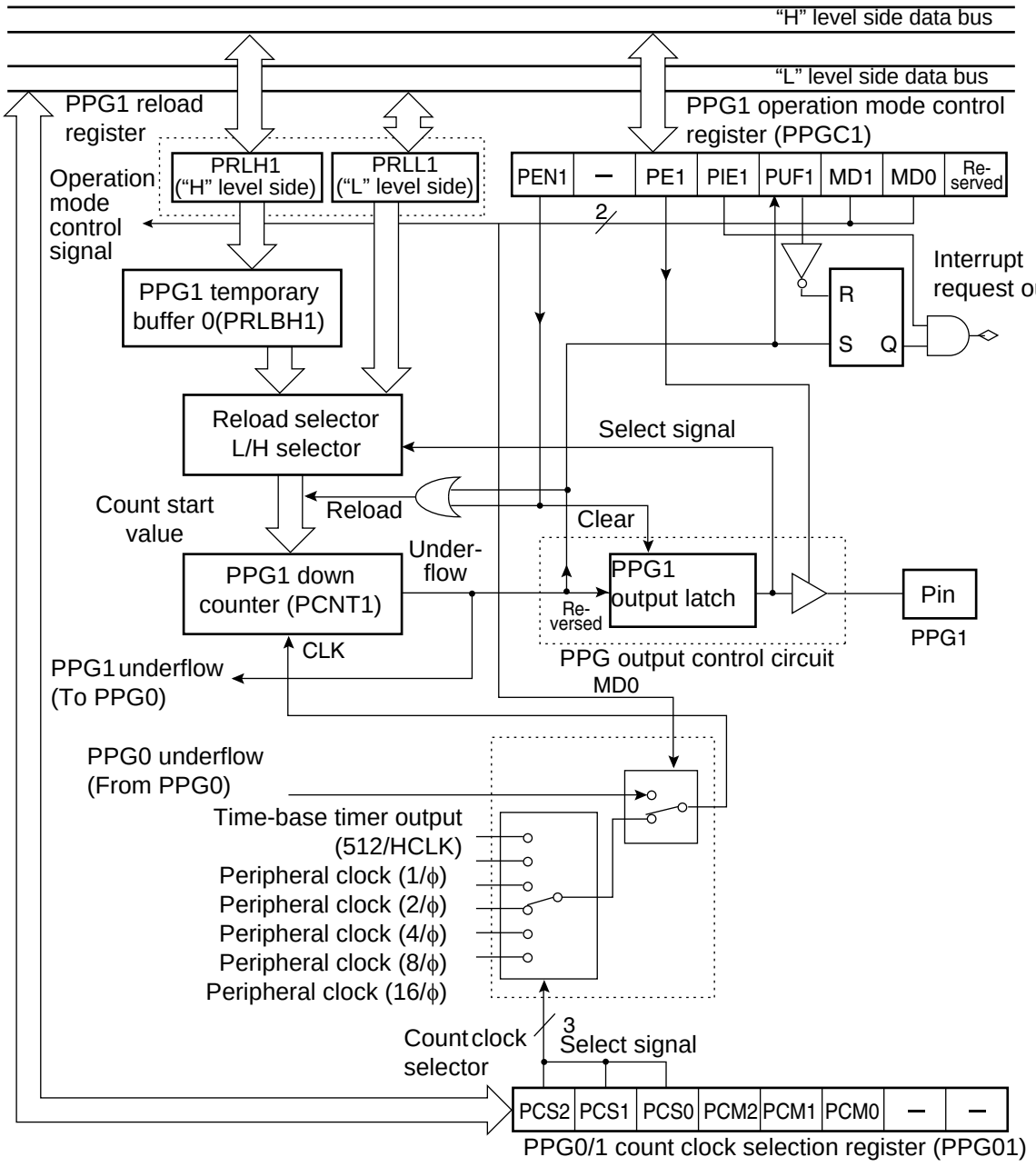
Interval Time of Watch Timer

Sub Clock Cycle	Interval Time
1/SCLK (122 μs)	2^8/SCLK (31.25 ms)
	2^9/SCLK (62.5 ms)
	2^{10}/SCLK (125 ms)
	2^{11}/SCLK (250 ms)
	2^{12}/SCLK (500 ms)
	2^{13}/SCLK (1.0 s)
	2^{14}/SCLK (2.0 s)

SCLK: Sub clock frequency

Values in parentheses “( )” are calculation when operating with 8.192 kHz clock.

8/16-bit PPG Timer 1 Block Diagram



– : Undefined
Reserved: Reserved bit
HCLK : Oscillation clock frequency
ϕ : Machine clock frequency
* : Interrupt output of 8/16-bit PPG timer 1 is incorporated into one by the OR circuit against interrupt output of 8/16-bit PPG timer 0.

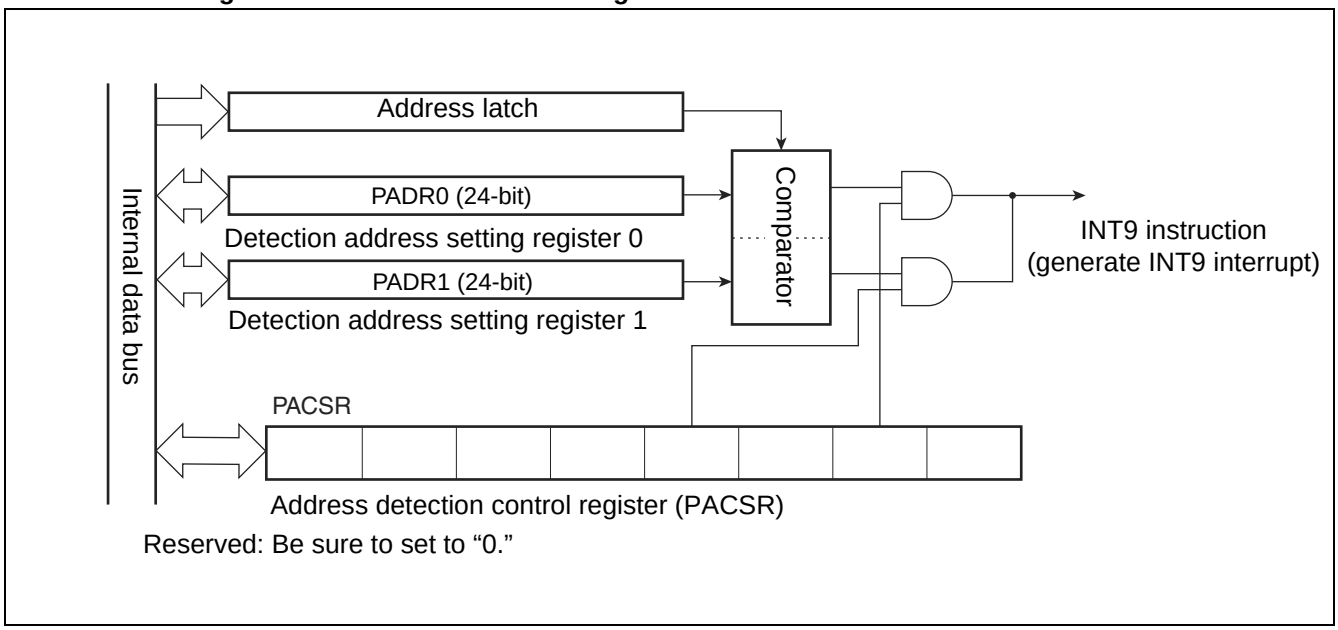
12.13 Address Matching Detection Function Outline

The address matching detection function checks if an address of an instruction to be processed next to a currently-processed instruction is identical with an address specified in the detection address register. If the addresses match with each other, an instruction to be processed next in program is forcibly replaced with INT9 instruction, and process branches to the interrupt process program. Using INT9 interrupt, this function is available for correcting program by batch processing.

Address Matching Detection Function Outline

- An address of an instruction to be processed next to a currently-processed instruction of the program is always retained in an address latch via internal data bus. By the address matching detection function, the address value retained in the address latch is always compared with an address specified in detection address setting register. If the compared address values match with each other, an instruction to be processed next by CPU is forcibly replaced with INT9 instruction, and an interrupt process program is executed.
- Two detection address setting registers are provided (PADR0 and PADR1), and each register is provided with interrupt permission bit. Generation of interrupt, which is caused by address matching between the address retained in address latch and the address specified in address setting register, is permitted and prohibited on a register-by-register basis.

Address Matching Detection Function Block Diagram



- Address latch

  Retains address value output to internal data bus.

- Address detection control register (PACSR)

  Specifies if interrupt is permitted or prohibited when addresses match with each other.

- Detection address setting (PADR0, PADR1)

  Specifies addresses to be compared with values in address latch.

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

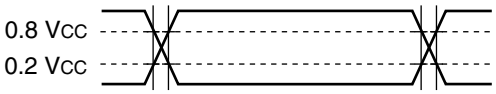
Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current*	I_{CCL}	V_{CC}	V_{CC} = 5.0 V, Internally operating at 8 kHz, subclock operation, T_A = + 25°C	—	0.3	1.2	mA	MB90F387/S
				—	40	100	µA	MB90387/S
	I_{CCLS}		V_{CC} = 5.0 V, Internally operating at 8 kHz, subclock, sleep mode, T_A = + 25°C	—	10	30	µA	
	I_{CCT}		V_{CC} = 5.0 V, Internally operating at 8 kHz, watch mode, T_A = + 25°C	—	8	25	µA	
	I_{CCH}		Stopping, T_A = + 25°C	—	5	20	µA	
Input capacity	C_{IN}	Other than AV_{CC}, AV_{SS}, AVR, C, V_{CC}, V_{SS}	–	—	5	15	pF	
Pull-up resistor	R_{UP}	RST	–	25	50	100	kΩ	
Pull-down resistor	R_{DOWN}	MD2	–	25	50	100	kΩ	Flash product is not provided with pull-down resistor.

*: Test conditions of power supply current are based on a device using external clock.

Rating values of alternating current is defined by the measurement reference voltage values shown below:

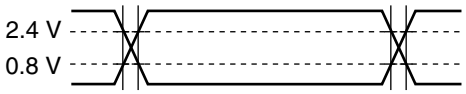
- Input signal waveform

Hysteresis input pin



- Output signal waveform

Output pin



13.4.2 Reset Input Timing

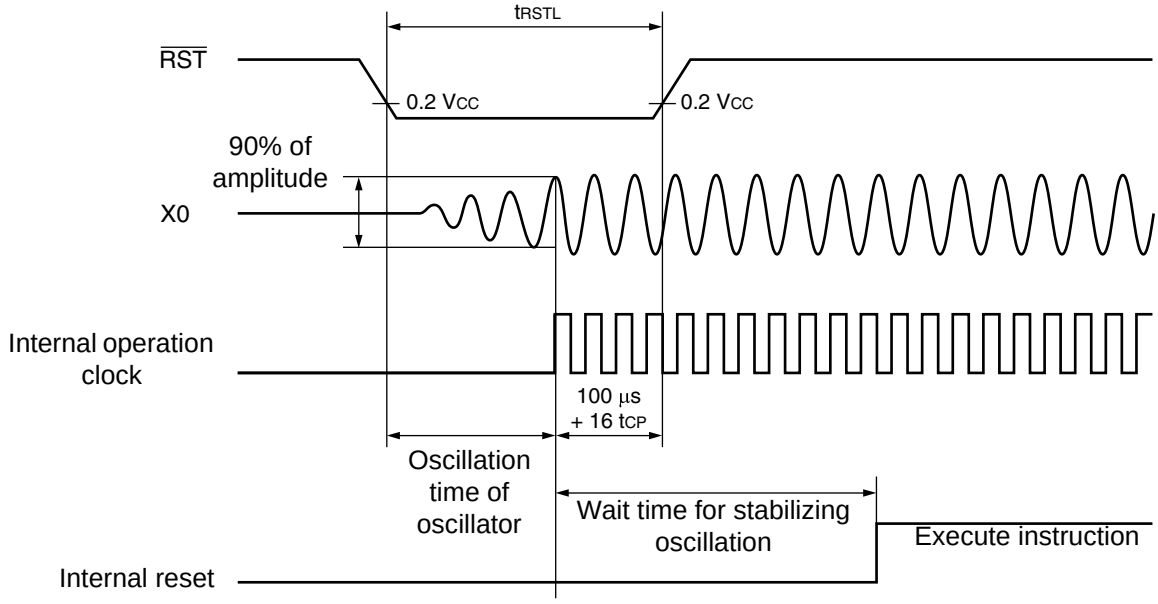
Parameter	Symbol	Pin Name	Value		Unit	Remarks
			Min	Max		
Reset input time	t_{RSTL}	RST	16 t_{CP}*3	–	ns	Normal operation
			Oscillation time of oscillator*1 + 100 μs + 16 t_{CP}*3	–	–	In sub clock*2, sub sleep*2, watch*2 and stop mode
			100	–	μs	In timebase timer

*1: Oscillation time of oscillator is time that the amplitude reached the 90%. In the crystal oscillator, the oscillation time is between several ms to tens of ms. In ceramic oscillator, the oscillation time is between hundreds of μs to several ms. In the external clock, the oscillation time is 0 ms.

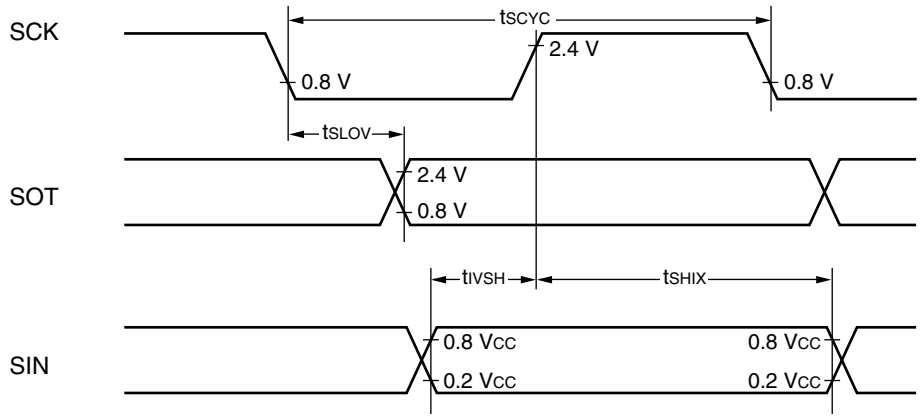
*2: Except for MB90F387S and MB90387S.

*3: Refer to "(1) Clock timing" ratings for t_{CP} (internal operation clock cycle time).

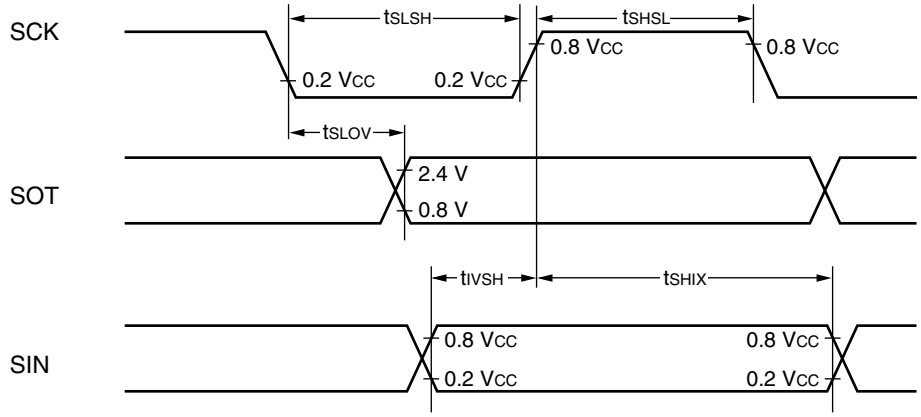
- In sub clock, sub sleep, watch and stop mode



• Internal shift clock mode



• External shift clock mode



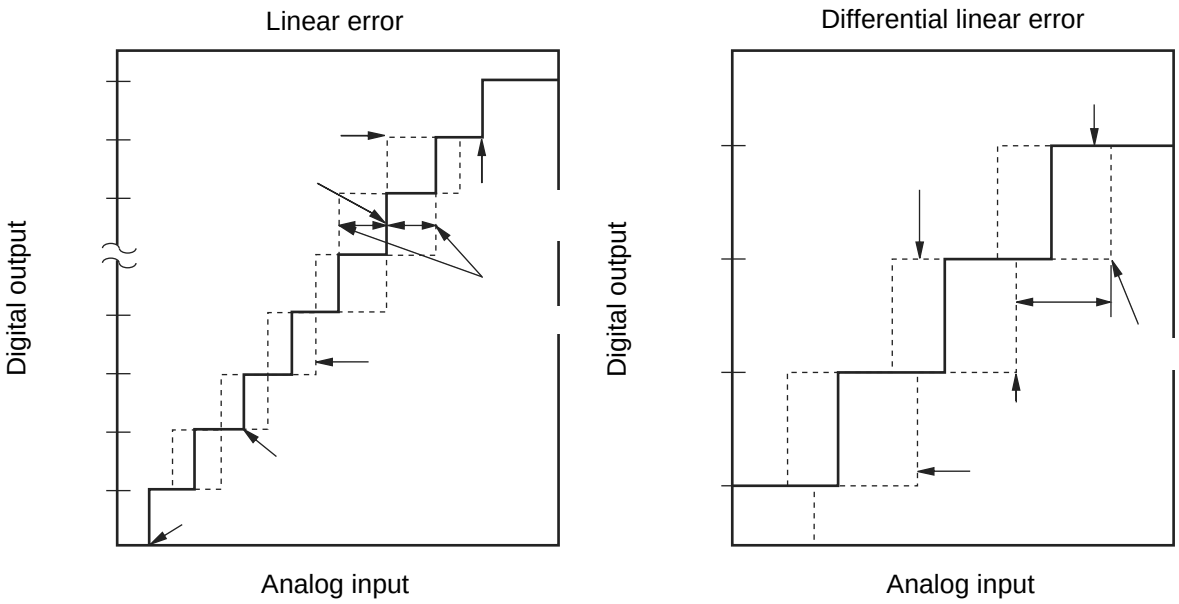
13.4.5 Timer Input Timing

(V_{CC} = 4.5 V to 5.5 V, V_{SS} = 0.0 V, T_A = −40 °C to +105 °C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH}	TIN0, TIN1	–	4 t_{CP} *	–	ns	
	t_{TIWL}	IN0 to IN3					

*: Refer to Clock Timing ratings for t_{CP} (internal operation clock cycle time).

(Continued)



$$\text{Linear error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + V_{OT}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

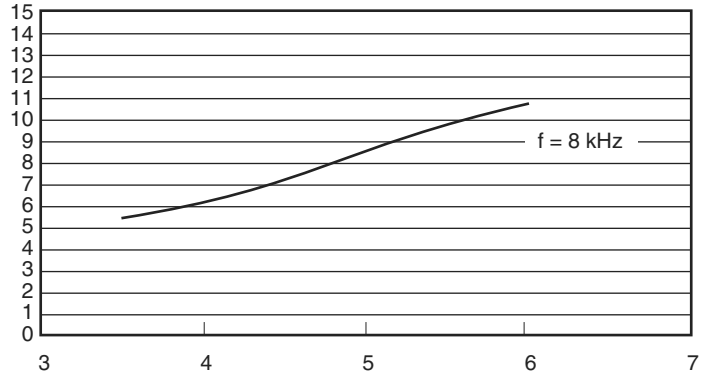
$$\text{Differential linear error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\text{LSB}\ [\text{LSB}]$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ [\text{V}]$$

V_{OT}: Voltage at which digital output transits from “000_H” to “001_H.”
V_{FST}: Voltage at which digital output transits from “$3FE_H$” to “$3FF_H$.”

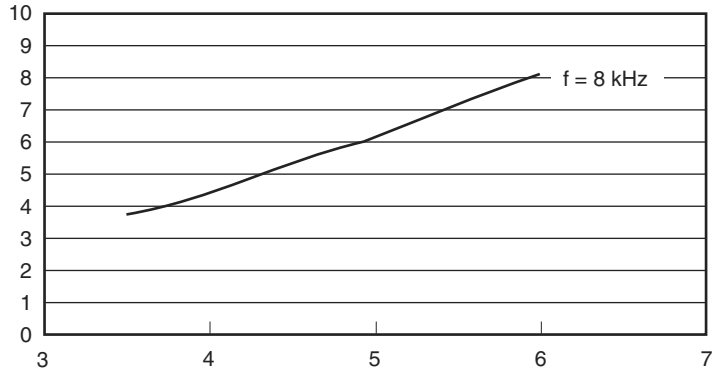
I_{CCLS} – V_{CC}

T_A = +25 °C, In external clock operation
f = Internal operating frequency



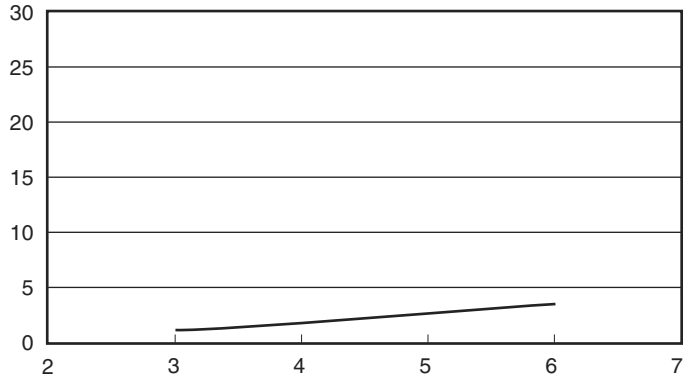
I_{CCT} – V_{CC}

T_A = +25 °C, In external clock operation
f = Internal operating frequency



I_{CCH} – V_{CC}

Stopping, T_A = +25 °C

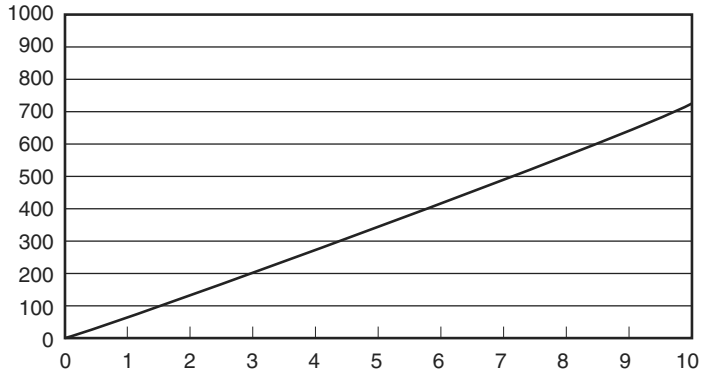


(Continued)

(Continued)

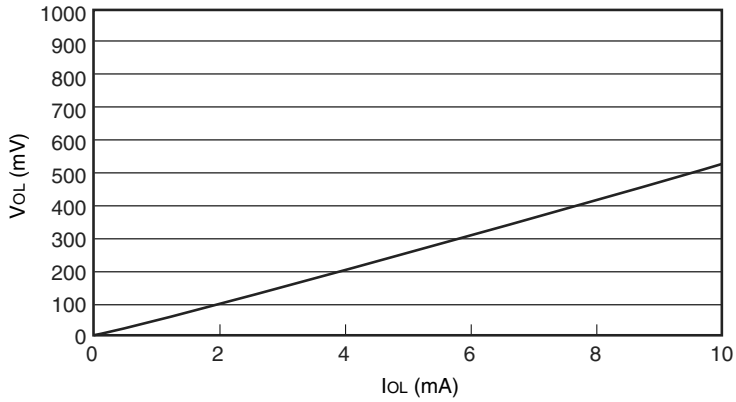
(V_{CC} - V_{OH}) – I_{OH}

T_A = +25 °C, V_{CC} = 4.5 V



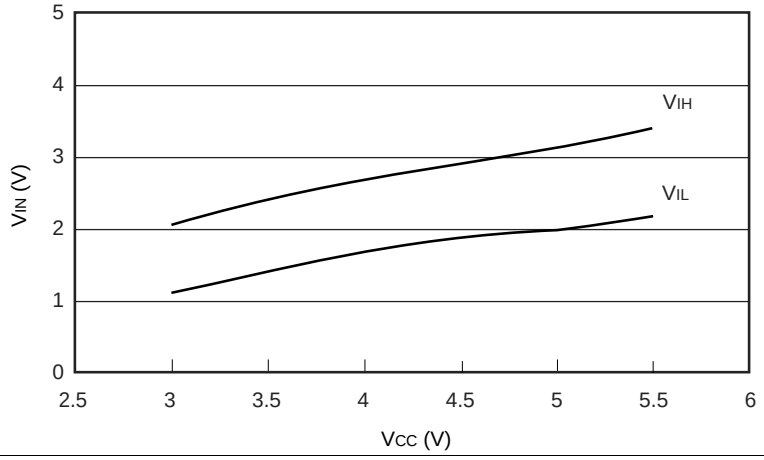
V_{OL} – I_{OL}

T_A = +25 °C, V_{CC} = 4.5 V



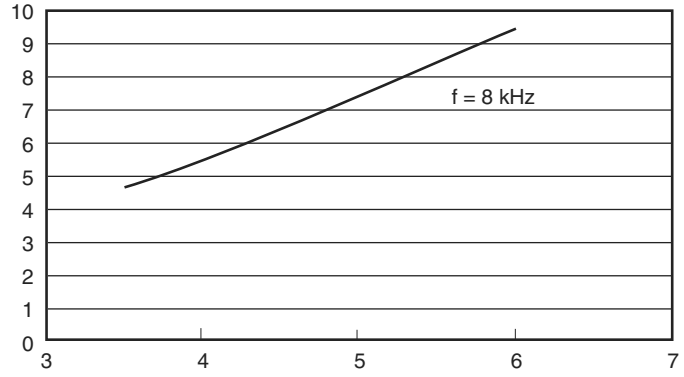
H level input voltage/ L level input voltage
V_{IN} – V_{CC}

T_A = +25 °C



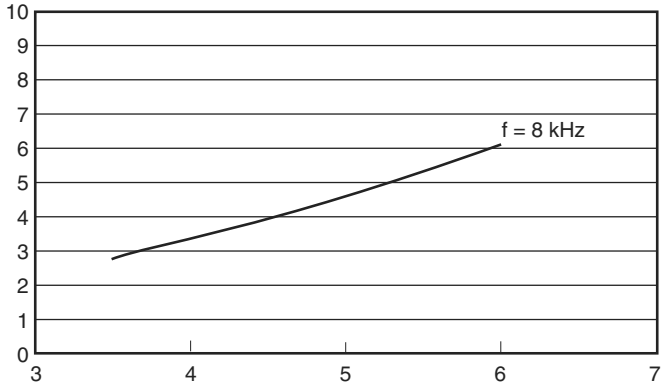
I_{CCLS} – V_{CC}

T_A = +25 °C, In external clock operation
f = Internal operating frequency



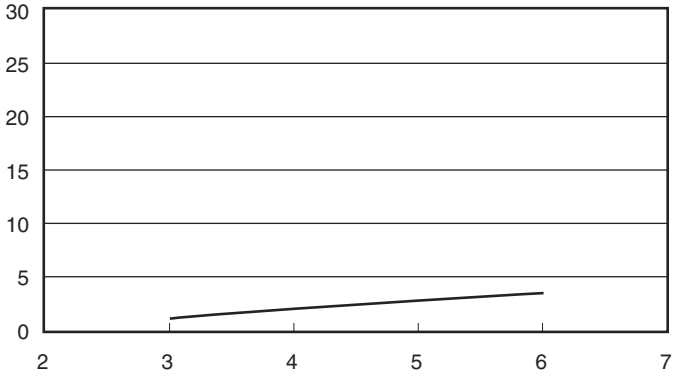
I_{CCT} – V_{CC}

T_A = +25 °C, In external clock operation
f = Internal operating frequency



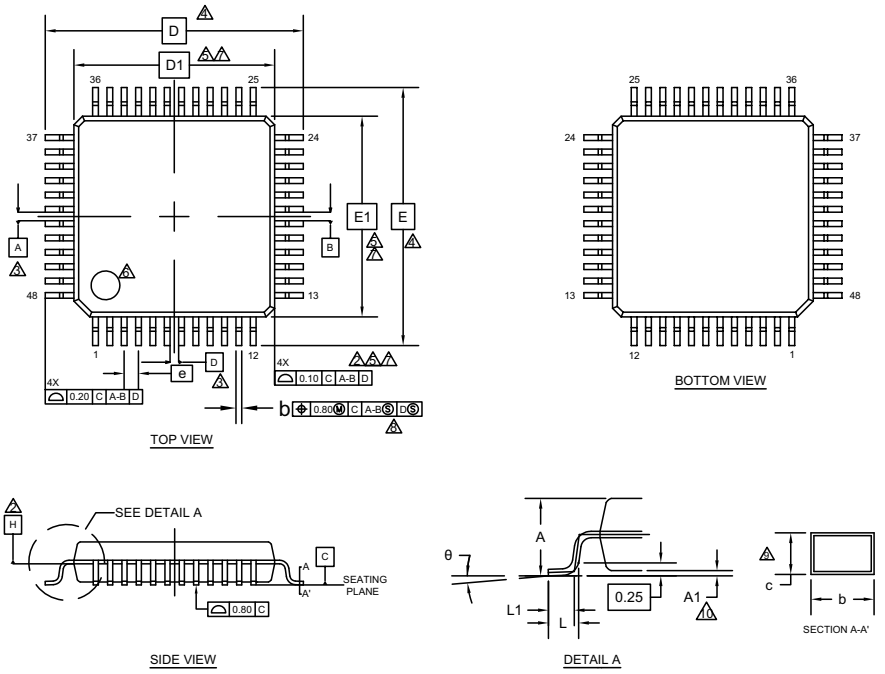
I_{CCH} – V_{CC}

Stopping, T_A = +25 °C



(Continued)

16. Package Dimension



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.00	—	0.20
b	0.15	—	0.27
c	0.09	—	0.20
D	9.00 BSC		
D1	7.00 BSC		
e	0.50 BSC		
E	9.00 BSC		
E1	7.00 BSC		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
θ	0°	—	8°

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-13731 **

PACKAGE OUTLINE, 48 LEAD LQFP
7.0X7.0X1.7 MM LQA048 REV**