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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

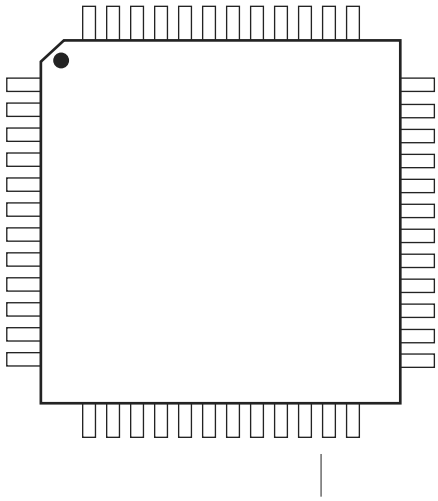
Details	
Product Status	Active
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, SCI, UART/USART
Peripherals	POR, WDT
Number of I/O	36
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90f387spmc-gs

1. Product Lineup

Parameter \ Part Number		MB90F387 MB90F387S	MB90387 MB90387S	MB90V495G
Classification		Flash ROM	Mask ROM	Evaluation product
ROM capacity		64 Kbytes		–
RAM capacity		2 Kbytes		6 Kbytes
Process		CMOS		
Package		LQFP-48 (pin pitch 0.50 mm)		PGA-256
Operating power supply voltage		3.5 V to 5.5 V		4.5 V to 5.5 V
Special power supply for emulator*1		–		None
CPU functions		Number of basic instructions : 351 instructions Instruction bit length : 8 bits and 16 bits Instruction length : 1 byte to 7 bytes Data bit length : 1 bit, 8 bits, 16 bits		
		Minimum instruction execution time: 62.5 ns (at 16 MHz machine clock)		
		Interrupt processing time: 1.5 μs at minimum (at 16 MHz machine clock)		
Low power consumption (standby) mode		Sleep mode / Watch mode / Time-base timer mode / Stop mode / CPU intermittent		
I/O port		General-purpose input/output ports (CMOS output): 34 ports (36 ports*2) including 4 high-current output ports (P14 to P17)		
Time-base timer		18-bit free-run counter Interrupt cycle: 1.024 ms, 4.096 ms, 16.834 ms, 131.072 ms (with oscillation clock frequency at 4 MHz)		
Watchdog timer		Reset generation cycle: 3.58 ms, 14.33 ms, 57.23 ms, 458.75 ms (with oscillation clock frequency at 4 MHz)		
16-bit input/ output timer	16-bit free-run timer	Number of channels: 1 Interrupt upon occurrence of overflow		
	Input capture	Number of channels: 4 Retaining free-run timer value set by pin input (rising edge, falling edge, and both edges)		
16-bit reload timer		Number of channels: 2 16-bit reload timer operation Count clock cycle: 0.25 μs, 0.5 μs, 2.0 μs (at 16-MHz machine clock frequency) External event count is allowed.		
Watch timer		15-bit free-run counter Interrupt cycle: 31.25 ms, 62.5 ms, 12 ms, 250 ms, 500 ms, 1.0 s, 2.0 s (with 8.192 kHz sub clock)		
8/16-bit PPG timer		Number of channels: 2 (four 8-bit channels are available also.) PPG operation is allowed with four 8-bit channels or two 16-bit channels. Outputting pulse wave of arbitrary cycle or arbitrary duty is allowed. Count clock: 62.5 ns to 1 μs (with 16 MHz machine clock)		
Delay interrupt generator module		Interrupt generator module for task switching. Used for realtime OS.		
DTP/External interrupt		Number of inputs: 4 Activated by rising edge, falling edge, “H” level or “L” level input. External interrupt or expanded intelligent I/O service (EI^{2}OS) is available.		

4. Pin Assignment

(Top View)



(LQA048)

*: MB90387, MB90F387 : X1A, X0A
MB90387S, MB90F387S: P36, P35

5. Pin Description

Pin No.	Pin Name	Circuit Type	Function
1	AVcc	–	Vcc power input pin for A/D converter.
2	AVR	–	Power (Vref+) input pin for A/D converter. Use as input for Vcc or lower.
3 to 10	P50 to P57	E	General-purpose input/output ports.
	AN0 to AN7		Functions as analog input pins for A/D converter. Valid when analog input setting is “enabled.”
11	P37	D	General-purpose input/output port.
	ADTG		Function as an external trigger input pin for A/D converter. Use the pin by setting as input port.
12	P20	D	General-purpose input/output port.
	TIN0		Function as an event input pin for reload timer 0. Use the pin by setting as input port.
13	P21	D	General-purpose input/output port.
	TOT0		Function as an event output pin for reload timer 0. Valid only when output setting is “enabled.”
14	P22	D	General-purpose input/output port.
	TIN1		Function as an event input pin for reload timer 1. Use the pin by setting as input port.
15	P23	D	General-purpose input/output port.
	TOT1		Function as an event output pin for reload timer 1. Valid only when output setting is “enabled.”
16 to 19	P24 to P27	D	General-purpose input/output ports.
	INT4 to INT7		Functions as external interrupt input pins. Use the pins by setting as input port.
20	MD2	F	Input pin for specifying operation mode. Connect directly to Vss.
21	MD1	C	Input pin for specifying operation mode. Connect directly to Vcc.
22	MD0	C	Input pin for specifying operation mode. Connect directly to Vcc.
23	RST	B	External reset input pin.
24	Vcc	–	Power source (5 V) input pin.
25	Vss	–	Power source (0 V) input pin.
26	C	–	Capacitor pin for stabilizing power source. Connect a ceramic capacitor of approximately 0.1 μF.
27	X0	A	Pin for high-rate oscillation.
28	X1	A	Pin for high-rate oscillation.
29 to 32	P10 to P13	D	General-purpose input/output ports.
	IN0 to IN3		Functions as trigger input pins of input capture ch.0 to ch.3. Use the pins by setting as input ports.
33 to 36	P14 to P17	G	General-purpose input/output ports. High-current output ports.
	PPG0 to PPG3		Functions as output pins of PPG timers 01 and 23. Valid when output setting is “enabled.”
37	P40	D	General-purpose input/output port.
	SIN1		Serial data input pin for UART. Use the pin by setting as input port.
38	P41	D	General-purpose input/output port.
	SCK1		Serial clock input pin for UART. Valid only when serial clock input/output setting on UART is “enabled.”

10. I/O Map

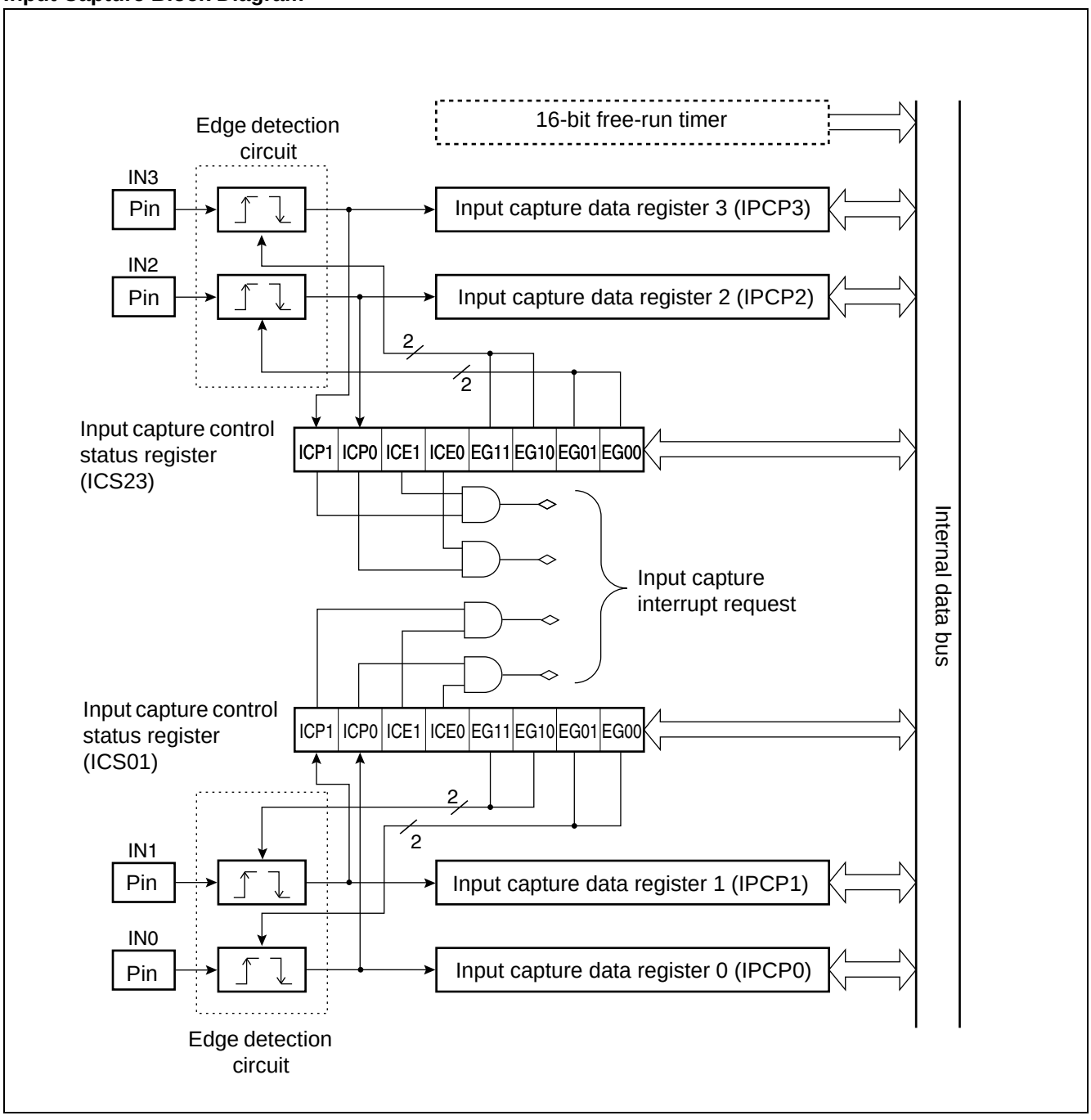
Address	Register Abbreviation	Register	Read/ Write	Resource	Initial Value
000000H	(Reserved area) *				
000001H	PDR1	Port 1 data register	R/W	Port 1	XXXXXXXXB
000002H	PDR2	Port 2 data register	R/W	Port 2	XXXXXXXXB
000003H	PDR3	Port 3 data register	R/W	Port 3	XXXXXXXXB
000004H	PDR4	Port 4 data register	R/W	Port 4	XXXXXXXXB
000005H	PDR5	Port 5 data register	R/W	Port 5	XXXXXXXXB
000006H to 000010H	(Reserved area) *				
000011H	DDR1	Port 1 direction data register	R/W	Port 1	00000000B
000012H	DDR2	Port 2 direction data register	R/W	Port 2	00000000B
000013H	DDR3	Port 3 direction data register	R/W	Port 3	000X0000B
000014H	DDR4	Port 4 direction data register	R/W	Port 4	XXX00000B
000015H	DDR5	Port 5 direction data register	R/W	Port 5	00000000B
000016H to 00001AH	(Reserved area) *				
00001BH	ADER	Analog input permission register	R/W	8/10-bit A/D converter	11111111B
00001CH to 000025H	(Reserved area) *				
000026H	SMR1	Serial mode register 1	R/W	UART1	00000000B
000027H	SCR1	Serial control register 1	R/W, W		00000100B
000028H	SIDR1/ SODR1	Serial input data register 1/ Serial output data register 1	R, W		XXXXXXXXB
000029H	SSR1	Serial status data register 1	R, R/W		00001000B
00002AH	(Reserved area) *				
00002BH	CDCR1	Communication prescaler control register 1	R/W	UART1	0XXX0000B
00002CH to 00002FH	(Reserved area) *				
000030H	ENIR	DTP/External interrupt permission register	R/W	DTP/External interrupt	00000000B
000031H	EIRR	DTP/External interrupt permission register	R/W		XXXXXXXXB
000032H	ELVR	Detection level setting register	R/W		00000000B
000033H			R/W		00000000B
000034H	ADCS	A/D control status register	R/W	8/10-bit A/D converter	00000000B
000035H			R/W, W		00000000B
000036H	ADCR	A/D data register	W, R		XXXXXXXXB
000037H			R		00101XXXB

Address	Register Abbreviation	Register	Read/ Write	Resource	Initial Value
003C38H, 003C39H	DLCR4	DLC register 4	R/W	CAN controller	XXXXXXXXB, XXXXXXXXB
003C3AH, 003C3BH	DLCR5	DLC register 5	R/W		XXXXXXXXB, XXXXXXXXB
003C3CH, 003C3DH	DLCR6	DLC register 6	R/W		XXXXXXXXB, XXXXXXXXB
003C3EH, 003C3FH	DLCR7	DLC register 7	R/W		XXXXXXXXB, XXXXXXXXB
003C40H to 003C47H	DTR0	Data register 0	R/W		XXXXXXXXB to XXXXXXXXB
003C48H to 003C4FH	DTR1	Data register 1	R/W		XXXXXXXXB to XXXXXXXXB
003C50H to 003C57H	DTR2	Data register 2	R/W		XXXXXXXXB to XXXXXXXXB
003C58H to 003C5FH	DTR3	Data register 3	R/W		XXXXXXXXB to XXXXXXXXB
003C60H to 003C67H	DTR4	Data register 4	R/W		XXXXXXXXB to XXXXXXXXB
003C68H to 003C6FH	DTR5	Data register 5	R/W		XXXXXXXXB to XXXXXXXXB
003C70H to 003C77H	DTR6	Data register 6	R/W		XXXXXXXXB to XXXXXXXXB
003C78H to 003C7FH	DTR7	Data register 7	R/W		XXXXXXXXB to XXXXXXXXB
003C80H to 003CFFH	(Reserved area) *				
003D00H, 003D01H	CSR	Control status register	R/W, R	CAN controller	0XXXX001B, 00XXX000B
003D02H	LEIR	Last event display register	R/W		000XX000B
003D03H	(Reserved area) *				
003D04H, 003D05H	RTEC	Send/receive error counter	R	CAN controller	00000000B, 00000000B
003D06H, 003D07H	BTR	Bit timing register	R/W		11111111B, X1111111B
003D08H	IDER	IDE register	R/W		XXXXXXXXB
003D09H	(Reserved area) *				
003D0AH	TRTRR	Send RTR register	R/W	CAN controller	00000000B
003D0BH	(Reserved area) *				
003D0CH	RFWTR	Remote frame receive wait register	R/W	CAN controller	XXXXXXXXB

11. Interrupt Sources, Interrupt Vectors, And Interrupt Control Registers

Interrupt Source	EI²OS Readiness	Interrupt Vector			Interrupt Control Register		Priority*3
		Number		Address	ICR	Address	
Reset	×	#08	08H	FFFFDCH	–	–	High
INT 9 instruction	×	#09	09H	FFFFD8H	–	–	↑
Exceptional treatment	×	#10	0AH	FFFFD4H	–	–	
CAN controller reception completed (RX)	´	#11	0BH	FFFFD0H	ICR00	0000B0H*1	
CAN controller transmission completed (TX) / Node status transition (NS)	´	#12	0CH	FFFFCCH			
Reserved	×	#13	0DH	FFFFC8H	ICR01	0000B1H	
Reserved	×	#14	0EH	FFFFC4H			
CAN wakeup	Δ	#15	0FH	FFFFC0H	ICR02	0000B2H*1	
Time-base timer	×	#16	10H	FFFFBCH			
16-bit reload timer 0	Δ	#17	11H	FFFFB8H	ICR03	0000B3H*1	
8/10-bit A/D converter	Δ	#18	12H	FFFFB4H			
16-bit free-run timer overflow	Δ	#19	13H	FFFFB0H	ICR04	0000B4H*1	
Reserved	×	#20	14H	FFFFACH			
Reserved	×	#21	15H	FFFFA8H	ICR05	0000B5H*1	
PPG timer ch0, ch1 underflow	´	#22	16H	FFFFA4H			
Input capture 0-input	Δ	#23	17H	FFFFA0H	ICR06	0000B6H*1	
External interrupt (INT4/INT5)	Δ	#24	18H	FFFF9CH			
Input capture 1-input	Δ	#25	19H	FFFF98H	ICR07	0000B7H*2	
PPG timer ch2, ch3 underflow	´	#26	1AH	FFFF94H			
External interrupt (INT6/INT7)	Δ	#27	1BH	FFFF90H	ICR08	0000B8H*1	
Watch timer	Δ	#28	1CH	FFFF8CH			
Reserved	×	#29	1DH	FFFF88H	ICR09	0000B9H*1	
Input capture 2-input Input capture 3-input	´	#30	1EH	FFFF84H			
Reserved	×	#31	1FH	FFFF80H	ICR10	0000BAH*1	
Reserved	×	#32	20H	FFFF7CH			
Reserved	×	#33	21H	FFFF78H	ICR11	0000BBH*1	
Reserved	×	#34	22H	FFFF74H			
Reserved	×	#35	23H	FFFF70H	ICR12	0000BCH*1	↓
16-bit reload timer 1	○	#36	24H	FFFF6CH			Low

Input Capture Block Diagram



12.5 16-bit Reload Timer

The 16-bit reload timer has the following functions:

- Count clock is selectable among 3 internal clocks and external event clock.
- Activation trigger is selectable between software trigger and external trigger.
- Generation of CPU interrupt is allowed upon occurrence of underflow on 16-bit timer register. Available as an interval timer using the interrupt function.
- When underflow of 16-bit timer register (TMR) occurs, one of two reload modes is selectable between one-shot mode that halts counting operation of TMR, and reload mode that reloads 16-bit reload register value to TMR, continuing TMR counting operation.
- The 16-bit reload timer is ready for expanded intelligent I/O service (EI^2OS).
- MB90385 series device has 2 channels of built-in 16-bit reload timer.

Operation Mode of 16-bit Reload Timer

Count Clock	Activation Trigger	Operation upon Underflow
Internal clock mode	Software trigger, external trigger	One-shot mode, reload mode
Event count mode	Software trigger	One-shot mode, reload mode

Internal Clock Mode

- The 16-bit reload timer is set to internal clock mode, by setting count clock selection bit (TMCSR: CSL1, CSL0) to “00_B”, “01_B”, “10_B”.
- In the internal clock mode, the counter decrements in synchronization with the internal clock.
- Three types of count clock cycles are selectable by count clock selection bit (TMCSR: CSL1, CSL0) in timer control status register.
- Edge detection of software trigger or external trigger is specified as an activation trigger.

12.6 Watch Timer Outline

The watch timer is a 15-bit free-run counter that increments in synchronization with sub clock.

- Interval time is selectable among 7 choices, and generation of interrupt request is allowed for each interval.
- Provides operation clock to the subclock oscillation stabilizing wait timer and watchdog timer.
- Always uses subclock as a count clock regardless of settings of clock selection register (CKSCR).

Interval Timer Function

- In the watch timer, a bit corresponding to the interval time overflows (carry-over) when an interval time, which is specified by interval time selection bit, is reached. Then overflow flag bit is set (WTC: WTOF=1).
- If an interrupt by overflow is permitted (WTC: WTIE=1), an interrupt request is generated upon setting an overflow flag bit.
- Interval time of watch timer is selectable among the following seven choices:

Interval Time of Watch Timer

Sub Clock Cycle	Interval Time
1/SCLK (122 μs)	2^8/SCLK (31.25 ms)
	2^9/SCLK (62.5 ms)
	2^{10}/SCLK (125 ms)
	2^{11}/SCLK (250 ms)
	2^{12}/SCLK (500 ms)
	2^{13}/SCLK (1.0 s)
	2^{14}/SCLK (2.0 s)

SCLK: Sub clock frequency

Values in parentheses “( )” are calculation when operating with 8.192 kHz clock.

12.8 Delay Interrupt Generation Module Outline

The delay interrupt generation module is a module that generates interrupts for switching tasks. Generation of a hardware interrupt request is performed by software.

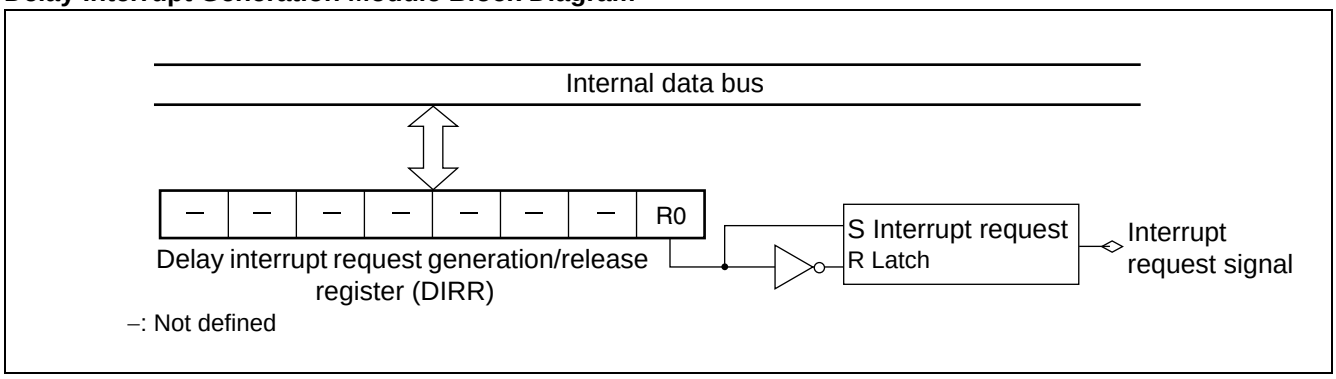
Delay Interrupt Generation Module Outline

Using the delay interrupt generation module, hardware interrupt request is generated and released by software.

Table 12-1. Delay Interrupt Generation Module Outline

	Function and Control
Cause of interrupt	Set “1” in R0 bit of delay interrupt request generation/release register (DIRR: R0=1), generating an interrupt request. Set “0” in R0 bit of delay interrupt request generation/release register (DIRR: R0=0), releasing an interrupt request.
Interrupt number	#42 ($2A_H$)
Interrupt control	No setting of permission register is provided.
Interrupt flag	Retained in DIRR: R0 bit
EI^2OS	Not ready for expanded intelligent I/O service.

Delay Interrupt Generation Module Block Diagram



Interrupt Request Latch

A latch that retains settings on delay interrupt request generation/release register (generation or release of delay interrupt request).

Delay Interrupt Request Generation/Release Register (DIRR)

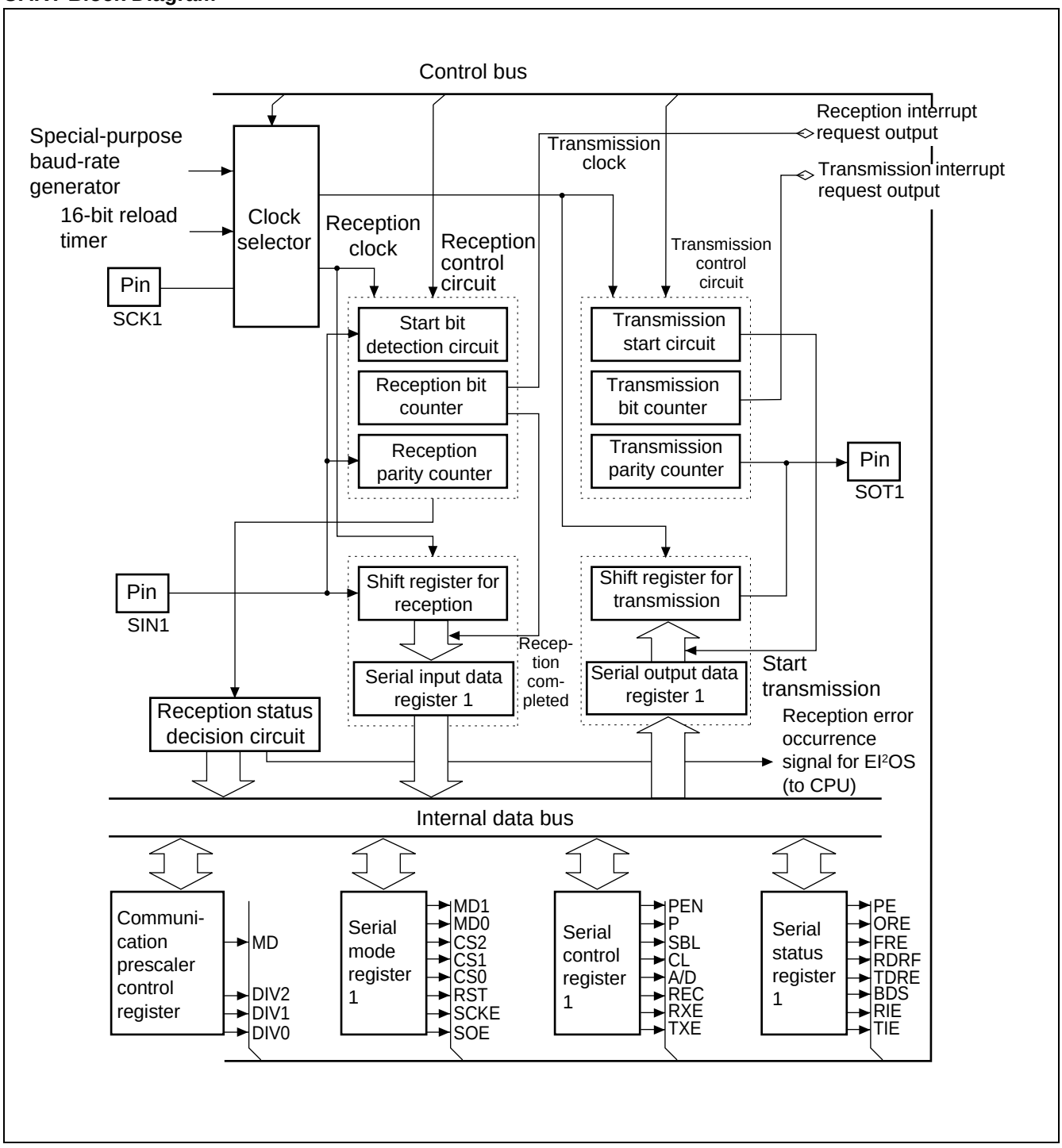
Generates or releases delay interrupt request.

Interrupt Number

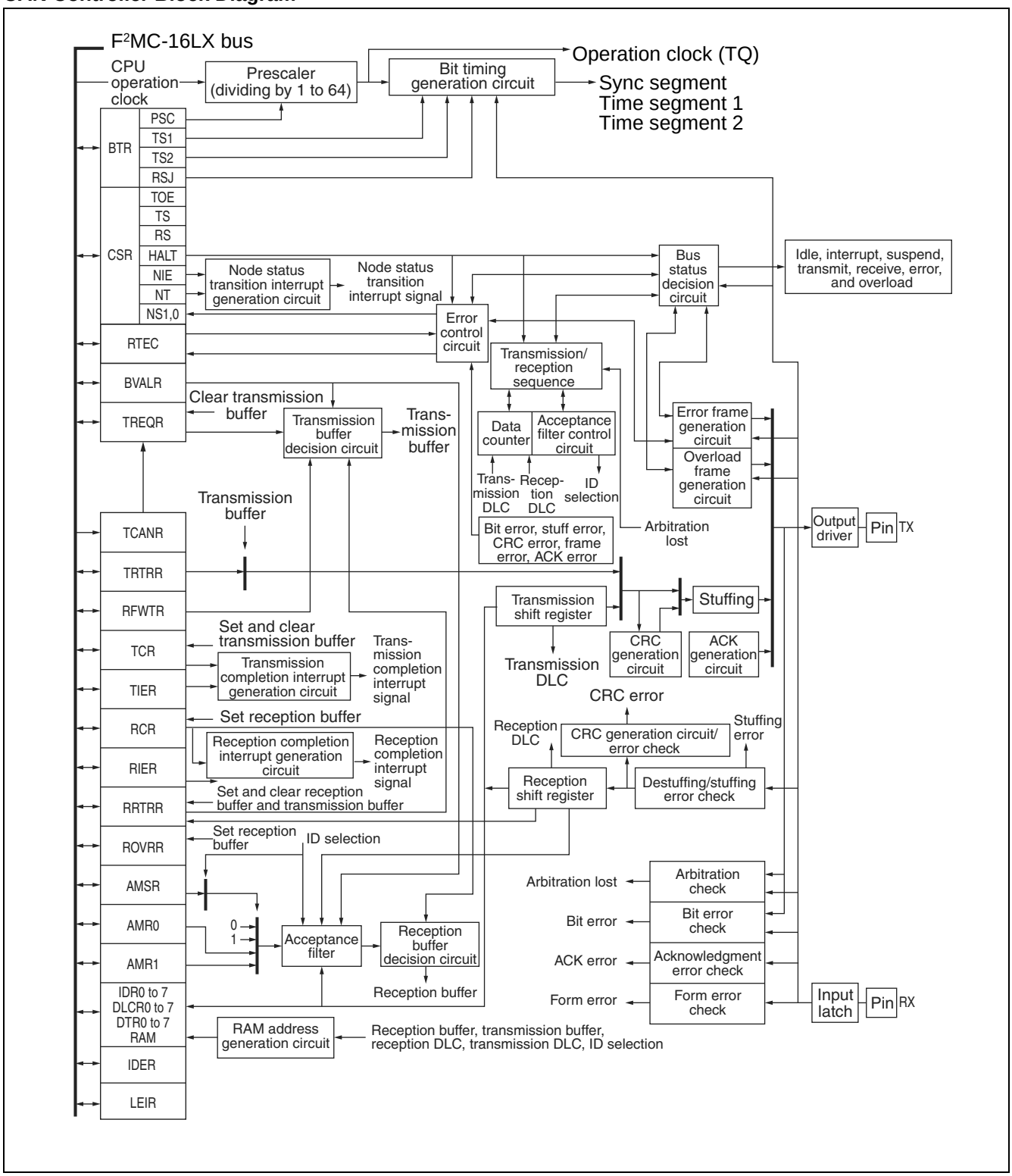
An interrupt number used in delay interrupt generation module is as follows:

Interrupt number: #42 ($2A_H$)

UART Block Diagram



CAN Controller Block Diagram



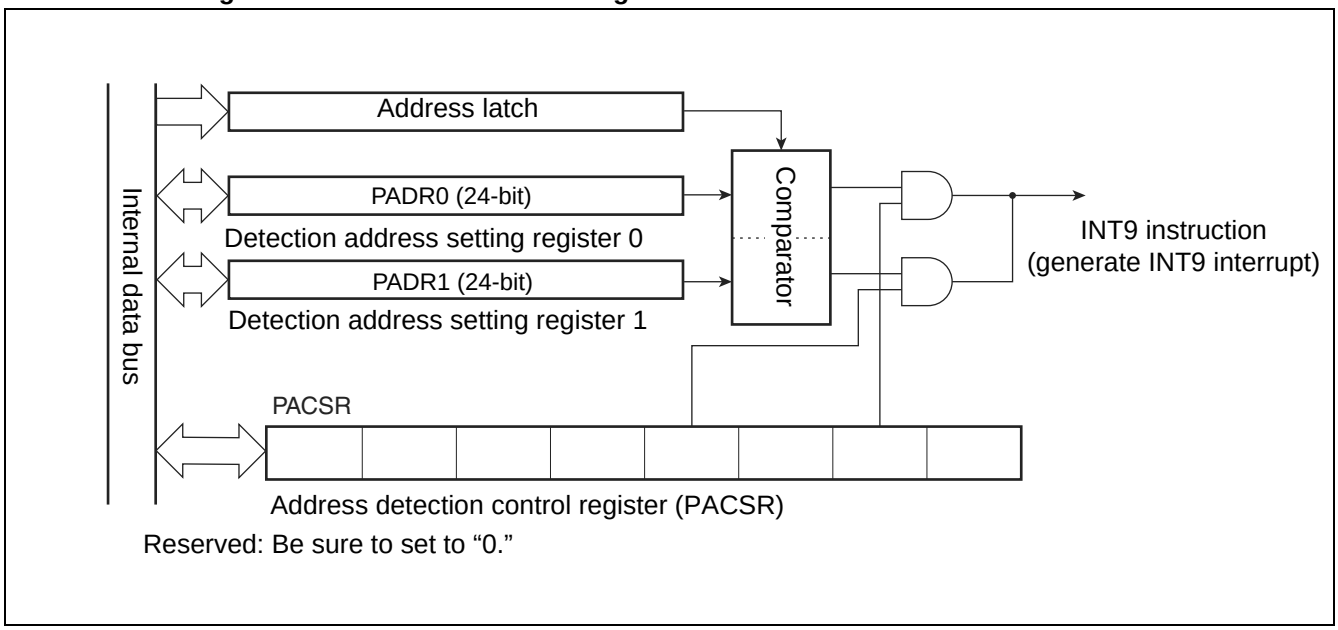
12.13 Address Matching Detection Function Outline

The address matching detection function checks if an address of an instruction to be processed next to a currently-processed instruction is identical with an address specified in the detection address register. If the addresses match with each other, an instruction to be processed next in program is forcibly replaced with INT9 instruction, and process branches to the interrupt process program. Using INT9 interrupt, this function is available for correcting program by batch processing.

Address Matching Detection Function Outline

- An address of an instruction to be processed next to a currently-processed instruction of the program is always retained in an address latch via internal data bus. By the address matching detection function, the address value retained in the address latch is always compared with an address specified in detection address setting register. If the compared address values match with each other, an instruction to be processed next by CPU is forcibly replaced with INT9 instruction, and an interrupt process program is executed.
- Two detection address setting registers are provided (PADR0 and PADR1), and each register is provided with interrupt permission bit. Generation of interrupt, which is caused by address matching between the address retained in address latch and the address specified in address setting register, is permitted and prohibited on a register-by-register basis.

Address Matching Detection Function Block Diagram



- Address latch

  Retains address value output to internal data bus.

- Address detection control register (PACSR)

  Specifies if interrupt is permitted or prohibited when addresses match with each other.

- Detection address setting (PADR0, PADR1)

  Specifies addresses to be compared with values in address latch.

13.2 Recommended Operating Conditions

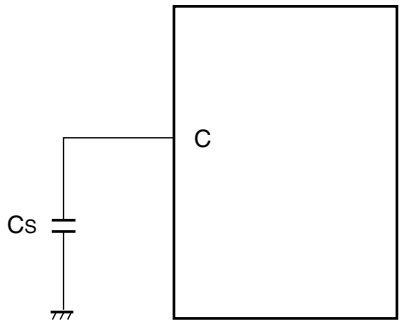
(V_{SS} = AV_{SS} = 0.0V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	V_{CC}	3.5	5.0	5.5	V	Under normal operation
		3.0	–	5.5	V	Retain status of stop operation
	AV_{CC}	4.0	–	5.5	V	*2
Smoothing capacitor	C_S	0.1	–	1.0	μF	*1
Operating temperature	T_A	−40	–	+105	°C	

*1: Use a ceramic capacitor, or a capacitor of similar frequency characteristics. On the Vcc pin, use a bypass capacitor that has a larger capacity than that of Cs.
Refer to the following figure for connection of smoothing capacitor Cs.

*2: AVcc is a voltage at which accuracy is guaranteed. AVcc should not exceed Vcc.

- C pin connection diagram



WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current*	I_{CCL}	V_{CC}	V_{CC} = 5.0 V, Internally operating at 8 kHz, subclock operation, T_A = + 25°C	—	0.3	1.2	mA	MB90F387/S
				—	40	100	µA	MB90387/S
	I_{CCLS}		V_{CC} = 5.0 V, Internally operating at 8 kHz, subclock, sleep mode, T_A = + 25°C	—	10	30	µA	
	I_{CCT}		V_{CC} = 5.0 V, Internally operating at 8 kHz, watch mode, T_A = + 25°C	—	8	25	µA	
	I_{CCH}		Stopping, T_A = + 25°C	—	5	20	µA	
Input capacity	C_{IN}	Other than AV_{CC}, AV_{SS}, AVR, C, V_{CC}, V_{SS}	–	—	5	15	pF	
Pull-up resistor	R_{UP}	RST	–	25	50	100	kΩ	
Pull-down resistor	R_{DOWN}	MD2	–	25	50	100	kΩ	Flash product is not provided with pull-down resistor.

*: Test conditions of power supply current are based on a device using external clock.

13.4 AC Characteristics

13.4.1 Clock Timing

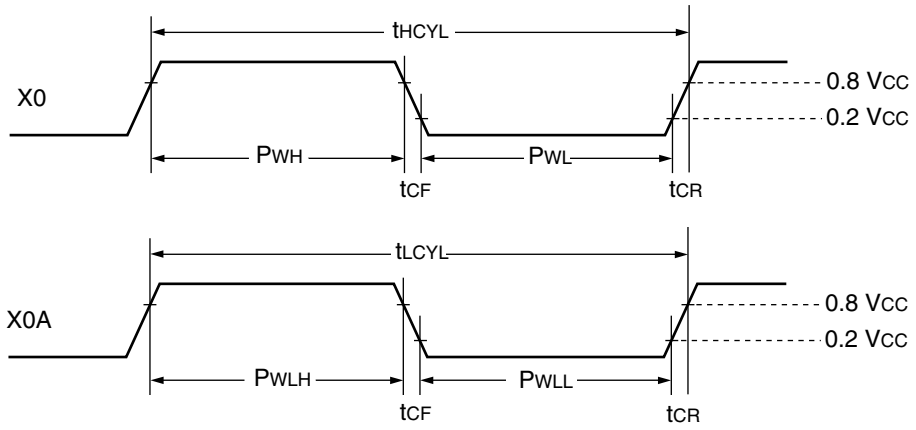
(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_C	X0, X1	3	—	8	MHz	When crystal or ceramic resonator is used*2
			3	—	16	MHz	External clock input*1, *2
			4	—	16	MHz	PLL Multiply by 1 *2
			4	—	8	MHz	PLL Multiply by 2 *2
			4	—	5.33	MHz	PLL Multiply by 3 *2
			4	—	4	MHz	PLL Multiply by 4 *2
	f_{CL}	X0A, X1A	—	32.768	—	kHz	
Clock cycle time	t_{HCYL}	X0, X1	125	—	333	ns	
	t_{LCYL}	X0A, X1A	—	30.5	—	µs	
Input clock pulse width	P_{WH}, P_{WL}	X0	10	—	—	ns	Set duty factor at 30% to 70% as a guideline.
	P_{WLH},P_{WLL}	X0A	—	15.2	—	µs	
Input clock rise time and fall time	t_{CR}, t_{CF}	X0	—	—	5	ns	When external clock is used
Internal operation clock frequency	f_{CP}	—	1.5	—	16	MHz	When main clock is used
	f_{LCP}	—	—	8.192	—	kHz	When sub clock is used
Internal operation clock cycle time	t_{CP}	—	62.5	—	666	ns	When main clock is used
	t_{LCP}	—	—	122.1	—	µs	When sub clock is used

*1: Internal operation clock frequency should not exceed 16 MHz.

*2: When selecting the PLL clock, the range of clock frequency is limited. Use this product within range as mentioned in “Relation among external clock frequency and internal clock frequency”.

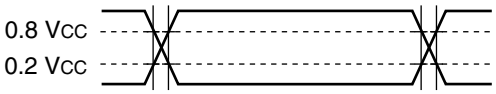
• Clock timing



Rating values of alternating current is defined by the measurement reference voltage values shown below:

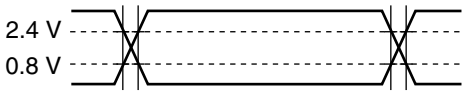
- Input signal waveform

Hysteresis input pin



- Output signal waveform

Output pin



13.4.2 Reset Input Timing

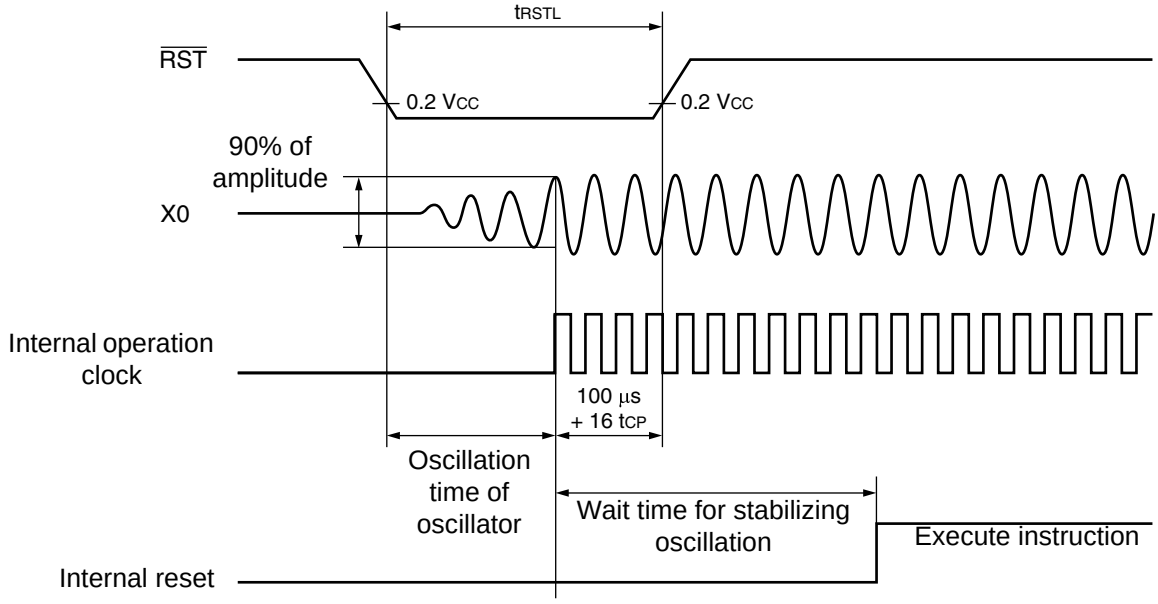
Parameter	Symbol	Pin Name	Value		Unit	Remarks
			Min	Max		
Reset input time	t_{RSTL}	RST	16 t_{CP}*3	–	ns	Normal operation
			Oscillation time of oscillator*1 + 100 μs + 16 t_{CP}*3	–	–	In sub clock*2, sub sleep*2, watch*2 and stop mode
			100	–	μs	In timebase timer

*1: Oscillation time of oscillator is time that the amplitude reached the 90%. In the crystal oscillator, the oscillation time is between several ms to tens of ms. In ceramic oscillator, the oscillation time is between hundreds of μs to several ms. In the external clock, the oscillation time is 0 ms.

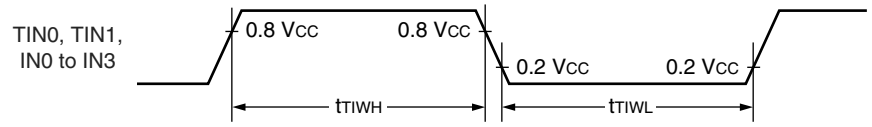
*2: Except for MB90F387S and MB90387S.

*3: Refer to "(1) Clock timing" ratings for t_{CP} (internal operation clock cycle time).

- In sub clock, sub sleep, watch and stop mode



• Timer input timing



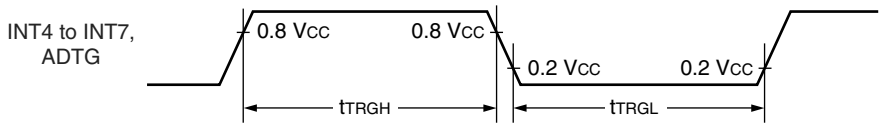
13.4.6 Trigger Input Timing

(V_{CC} = 4.5 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH} t_{TRGL}	INT4 to INT7, ADTG	–	5 t_{CP} *	–	ns	

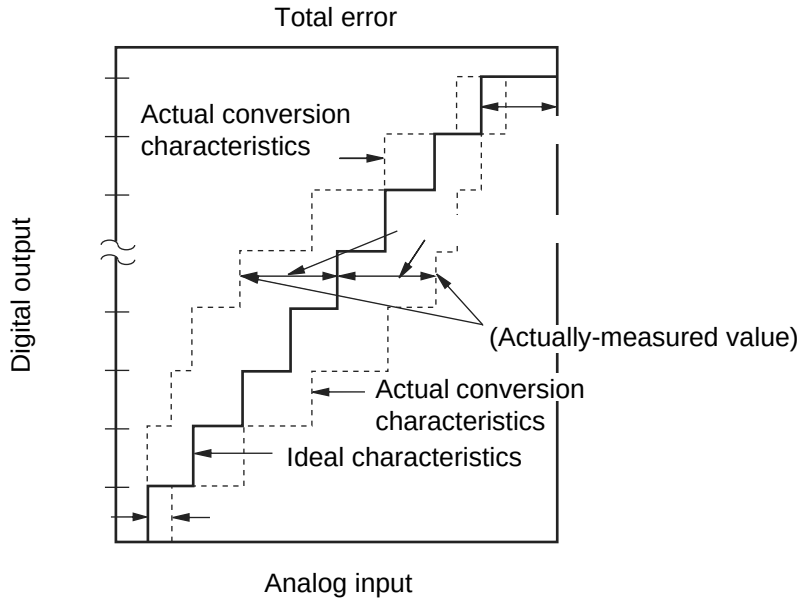
*: Refer to Clock Timing ratings for t_{CP} (internal operation clock cycle time).

• Trigger input timing



13.6 Definition of A/D Converter Terms

Resolution:	Analog variation that is recognized by an A/D converter.
Linear error:	Deviation between a line across zero-transition line (“00 0000 00 0 0” ←→“00 0000 0001”) and full-scale transition line (“11 1111 11 1 0” ←→ “11 1111 1111”) and actual conversion characteristics.
Differential linear error:	Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.
Total error:	Difference between an actual value and an ideal value. A total error includes zero transition error, full-scale transition error, and linear error.



$$\text{Total error of digital output “N”} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}} \quad [\text{LSB}]$$

$$1\ \text{LSB} = (\text{Ideal value})\ \frac{AVR - AV_{SS}}{1024}\ [V]$$

V_{OT} (Ideal value) = AV_{SS} + 0.5 LSB [V]

V_{FST} (Ideal value) = AVR − 1.5 LSB [V]

V_{NT}: A voltage at which digital output transits from $(N\text{-}1)_H$ to N_H.

(Continued)

Document History

Document Title: MB90387/387S/F387/F387S, MB90V495G, 16-bit Microcontrollers F²MC-16LX MB90385 Series Document Number:002-07765				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	—	AKIH	12/19/2008	Migrated to Cypress and assigned document number 002-07765. No change to document contents or format.
*A	6059071	SSAS	02/05/2018	Updated to Cypress template Package: FPT-48P-M26 --> LQA048