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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	F ² MC-16LX
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, SCI, UART/USART
Peripherals	POR, WDT
Number of I/O	36
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90f387spmcr-g-ef2

16-bit Microcontrollers F²MC-16LX MB90385 Series

MB90385 series devices are general-purpose high-performance 16-bit micro controllers designed for process control of consumer products, which require high-speed real-time processing. The devices of this series have the built-in full-CAN interface.

The system, inheriting the architecture of F²MC family, employs additional instruction ready for high-level languages, expanded addressing mode, enhanced multiply-divide instructions, and enriched bit-processing instructions. Furthermore, employment of 32-bit accumulator achieves processing of long-word data (32 bits).

The peripheral resources of MB90385 series include the following:

8/10-bit A/D converter, UART (SCI), 8/16-bit PPG timer, 16-bit input-output timer (16-bit free-run timer, input capture 0, 1, 2, 3 (ICU)), and CAN controller.

Features

Clock

- Built-in PLL clock frequency multiplication circuit
- Selection of machine clocks (PLL clocks) is allowed among frequency division by two on oscillation clock, and multiplication of 1 to 4 times of oscillation clock (for 4-MHz oscillation clock, 4 MHz to 16 MHz).
- Operation by sub-clock (8.192 kHz) is allowed. (MB90387, MB90F387)
- Minimum execution time of instruction: 62.5 ns (when operating with 4-MHz oscillation clock, and 4-time multiplied PLL clock).

16 Mbyte CPU memory Space

- 24-bit internal addressing

Instruction System Best Suited to Controller

- Wide choice of data types (bit, byte, word, and long word)
- Wide choice of addressing modes (23 types)
- Enhanced multiply-divide instructions and RETI instructions
- Enhanced high-precision computing with 32-bit accumulator

Instruction System Compatible with High-level Language (C language) and Multitask

- Employing system stack pointer
- Enhanced various pointer indirect instructions
- Barrel shift instructions

Increased Processing Speed

- 4-byte instruction queue

Powerful Interrupt Function with 8 Levels and 34 Factors

Automatic Data Transfer Function Independent of CPU

- Expanded intelligent I/O service function (EI² OS): Maximum of 16 channels

Low Power Consumption (standby) Mode

- Sleep mode (a mode that halts CPU operating clock)

- Time-base timer mode (a mode that operates oscillation clock, sub clock, time-base timer and watch timer only)
- Watch mode (a mode that operates sub clock and watch timer only)
- Stop mode (a mode that stops oscillation clock and sub clock)
- CPU blocking operation mode

Process

- CMOS technology

I/O Port

- General-purpose input/output port (CMOS output):
MB90387, MB90F387: 34 ports (including 4 high-current output ports)
MB90387S, MB90F387S: 36 ports (including 4 high-current output ports)

Timer

- Time-base timer, watch timer, watchdog timer: 1 channel
- 8/16-bit PPG timer: 8-bit x 4 channels, or 16-bit x 2 channels
- 16-bit reload timer: 2 channels
- 16-bit input/output timer
 - 16-bit free run timer: 1 channel
 - 16-bit input capture: (ICU): 4 channelsInterrupt request is issued upon latching a count value of 16-bit free run timer by detection of an edge on pin input.

CAN Controller: 1 channel

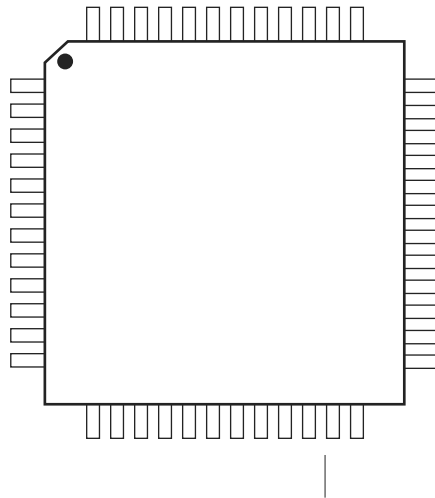
- Compliant with Ver2.0A and Ver2.0B CAN specifications
- 8 built-in message buffers
- Transmission rate of 10 kbps to 1 Mbps (by 16 MHz machine clock)
- CAN wake-up

UART (SCI): 1 channel

- Equipped with full-duplex double buffer
- Clock-asynchronous or clock-synchronous serial transmission is available.

4. Pin Assignment

(Top View)



(LQA048)

*: MB90387, MB90F387 : X1A, X0A
MB90387S, MB90F387S: P36, P35

Pin No.	Pin Name	Circuit Type	Function
39	P42	D	General-purpose input/output port.
	SOT1		Serial data input pin for UART. Valid only when serial data input/output setting on UART is "enabled."
40	P43	D	General-purpose input/output port.
	TX		Transmission output pin for CAN. Valid only when output setting is "enabled."
41	P44	D	General-purpose input/output port.
	RX		Transmission output pin for CAN. Valid only when output setting is "enabled."
42 to 45	P30 to P33	D	General-purpose input/output ports.
46	X0A*	A	Pin for low-rate oscillation.
	P35*		General-purpose input/output port.
47	X1A*	A	Pin for low-rate oscillation.
	P36*		General-purpose input/output port.
48	AVss	—	Vss power source input pin for A/D converter.

*: MB90387, MB90F387: X1A, X0A
 MB90387S, MB90F387S: P36, P35

Address	Register Abbreviation	Register	Read/Write	Resource	Initial Value
003C38 _H , 003C39 _H	DLCR4	DLC register 4	R/W	CAN controller	XXXXXXXX _B , XXXXXXXX _B
003C3A _H , 003C3B _H	DLCR5	DLC register 5	R/W		XXXXXXXX _B , XXXXXXXX _B
003C3C _H , 003C3D _H	DLCR6	DLC register 6	R/W		XXXXXXXX _B , XXXXXXXX _B
003C3E _H , 003C3F _H	DLCR7	DLC register 7	R/W		XXXXXXXX _B , XXXXXXXX _B
003C40 _H to 003C47 _H	DTR0	Data register 0	R/W		XXXXXXXX _B to XXXXXXXX _B
003C48 _H to 003C4F _H	DTR1	Data register 1	R/W		XXXXXXXX _B to XXXXXXXX _B
003C50 _H to 003C57 _H	DTR2	Data register 2	R/W		XXXXXXXX _B to XXXXXXXX _B
003C58 _H to 003C5F _H	DTR3	Data register 3	R/W		XXXXXXXX _B to XXXXXXXX _B
003C60 _H to 003C67 _H	DTR4	Data register 4	R/W		XXXXXXXX _B to XXXXXXXX _B
003C68 _H to 003C6F _H	DTR5	Data register 5	R/W		XXXXXXXX _B to XXXXXXXX _B
003C70 _H to 003C77 _H	DTR6	Data register 6	R/W		XXXXXXXX _B to XXXXXXXX _B
003C78 _H to 003C7F _H	DTR7	Data register 7	R/W		XXXXXXXX _B to XXXXXXXX _B
003C80 _H to 003CFF _H	(Reserved area) *				
003D00 _H , 003D01 _H	CSR	Control status register	R/W, R	CAN controller	0XXXX001 _B , 00XXX000 _B
003D02 _H	LEIR	Last event display register	R/W		000XX000 _B
003D03 _H	(Reserved area) *				
003D04 _H , 003D05 _H	RTEC	Send/receive error counter	R	CAN controller	00000000 _B , 00000000 _B
003D06 _H , 003D07 _H	BTR	Bit timing register	R/W		11111111 _B , X1111111 _B
003D08 _H	IDER	IDE register	R/W		XXXXXXXX _B
003D09 _H	(Reserved area) *				
003D0A _H	TRTRR	Send RTR register	R/W	CAN controller	00000000 _B
003D0B _H	(Reserved area) *				
003D0C _H	RFWTR	Remote frame receive wait register	R/W	CAN controller	XXXXXXXX _B

Address	Register Abbreviation	Register	Read/Write	Resource	Initial Value
003D0D _H	(Reserved area) *				
003D0E _H	TIER	Send completion interrupt permission register	R/W	CAN controller	00000000 _B
003D0F _H	(Reserved area) *				
003D10 _H , 003D11 _H	AMSR	Acceptance mask selection register	R/W	CAN controller	XXXXXXXX _B , XXXXXXXX _B
003D12 _H , 003D13 _H	(Reserved area) *				
003D14 _H to 003D17 _H	AMR0	Acceptance mask register 0	R/W	CAN controller	XXXXXXXX _B to XXXXXXXX _B
003D18 _H to 003D1B _H	AMR1	Acceptance mask register 1	R/W		XXXXXXXX _B to XXXXXXXX _B
003D1C _H to 003DFF _H	(Reserved area) *				
003E00 _H to 003EFF _H	(Reserved area) *				
003FF0 _H to 003FFF _H	(Reserved area) *				

Initial values:

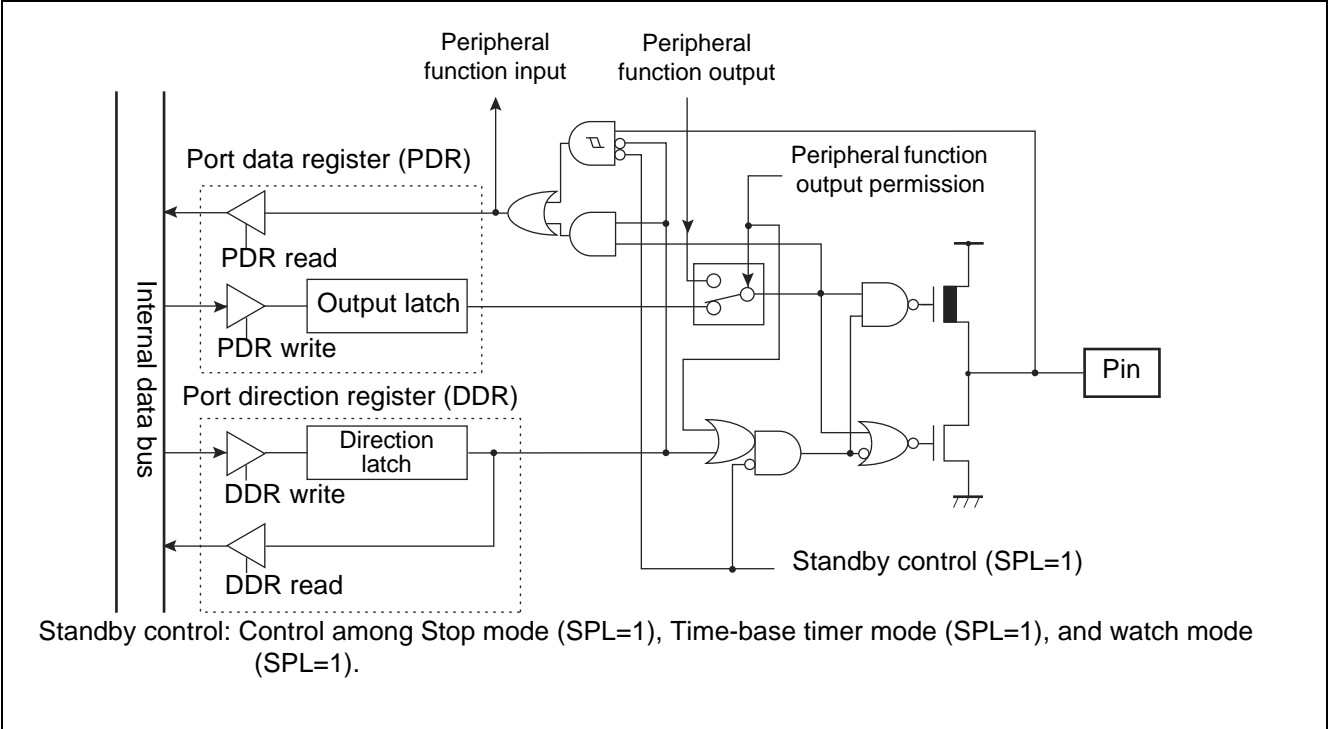
0: Initial value of this bit is "0."

1: Initial value of this bit is "1."

X: Initial value of this bit is undefined.

*: "Reserved area" should not be written anything. Result of reading from "Reserved area" is undefined.

Port 2 Pins Block Diagram (general-purpose input/output port)



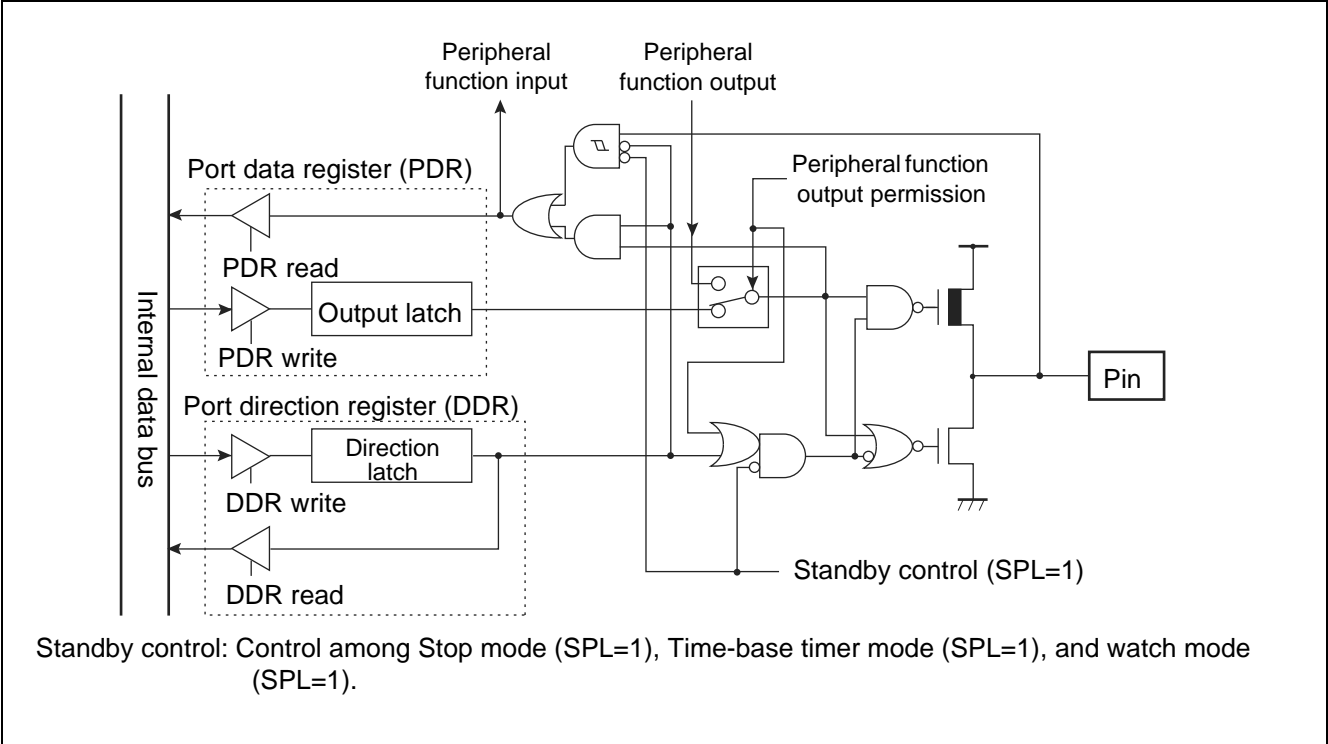
Port 2 Registers

- Port 2 registers include port 2 data register (PDR2) and port 2 direction register (DDR2).
- The bits configuring the register correspond to port 2 pins on a one-to-one basis.

Relation between Port 2 Registers and Pins

Port Name	Bits of Register and Corresponding Pins								
Port 2	PDR2,DDR2	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	Corresponding pins	P27	P26	P25	P24	P23	P22	P21	P20

Port 3 Pins Block Diagram (general-purpose input/output port)



Port 3 Registers

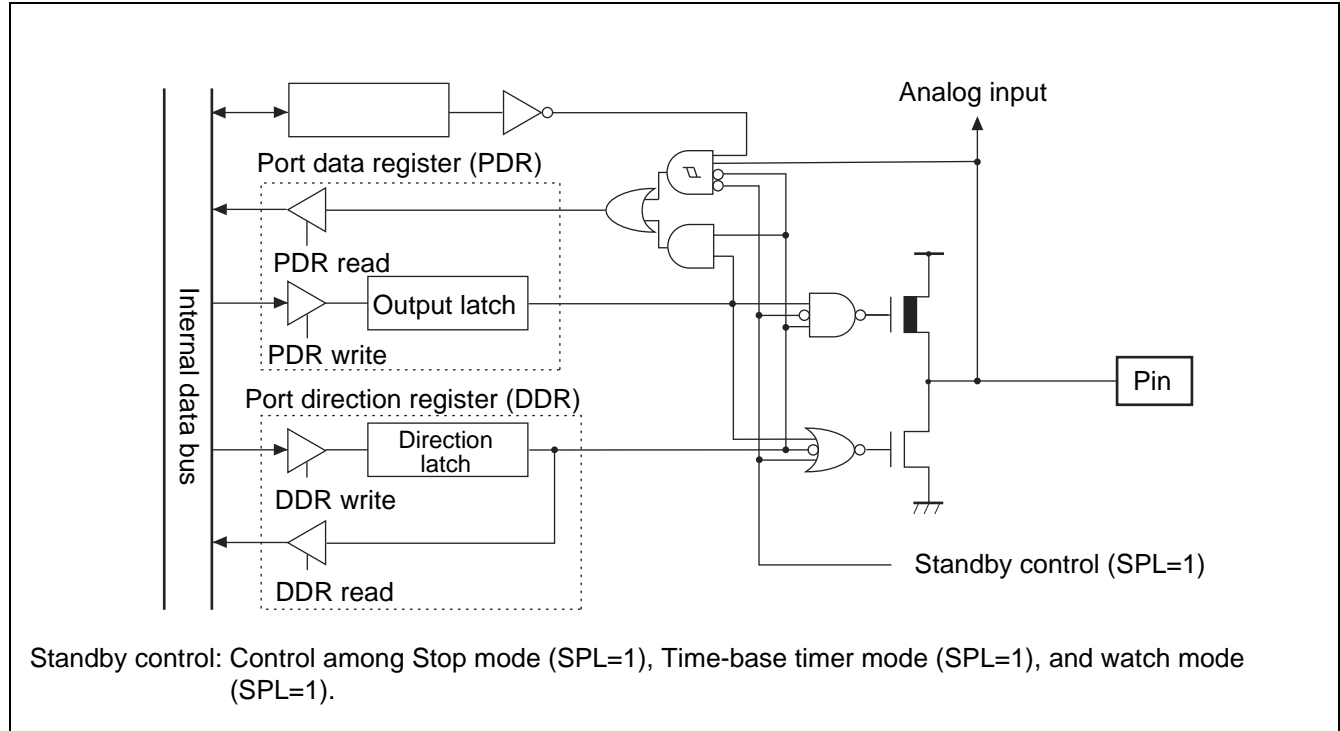
- Port 3 registers include port 3 data register (PDR3) and port 3 direction register (DDR3).
- The bits configuring the register correspond to port 3 pins on a one-to-one basis.

Relation between Port 3 Registers and Pins

Port Name	Bits of Register and Corresponding Pins								
Port 3	PDR3, DDR3	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	Corresponding pins	P37	P36*	P35*	–	P33	P32	P31	P30

*: P35 and P36 do not exist on MB90387and MB90F387.

Port 5 Pins Block Diagram



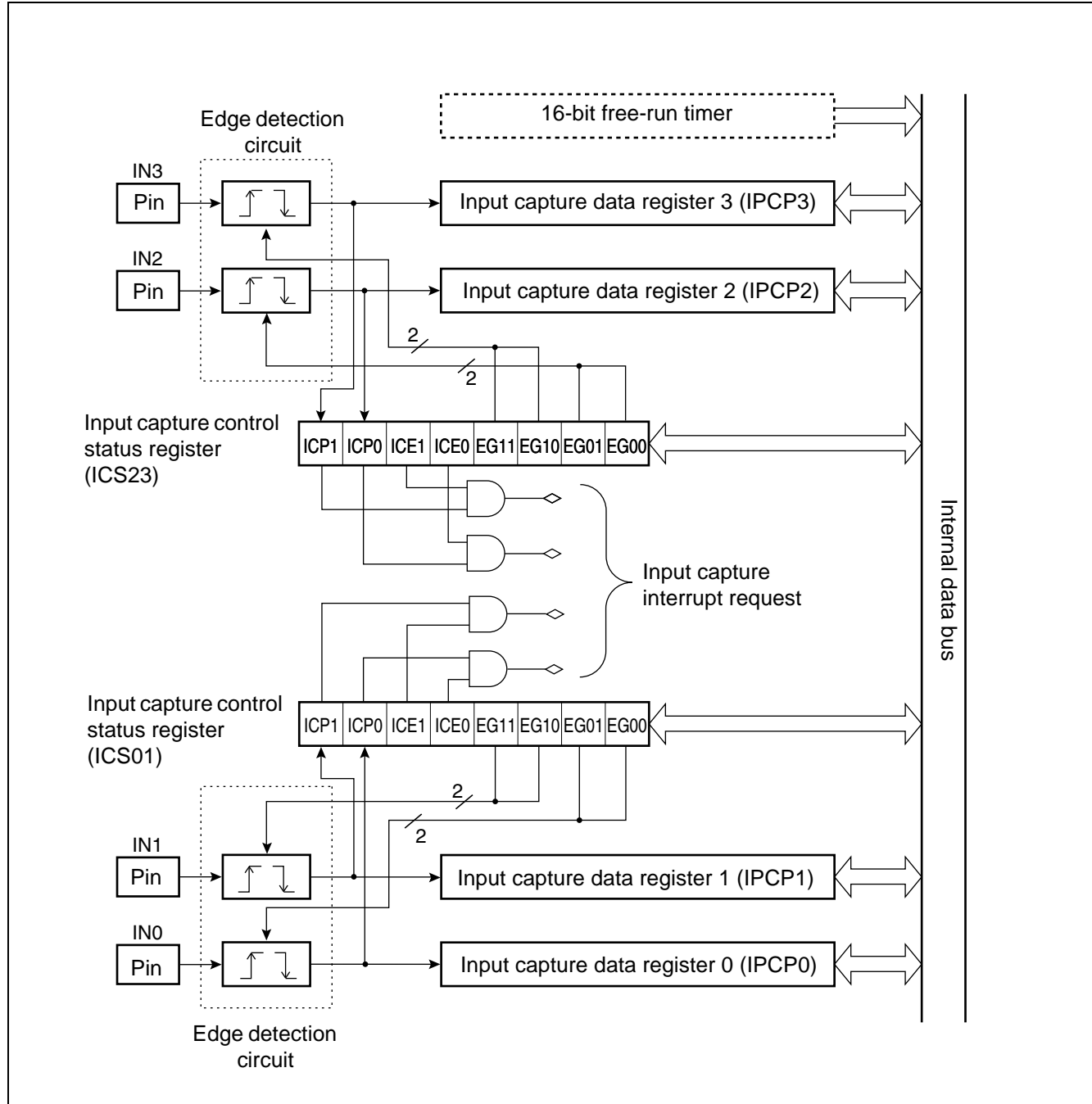
Port 5 Registers

- Port 5 registers include port 5 data register (PDR5), port 5 direction register (DDR5), and analog input permission register (ADER).
- Analog input permission register (ADER) allows or disallows input of analog signal to the analog input pin.
- The bits configuring the register correspond to port 5 pins on a one-to-one basis.

Relation between Port 5 Registers and Pins

Port Name	Bits of Register and Corresponding Pins								
Port 5	PDR5, DDR5	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	ADER	ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0
	Corresponding pins	P57	P56	P55	P54	P53	P52	P51	P50

Input Capture Block Diagram



12.5 16-bit Reload Timer

The 16-bit reload timer has the following functions:

- Count clock is selectable among 3 internal clocks and external event clock.
- Activation trigger is selectable between software trigger and external trigger.
- Generation of CPU interrupt is allowed upon occurrence of underflow on 16-bit timer register. Available as an interval timer using the interrupt function.
- When underflow of 16-bit timer register (TMR) occurs, one of two reload modes is selectable between one-shot mode that halts counting operation of TMR, and reload mode that reloads 16-bit reload register value to TMR, continuing TMR counting operation.
- The 16-bit reload timer is ready for expanded intelligent I/O service (EI²OS).
- MB90385 series device has 2 channels of built-in 16-bit reload timer.

Operation Mode of 16-bit Reload Timer

Count Clock	Activation Trigger	Operation upon Underflow
Internal clock mode	Software trigger, external trigger	One-shot mode, reload mode
Event count mode	Software trigger	One-shot mode, reload mode

Internal Clock Mode

- The 16-bit reload timer is set to internal clock mode, by setting count clock selection bit (TMCSR: CSL1, CSL0) to "00_b", "01_b", "10_b".
- In the internal clock mode, the counter decrements in synchronization with the internal clock.
- Three types of count clock cycles are selectable by count clock selection bit (TMCSR: CSL1, CSL0) in timer control status register.
- Edge detection of software trigger or external trigger is specified as an activation trigger.

12.6 Watch Timer Outline

The watch timer is a 15-bit free-run counter that increments in synchronization with sub clock.

- Interval time is selectable among 7 choices, and generation of interrupt request is allowed for each interval.
- Provides operation clock to the subclock oscillation stabilizing wait timer and watchdog timer.
- Always uses subclock as a count clock regardless of settings of clock selection register (CKSCR).

Interval Timer Function

- In the watch timer, a bit corresponding to the interval time overflows (carry-over) when an interval time, which is specified by interval time selection bit, is reached. Then overflow flag bit is set (WTC: WTOF=1).
- If an interrupt by overflow is permitted (WTC: WTIE=1), an interrupt request is generated upon setting an overflow flag bit.
- Interval time of watch timer is selectable among the following seven choices:

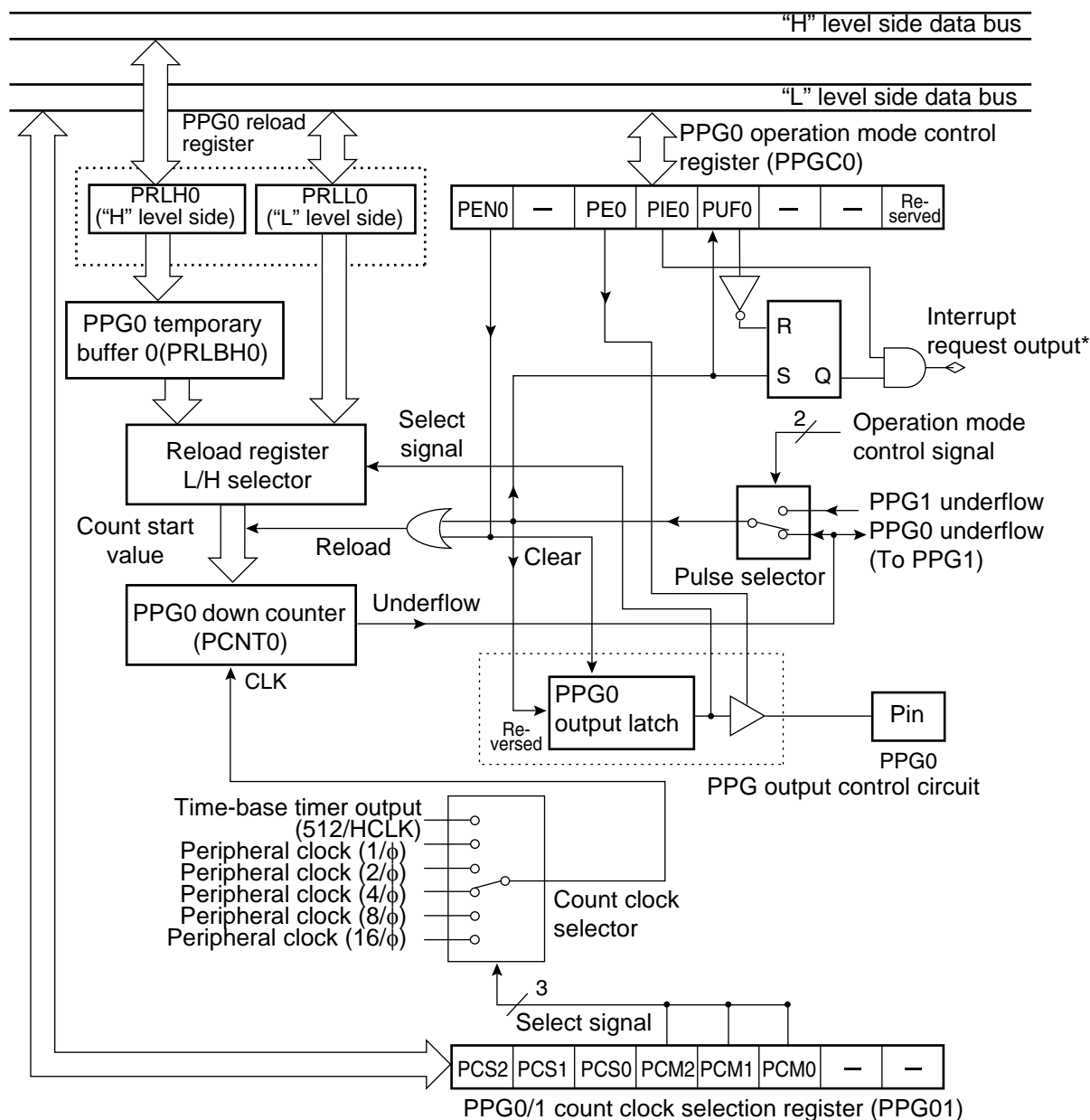
Interval Time of Watch Timer

Sub Clock Cycle	Interval Time
1/SCLK (122 μ s)	2^8 /SCLK (31.25 ms)
	2^9 /SCLK (62.5 ms)
	2^{10} /SCLK (125 ms)
	2^{11} /SCLK (250 ms)
	2^{12} /SCLK (500 ms)
	2^{13} /SCLK (1.0 s)
	2^{14} /SCLK (2.0 s)

SCLK: Sub clock frequency

Values in parentheses “()” are calculation when operating with 8.192 kHz clock.

8/16-bit PPG Timer 0 Block Diagram



— : Undefined

Reserved: Reserved bit

HCLK : Oscillation clock frequency

 ϕ : Machine clock frequency

* : Interrupt output of 8/16-bit PPG timer 0 is incorporated into one by the OR circuit against interrupt output of 8/16-bit PPG timer 1.

12.8 Delay Interrupt Generation Module Outline

The delay interrupt generation module is a module that generates interrupts for switching tasks. Generation of a hardware interrupt request is performed by software.

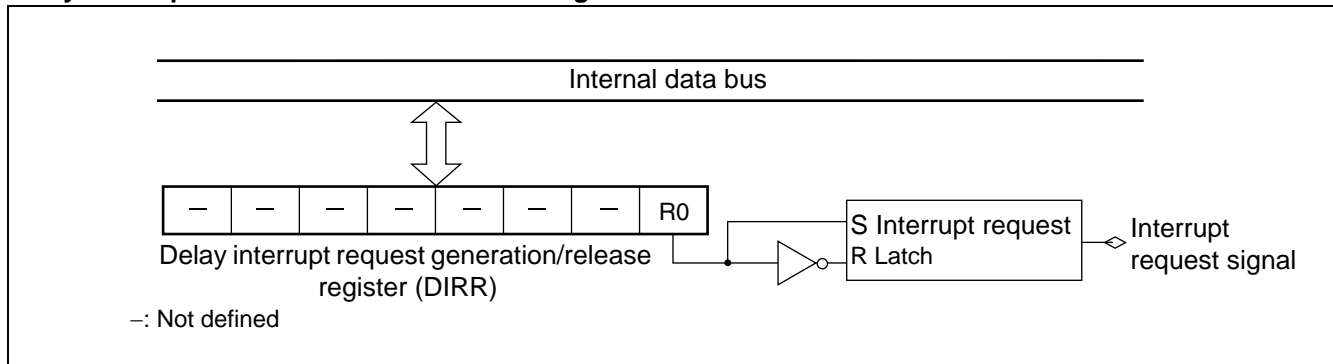
Delay Interrupt Generation Module Outline

Using the delay interrupt generation module, hardware interrupt request is generated and released by software.

Table 12-1. Delay Interrupt Generation Module Outline

	Function and Control
Cause of interrupt	Set "1" in R0 bit of delay interrupt request generation/release register (DIRR: R0=1), generating an interrupt request. Set "0" in R0 bit of delay interrupt request generation/release register (DIRR: R0=0), releasing an interrupt request.
Interrupt number	#42 (2AH)
Interrupt control	No setting of permission register is provided.
Interrupt flag	Retained in DIRR: R0 bit
El ² OS	Not ready for expanded intelligent I/O service.

Delay Interrupt Generation Module Block Diagram



Interrupt Request Latch

A latch that retains settings on delay interrupt request generation/release register (generation or release of delay interrupt request).

Delay Interrupt Request Generation/Release Register (DIRR)

Generates or releases delay interrupt request.

Interrupt Number

An interrupt number used in delay interrupt generation module is as follows:

Interrupt number: #42 (2AH)

12.10 8/10-bit A/D Converter

The 8/10-bit A/D converter converts an analog input voltage into 8-bit or 10-bit digital value, using the RC-type successive approximation conversion method.

- Input signal is selected among 8 channels of analog input pins.
- Activation trigger is selected among software trigger, internal timer output, and external trigger.

Functions of 8/10-bit A/D Converter

The 8/10-bit A/D converter converts an analog voltage (input voltage) input to analog input pin into an 8-bit or 10-bit digital value (A/D conversion).

The 8/10-bit A/D converter has the following functions:

- A/D conversion takes a minimum of 6.12 μs^* for 1 channel, including sampling time. (A/D conversion)
- Sampling of one channel takes a minimum of 2.0 μs^* .
- RC-type successive approximation conversion method, with sample & hold circuit is used for conversion.
- Resolution of either 8 bits or 10 bits is specifiable.
- A maximum of 8 channels of analog input pins are allowed for use.
- Generation of interrupt request is allowed, by storing A/D conversion result in A/D data register.
- Activation of EI²OS is allowed upon occurrence of an interrupt request. With use of EI²OS, data loss is avoided even if A/D conversion is performed successively.
- An activation trigger is selectable among software trigger, internal timer output, and external trigger (fall edge).

: When operating with 16 MHz machine clock

8/10-bit A/D Converter Conversion Mode

Conversion Mode	Description
Singular conversion mode	The A/D conversion is performed from a start channel to an end channel sequentially. Upon completion of A/D conversion on an end channel, A/D conversion function stops.
Sequential conversion mode	The A/D conversion is performed from a start channel to an end channel sequentially. Upon completion of A/D conversion on an end channel, A/D conversion function resumes from the start channel.
Pausing conversion mode	The A/D conversion is performed by pausing at each channel. Upon completion of A/D conversion on an end channel, A/D conversion and pause functions resume from the start channel.

12.15 512 Kbit Flash Memory Outline

The following three methods are provided for data writing and deleting on Flash memory:

1. Parallel writer
2. Serial special-purpose writer
3. Writing/deleting by program execution

This section describes "3. Writing/deleting by program execution."

512 Kbit Flash Memory Outline

The 512 Kbit Flash memory is allocated on FF_H bank of CPU memory map. Using the function of Flash memory interface circuit, the memory allows read access and program access from CPU.

Writing/deleting on Flash memory is performed by instruction from CPU via Flash memory interface. Because rewriting is allowed on mounted memory, modifying program and data is performed efficiently.

Features of 512 Kbit Flash Memory

- 128 K words x 8 bits/64 K words x 16 bits (16 K + 8 K + 8 K + 32 K) sector configuration
- Automatic program algorithm (Embedded Algorithm: Similar to MBM29LV200.)
- Built-in deletion pause/deletion resume function
- Detection of completed writing/deleting by data polling and toggle bits.
- Detection of completed writing/deleting by CPU interrupt.
- Deletion is allowed on a sector-by-sector basis (sectors are combined freely).
- Number of writing/deleting operations (minimum): 10,000 times
- Sector protection
- Expanded sector protection
- Temporal sector unprotection

Note: A function of reading manufacture code and device code is not provided. These codes are not accessible by command either.

Flash Memory Writing/Deleting

- Writing and reading data is not allowed simultaneously on the Flash memory.
- Data writing and deleting on the Flash memory is performed by the processes as follows: Make a copy of program on Flash memory onto RAM. Then, execute the program copied on the RAM.

List of Registers and Reset Values in Flash Memory

Flash memory control status register (FMCS)		bit	7	6	5	4	3	2	1	0
			0	0	0	X	0	0	0	0
x : Undefined										

Sector Configuration

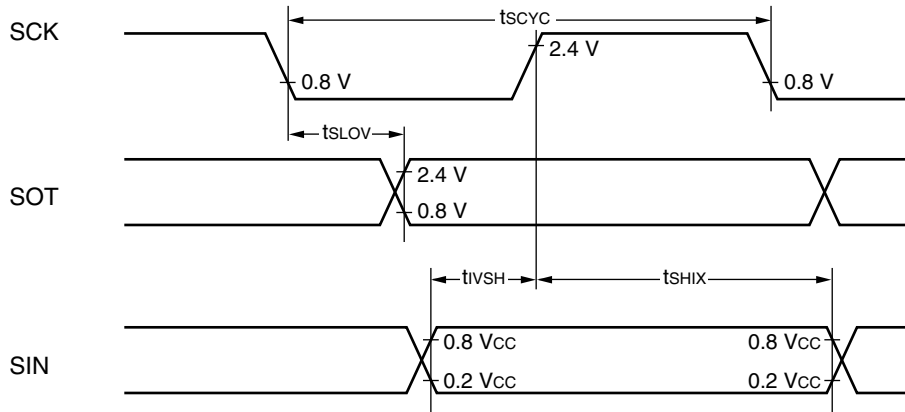
For access from CPU, SA0 to SA3 are allocated in FF bank register.

(V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = -40 °C to +105 °C)

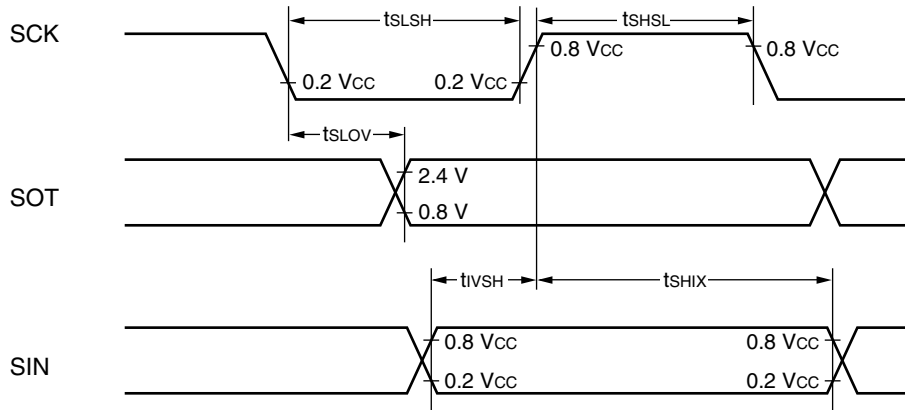
Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current*	I _{CC} L	V _{CC}	V _{CC} = 5.0 V, Internally operating at 8 kHz, subclock operation, T _A = + 25°C	—	0.3	1.2	mA	MB90F387/S
	I _{CC} LS		V _{CC} = 5.0 V, Internally operating at 8 kHz, subclock, sleep mode, T _A = + 25°C	—	40	100	μA	MB90387/S
	I _{CC} T		V _{CC} = 5.0 V, Internally operating at 8 kHz, watch mode, T _A = + 25°C	—	8	25	μA	
	I _{CC} H		Stopping, T _A = + 25°C	—	5	20	μA	
Input capacity	C _{IN}	Other than AV _{CC} , AV _{SS} , AVR, C, V _{CC} , V _{SS}	—	—	5	15	pF	
Pull-up resistor	R _{UP}	RST	—	25	50	100	kΩ	
Pull-down resistor	R _{DOWN}	MD2	—	25	50	100	kΩ	Flash product is not provided with pull-down resistor.

*: Test conditions of power supply current are based on a device using external clock.

• Internal shift clock mode



• External shift clock mode



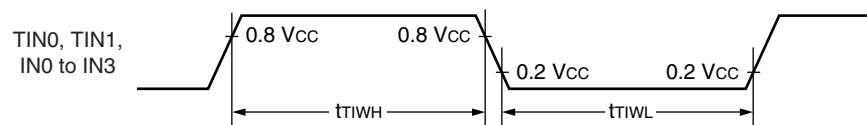
13.4.5 Timer Input Timing

($V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$, $V_{SS} = 0.0 \text{ V}$, $T_A = -40 \text{ }^{\circ}\text{C to } +105 \text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH}	TIN0, TIN1	—	$4 t_{CP}^*$	—	ns	
	t_{TIWL}	IN0 to IN3					

*: Refer to Clock Timing ratings for t_{CP} (internal operation clock cycle time).

• Timer input timing



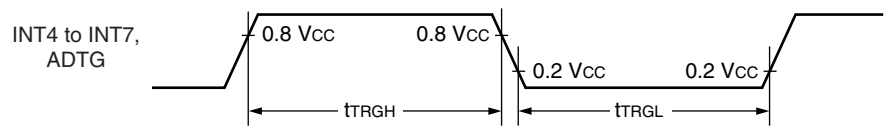
13.4.6 Trigger Input Timing

(V_{CC} = 4.5 V to 5.5 V, V_{SS} = 0.0 V, T_A = -40 °C to +105 °C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t _{TRGH} t _{TRGL}	INT4 to INT7, ADTG	—	5 t _{CP} *	—	ns	

*: Refer to Clock Timing ratings for t_{CP} (internal operation clock cycle time).

• Trigger input timing



15. Ordering Information

Part Number	Package	Remarks
MB90F387PMT MB90387PMT MB90F387SPMT MB90387SPMT	48-pin plastic LQFP (LQA048)	

Document History

Document Title: MB90387/387S/F387/F387S, MB90V495G, 16-bit Microcontrollers F ² MC-16LX MB90385 Series Document Number:002-07765				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	—	AKIH	12/19/2008	Migrated to Cypress and assigned document number 002-07765. No change to document contents or format.
*A	6059071	SSAS	02/05/2018	Updated to Cypress template Package: FPT-48P-M26 --> LQA048