What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.
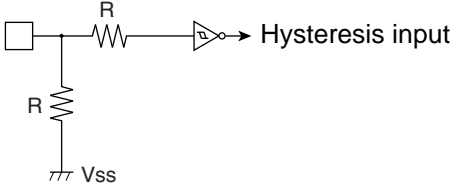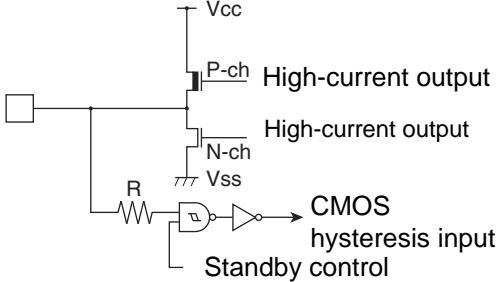
Applications of "Embedded - Microcontrollers"

Details

Product Status	Obsolete
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, SCI, UART/USART
Peripherals	POR, WDT
Number of I/O	36
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90f387spmcr-g-ef2e2

5. Pin Description

Pin No.	Pin Name	Circuit Type	Function
1	AVcc	–	Vcc power input pin for A/D converter.
2	AVR	–	Power (Vref+) input pin for A/D converter. Use as input for Vcc or lower.
3 to 10	P50 to P57	E	General-purpose input/output ports.
	AN0 to AN7		Functions as analog input pins for A/D converter. Valid when analog input setting is "enabled."
11	P37	D	General-purpose input/output port.
	ADTG		Function as an external trigger input pin for A/D converter. Use the pin by setting as input port.
12	P20	D	General-purpose input/output port.
	TIN0		Function as an event input pin for reload timer 0. Use the pin by setting as input port.
13	P21	D	General-purpose input/output port.
	TOT0		Function as an event output pin for reload timer 0. Valid only when output setting is "enabled."
14	P22	D	General-purpose input/output port.
	TIN1		Function as an event input pin for reload timer 1. Use the pin by setting as input port.
15	P23	D	General-purpose input/output port.
	TOT1		Function as an event output pin for reload timer 1. Valid only when output setting is "enabled."
16 to 19	P24 to P27	D	General-purpose input/output ports.
	INT4 to INT7		Functions as external interrupt input pins. Use the pins by setting as input port.
20	MD2	F	Input pin for specifying operation mode. Connect directly to Vss.
21	MD1	C	Input pin for specifying operation mode. Connect directly to Vcc.
22	MD0	C	Input pin for specifying operation mode. Connect directly to Vcc.
23	RST	B	External reset input pin.
24	Vcc	–	Power source (5 V) input pin.
25	Vss	–	Power source (0 V) input pin.
26	C	–	Capacitor pin for stabilizing power source. Connect a ceramic capacitor of approximately 0.1 μF.
27	X0	A	Pin for high-rate oscillation.
28	X1	A	Pin for high-rate oscillation.
29 to 32	P10 to P13	D	General-purpose input/output ports.
	IN0 to IN3		Functions as trigger input pins of input capture ch.0 to ch.3. Use the pins by setting as input ports.
33 to 36	P14 to P17	G	General-purpose input/output ports. High-current output ports.
	PPG0 to PPG3		Functions as output pins of PPG timers 01 and 23. Valid when output setting is "enabled."
37	P40	D	General-purpose input/output port.
	SIN1		Serial data input pin for UART. Use the pin by setting as input port.
38	P41	D	General-purpose input/output port.
	SCK1		Serial clock input pin for UART. Valid only when serial clock input/output setting on UART is "enabled."

Type	Circuit	Remarks
F		■ Hysteresis input with pull-down resistor ■ Pull-down resistor, approx. 50 kΩ ■ Flash product is not provided with pull-down resistor.
G		■ CMOS hysteresis input ■ CMOS level output (high-current output) ■ Standby control provided

7. Handling Devices

Do Not Exceed Maximum Rating (preventing "latch up")

■ On a CMOS IC, latch-up may occur when applying a voltage higher than Vcc or a voltage lower than Vss to input or output pin, which has no middle or high withstand voltage. Latch-up may also occur when a voltage exceeding maximum rating is applied across Vcc pin and Vss pin.

■ Latch-up causes drastic increase of power current, which may lead to destruction of elements by heat. Extreme caution must be taken not to exceed maximum rating.

■ When turning on and off analog power source, take extra care not to apply an analog power voltages (AVcc and AVR) and analog input voltage that are higher than digital power voltage (Vcc).

Handling Unused Pins

■ Leaving unused input pins open may cause permanent destruction by malfunction or latch-up. Apply pull-up or pull-down process to the unused pins using resistors of 2 kΩ or higher. Leave unused input/output pins open under output status, or process as input pins if they are under input status.

Using External Clock

■ When using an external clock, drive only X0 pin and leave X1 pin open. An example of using an external clock is shown below.

• Using external clock
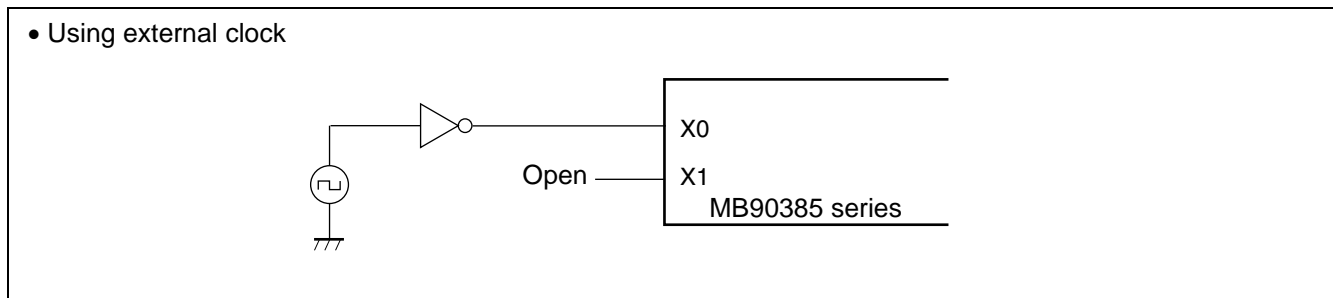
Notes When Using No Sub Clock

■ If an oscillator is not connected to X0A and X1A pin, apply pull-down resistor to X0A pin and leave X1A pin open.

About Power Supply Pins

■ If two or more Vcc and Vss pins exist, the pins that should be at the same potential are connected to each other inside the device. For reducing unwanted emissions and preventing malfunction of strobe signals caused by increase of ground level, however, be sure to connect the Vcc and Vss pins to the power source and the ground externally.

■ Pay attention to connect a power supply to Vcc and Vss of MB90385 series device in a lowest-possible impedance.

■ Near pins of MB90385 series device, connecting a bypass capacitor is recommended at 0.1 μF across Vcc pin and Vss pin.

Crystal Oscillator Circuit

■ Noises around X0 and X1 pins cause malfunctions on a MB90385 series device. Design a print circuit so that X0 and X1 pins, an crystal oscillator (or a ceramic oscillator), and bypass capacitor to the ground become as close as possible to each other. Furthermore, avoid wires to X0 and X1 pins crossing each other as much as possible.

■ Print circuit designing that surrounds X0 and X1 pins with grounding wires, which ensures stable operation, is strongly recommended.

Caution on Operations during PLL Clock Mode

■ If the PLL clock mode is selected, the microcontroller attempt to be working with the self-oscillating circuit even when there is no external oscillator or external clock input is stopped. Performance of this operation, however, cannot be guaranteed.

Sequence of Turning on Power of A/D Converter and Applying Analog Input

■ Be sure to turn on digital power (Vcc) before applying signals to the A/D converter and applying analog input signals (AN0 to AN7 pins).

■ Be sure to turn off the power of A/D converter and analog input before turning off the digital power source.

■ Be sure not to apply AVR exceeding AVcc when turning on and off. (No problems occur if analog and digital power is turned on and off simultaneously.)

Handling Pins When A/D Converter is Not Used

■ If the A/D converter is not used, connect the pins under the following conditions: "AVcc=AVR=Vcc," and "AVss=Vss"

Note on Turning on Power

■ For preventing malfunctions on built-in step-down circuit, maintain a minimum of 50 μs of voltage rising time (between 0.2 V and 2.7V) when turning on the power.

Stabilization of Supply Voltage

■ A sudden change in the supply voltage may cause the device to malfunction even within the specified Vcc supply voltage operating range. Therefore, the Vcc supply voltage should be stabilized.
For reference, the supply voltage should be controlled so that Vcc ripple variations (peak-to-peak values) at commercial frequencies (50 Hz / 60 Hz) fall below 10% of the standard Vcc supply voltage and the coefficient of fluctuation does not exceed 0.1 V/ms at instantaneous power switching.
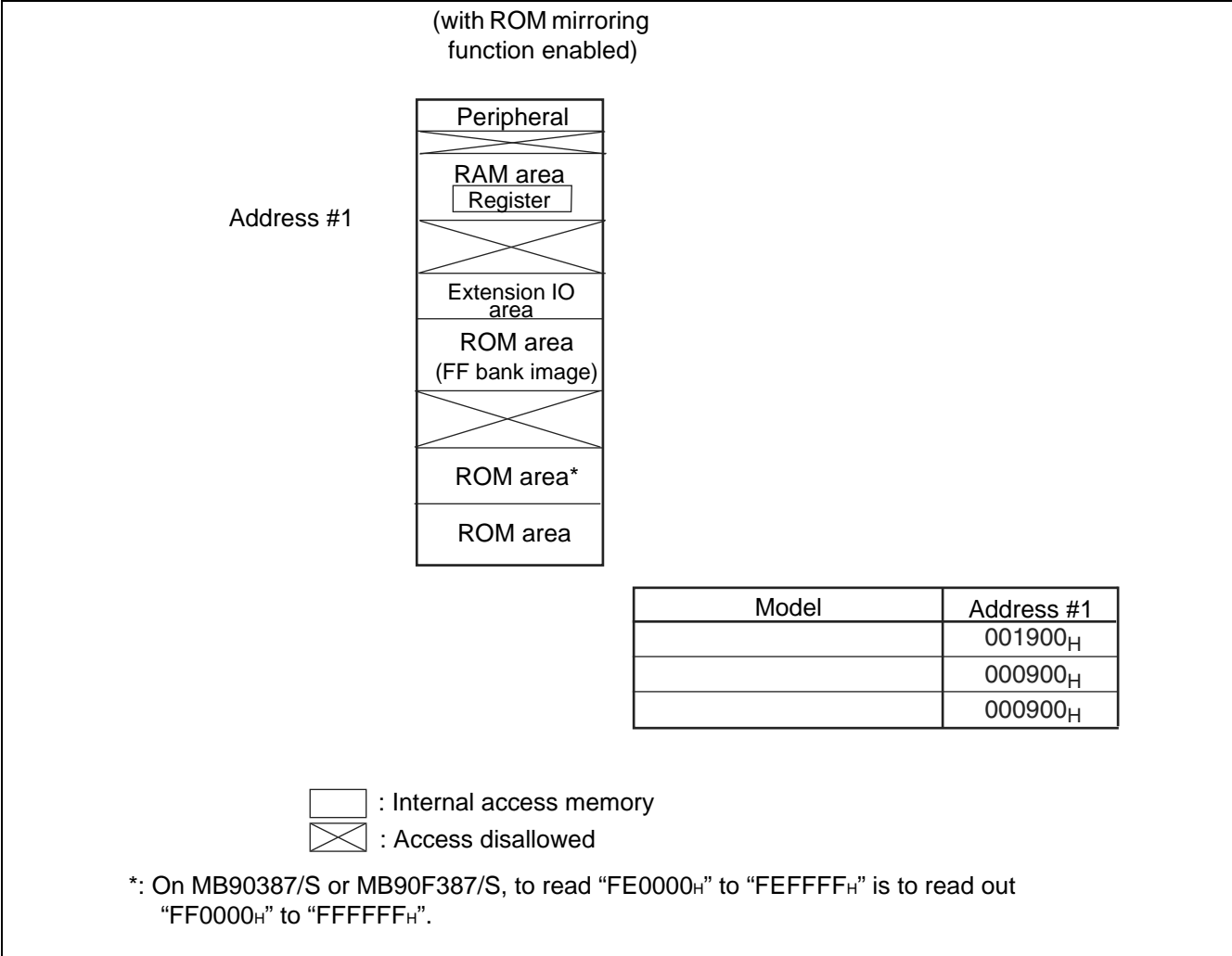
8. Block Diagram
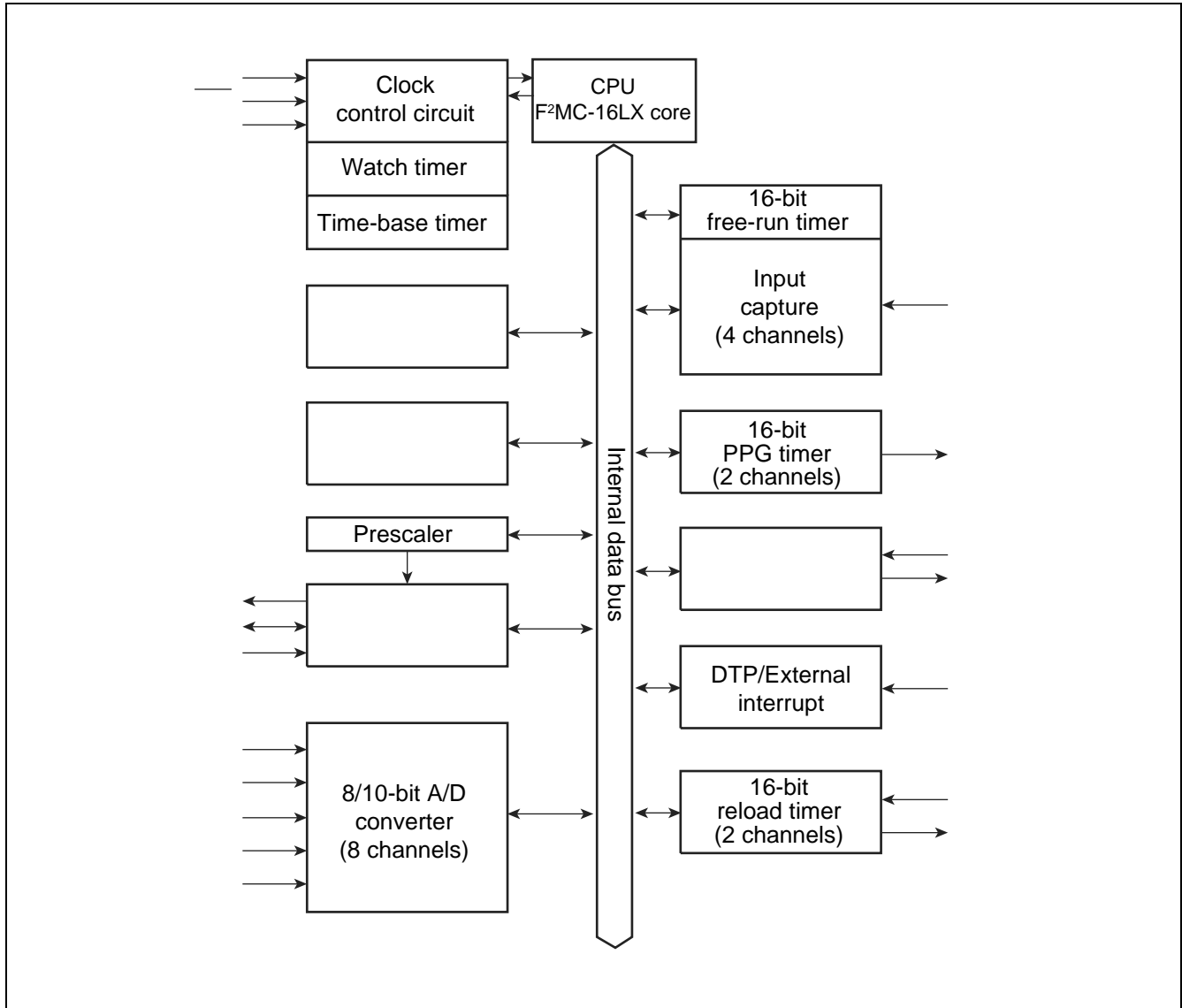
9. Memory Map

MB90385 series allows specifying a memory access mode "single chip mode."

9.1 Memory Allocation of MB90385

MB90385 series model has 24-bit wide internal address bus and up to 24-bit bus of external address bus.
A maximum of 16-Mbyte memory space of external access memory is accessible.
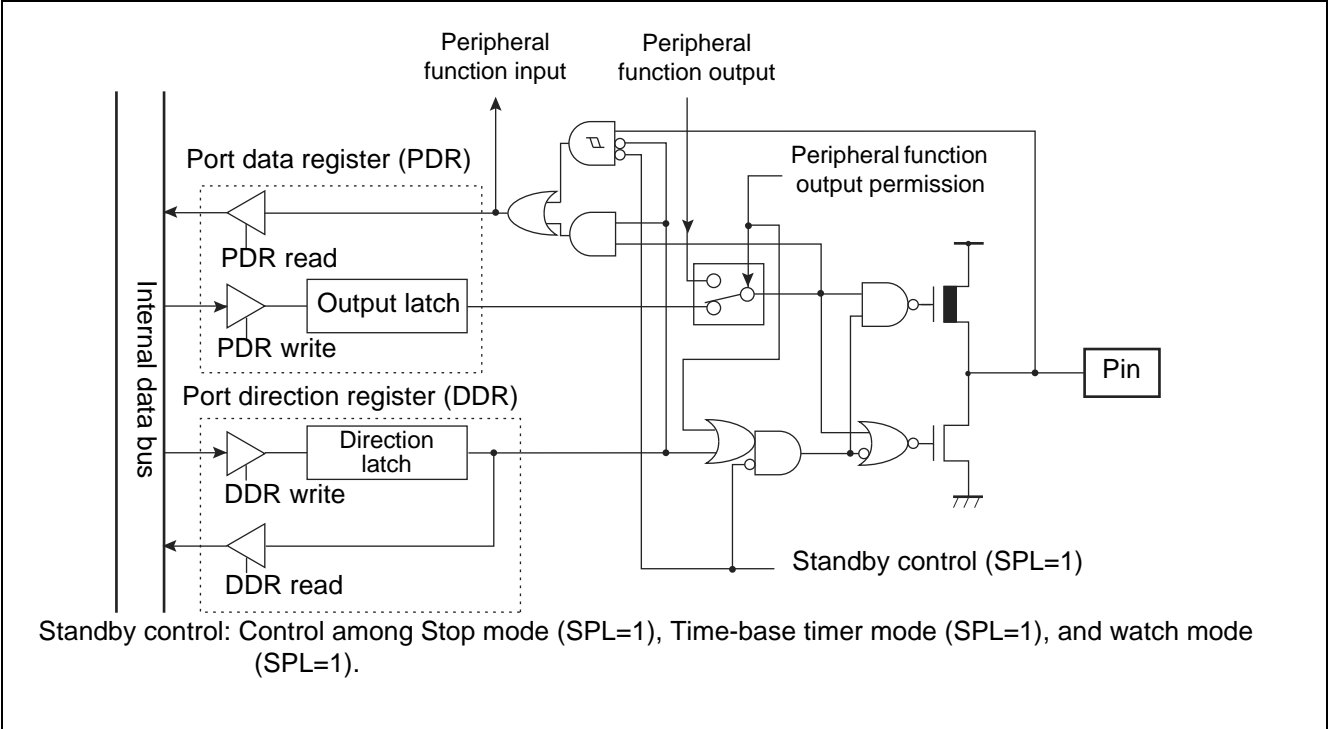
9.2 Memory Map

(with ROM mirroring
function enabled)

Address #1

Peripheral

RAM area

Register

Extension IO
area

ROM area
(FF bank image)

ROM area*

ROM area

Model	Address #1
	001900_H
	000900_H
	000900_H

☐ : Internal access memory

☒ : Access disallowed

*: On MB90387/S or MB90F387/S, to read "$FE0000_H$" to "$FEFFFF_H$" is to read out
"$FF0000_H$" to "$FFFFFF_H$".

Note: When internal ROM is operating, F²MC-16LX allows viewing ROM data image on FF bank at upper-level of 00 bank. This function is called "mirroring ROM," which allows effective use of C compiler small model.

F²MC-16LX assigns the same low order 16-bit address to FF bank and 00 bank, which allows referencing table in ROM without specifying "far" using pointer.

For example, when accessing to "$00C000_H$", ROM data at "$FFC000_H$" is accessed actually. However, because ROM area of FF bank exceeds 48 Kbytes, viewing all areas is not possible on 00 bank image. Because ROM data of "$FF4000_H$" to "$FFFFFF_H$" is viewed on "004000_H" to "$00FFFF_H$" image, store a ROM data table in area "$FF4000_H$" to "$FFFFFF_H$."

Address	Register Abbreviation	Register	Read/Write	Resource	Initial Value
003910H	PRLL0	PPG0 reload register L	R/W	8/16-bit PPG timer	XXXXXXXXB
003911H	PRLH0	PPG0 reload register H	R/W		XXXXXXXXB
003912H	PRLL1	PPG1 reload register L	R/W		XXXXXXXXB
003913H	PRLH1	PPG1 reload register H	R/W		XXXXXXXXB
003914H	PRLL2	PPG2 reload register L	R/W		XXXXXXXXB
003915H	PRLH2	PPG2 reload register H	R/W		XXXXXXXXB
003916H	PRLL3	PPG3 reload register L	R/W		XXXXXXXXB
003917H	PRLH3	PPG3 reload register H	R/W		XXXXXXXXB
003918H to 00392FH		(Reserved area) *			
003930H to 003BFFH		(Reserved area) *			
003C00H to 003C0FH		RAM (General-purpose RAM)			
003C10H to 003C13H	IDR0	ID register 0	R/W	CAN controller	XXXXXXXXB to XXXXXXXXB
003C14H to 003C17H	IDR1	ID register 1	R/W		XXXXXXXXB to XXXXXXXXB
003C18H to 003C1BH	IDR2	ID register 2	R/W		XXXXXXXXB to XXXXXXXXB
003C1CH to 003C1FH	IDR3	ID register 3	R/W		XXXXXXXXB to XXXXXXXXB
003C20H to 003C23H	IDR4	ID register 4	R/W		XXXXXXXXB to XXXXXXXXB
003C24H to 003C27H	IDR5	ID register 5	R/W		XXXXXXXXB to XXXXXXXXB
003C28H to 003C2BH	IDR6	ID register 6	R/W		XXXXXXXXB to XXXXXXXXB
003C2CH to 003C2FH	IDR7	ID register 7	R/W		XXXXXXXXB to XXXXXXXXB
003C30H, 003C31H	DLCR0	DLC register 0	R/W		XXXXXXXXB, XXXXXXXXB
003C32H, 003C33H	DLCR1	DLC register 1	R/W		XXXXXXXXB, XXXXXXXXB
003C34H, 003C35H	DLCR2	DLC register 2	R/W		XXXXXXXXB, XXXXXXXXB
003C36H, 003C37H	DLCR3	DLC register 3	R/W		XXXXXXXXB, XXXXXXXXB

Port 2 Pins Block Diagram (general-purpose input/output port)

Standby control: Control among Stop mode (SPL=1), Time-base timer mode (SPL=1), and watch mode (SPL=1).

Port 2 Registers

■ Port 2 registers include port 2 data register (PDR2) and port 2 direction register (DDR2).

■ The bits configuring the register correspond to port 2 pins on a one-to-one basis.

Relation between Port 2 Registers and Pins

Port Name	Bits of Register and Corresponding Pins								
Port 2	PDR2,DDR2	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	Corresponding pins	P27	P26	P25	P24	P23	P22	P21	P20

Port 4 Pins Block Diagram

Standby control: Control among Stop mode (SPL=1), Time-base timer mode (SPL=1), and watch mode (SPL=1).
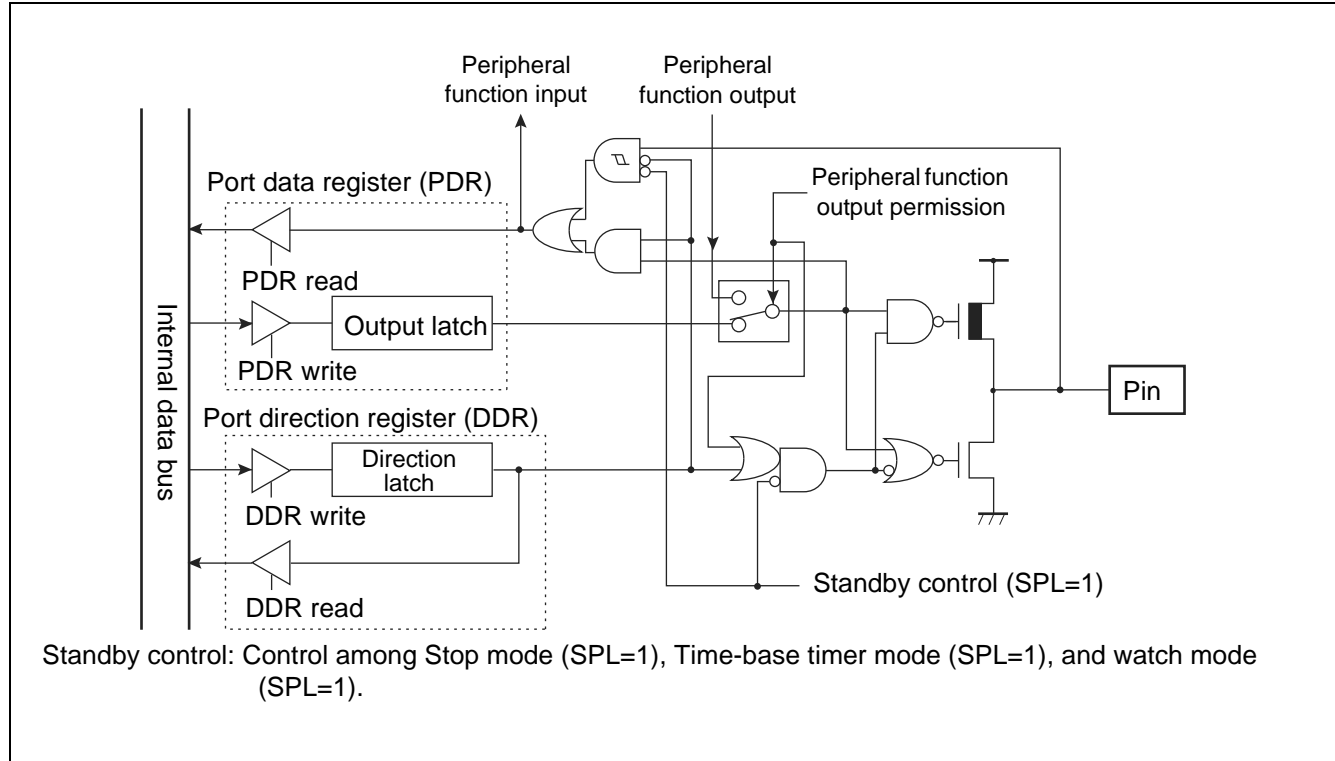
Port 4 Registers

■ Port 4 registers include port 4 data register (PDR4) and port 4 direction register (DDR4).

■ The bits configuring the register correspond to port 4 pins on a one-to-one basis.

Relation between Port 4 Registers and Pins

Port Name	Bits of Register and Corresponding Pins							
Port 4	PDR4, DDR4	–	–	–	bit4	bit3	bit2	bit1	bit0
	Corresponding pins	–	–	–	P44	P43	P42	P41	P40

12.2 Time-Base Timer

The time-base time is an 18-bit free-run counter (time-base timer counter) that counts up in synchronization with the main clock (dividing main oscillation clock by 2).

■ Four choices of interval time are selectable, and generation of interrupt request is allowed for each interval time.

■ Provides operation clock signal to oscillation stabilizing wait timer and peripheral functions.

Interval Timer Function

■ When the counter of time-base timer reaches an interval time specified by interval time selection bit (TBTC:TBC1, TBC0), an overflow (carrying-over) occurs (TBTC: TBOF=1) and interrupt request is generated.

■ If an interrupt by overflow is permitted (TBTC: TBIE=1), an interrupt is generated when overflow occurs (TBTC: TBOF=1).

■ The following four interval time settings are selectable:

Interval Time of Time-base Timer

Count Clock	Interval Time
2/HCLK (0.5 μs)	2^{12}/HCLK (Approx. 1.0 ms)
	2^{14}/HCLK (Approx. 4.1 ms)
	2^{16}/HCLK (Approx. 16.4 ms)
	2^{19}/HCLK (Approx. 131.1 ms)

HCLK: Oscillation clock

Values in parentheses "( )" are those under operation of 4-MHz oscillation clock.

12.3 Watchdog Timer

The watchdog timer is a 2-bit counter that uses time-base timer or watch timer as count clock. If the counter is not cleared within an interval time, CPU is reset.

Watchdog Timer Functions

■ The watchdog timer is a timer counter that prevents runaway of a program. Once a watchdog timer is activated, the counter of watchdog timer must always be cleared within a specified time of interval. If specified interval time elapses without clearing the counter of a watchdog timer, CPU resetting occurs. This is the function of a watchdog timer.

■ The interval time of a watchdog timer is determined by a clock cycle, which is input as a count clock. Watchdog resetting occurs between a minimum time and a maximum time specified.

■ The output target of a clock source is specified by the watchdog clock selection bit (WTC: WDCS) in the watch timer control register.

■ Interval time of a watchdog timer is specified by the time-base timer output selection bit / watch timer output selection bit (WDTC: WT1, WT0) in the watchdog timer control register.

Interval Timer of Watchdog Timer

Min	Max	Clock Cycle	Min	Max	Clock Cycle
Approx. 3.58 ms	Approx. 4.61 ms	$(2^{14}\pm2^{11})$ /HCLK	Approx. 0.457 s	Approx. 0.576 s	$(2^{12}\pm2^{9})$ /SCLK
Approx. 14.33 ms	Approx. 18.3 ms	$(2^{16}\pm2^{13})$ /HCLK	Approx. 3.584 s	Approx. 4.608 s	$(2^{15}\pm2^{12})$ /SCLK
Approx. 57.23 ms	Approx. 73.73 ms	$(2^{18}\pm2^{15})$ /HCLK	Approx. 7.168 s	Approx. 9.216 s	$(2^{16}\pm2^{13})$ /SCLK
Approx. 458.75 ms	Approx. 589.82 ms	$(2^{21}\pm2^{18})$ /HCLK	Approx. 14.336 s	Approx. 18.432 s	$(2^{17}\pm2^{14})$ /SCLK

HCLK: Oscillation clock (4 MHz), CSCLK: Sub clock (8.192 kHz)

Notes:

■ If the time-base timer is cleared when watchdog timer count clock is used as time base timer output (carry-over signal), watchdog reset time may become longer.

■ When using the sub clock as machine clock, be sure to specify watchdog timer clock source selection bit (WDCS) in watch timer control register (WTC) at "0," selecting output of watch timer.
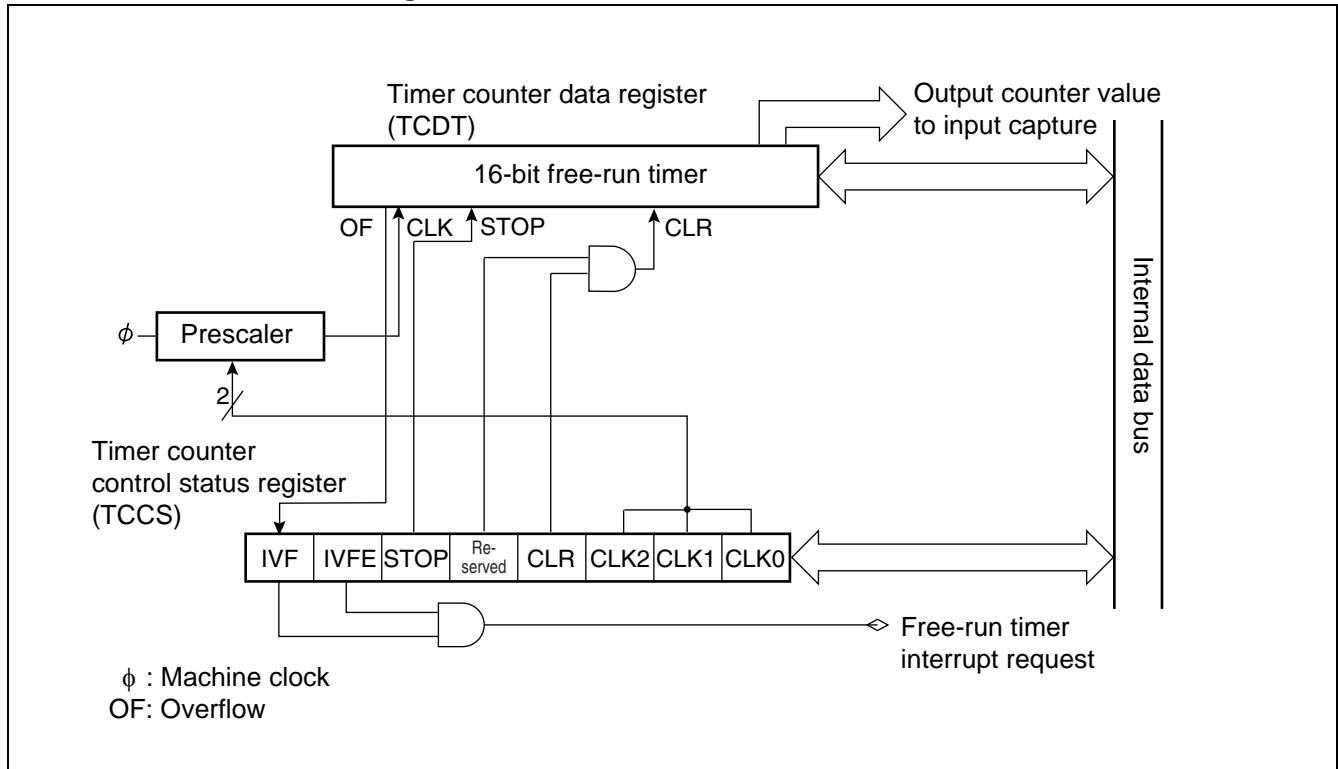
16-bit Free-run Timer

Counter value of 16-bit free-run timer is used as reference time (base time) of input capture.

Input Capture

Input capture detects rising edge, falling edge or both edges and retains a counter value of 16-bit free-run timer. Detection of edge on input signal is allowed to generate interrupt.

16-bit Free-run Timer Block Diagram

Detailed Pin Assignment on Block Diagram

The 16-bit input/output timer includes a 16-bit free-run timer. Interrupt request number of the 16-bit free-run timer is as follows:
Interrupt request number: 19 (13$_H$)

Prescaler

The prescaler divides a machine clock and provides a counter clock to the 16-bit up counter. Dividing ratio of the machine clock is specified by timer counter control status register (TCCS) among four values.

Timer Counter Data Register (TCDT)

The timer counter data register is a 16-bit up counter. A current counter value of the 16-bit free-run timer is read. Writing a value during halt of the counter allows setting an arbitrary counter value.

8/16-bit PPG Timer 0 Block Diagram

"H" level side data bus

"L" level side data bus

PPG0 reload register

PRLH0 ("H" level side)   PRLL0 ("L" level side)

PPG0 operation mode control register (PPGC0)

| PEN0 | — | PE0 | PIE0 | PUF0 | — | — | Re-served |

PPG0 temporary buffer 0(PRLBH0)

R
S   Q

Interrupt request output*

Select signal

Operation mode control signal

Reload register L/H selector

Count start value

Reload

PPG1 underflow
PPG0 underflow (To PPG1)

Pulse selector

Clear

PPG0 down counter (PCNT0)

Underflow

CLK

Re-versed

PPG0 output latch

Pin

PPG0

PPG output control circuit

Time-base timer output (512/HCLK)
Peripheral clock (1/φ)
Peripheral clock (2/φ)
Peripheral clock (4/φ)
Peripheral clock (8/φ)
Peripheral clock (16/φ)

Count clock selector

3

Select signal

| PCS2 | PCS1 | PCS0 | PCM2 | PCM1 | PCM0 | — | — |

PPG0/1 count clock selection register (PPG01)

− : Undefined
Reserved: Reserved bit
HCLK : Oscillation clock frequency
φ : Machine clock frequency
* : Interrupt output of 8/16-bit PPG timer 0 is incorporated into one by the OR circuit against interrupt output of 8/16-bit PPG timer 1.

12.9 DTP/External Interrupt and CAN Wakeup Outline

DTP/external interrupt transfers an interrupt request generated by an external peripheral device or a data transmission request to CPU, generating external interrupt request and activating expanded intelligent I/O service. Input RX of CAN controller is used as external interrupt input.

DTP/External Interrupt and CAN Wakeup Function

An interrupt request input from external peripheral device to external input pins (INT7 to INT4) and RX pin, just as interrupt request of peripheral device, generates an interrupt request. The interrupt request generates an external interrupt and activates expanded intelligent I/O service (EI^{2}OS).

If the expanded intelligent I/O service (EI^{2}OS) has been disabled by interrupt control register (ICR: ISE=0), external interrupt function is enabled and branches to interrupt processing.

If the EI^{2}OS has been enabled, (ICR: ISE=1), DTP function is enabled and automatic data transmission is performed by EI^{2}OS. After performing specified number of data transmission processes, the process branches to interrupt processing.

Table 12-2. DTP/External Interrupt and CAN Wakeup Outline

	External Interrupt	DTP Function
Input pin	5 pins (RX, and INT4 to INT7)	
Interrupt cause	Specify for each pin with detection level setting register (ELVR).	
	Input of "H" level/"L" level/rising edge/falling edge.	Input of "H" level/ "L" level
Interrupt number	#15 (0F$_H$), #24 (18$_H$), #27 (1B$_H$)	
Interrupt control	Enabling or disabling output of interrupt request, using DTP/external interrupt permission register (ENIR).	
Interrupt flag	Retaining interrupt cause with DTP/external interrupt cause register (EIRR).	
Process selection	Disable EI^{2}OS (ICR: ISE=0)	Enable EI^{2}OS (ICR: ISE=1)
Process	Branch to external interrupt process	After automatic data transmission by EI^{2}OS for specified number of times, branch to interrupt process.

12.11 UART Outline

UART is a general-purpose serial data communication interface for synchronous and asynchronous communication using external devices.

■ Provided with bi-directional communication function for both clock-synchronous and clock-asynchronous modes.

■ Provided with master/slave communication function (multi-processor mode). (Only master side is available.)

■ Interrupt request is generated upon completion of reception, completion of transmission and detection of reception error.

■ Ready for expanded intelligent service, EI^{2}OS.

Table 12-3. UART Functions

	Description
Data buffer	Full-duplex double buffer
Transmission mode	Clock synchronous (No start/stop bit, no parity bit) Clock asynchronous (start-stop synchronous)
Baud rate	Built-in special-purpose baud-rate generator. Setting is selectable among 8 values. Input of external values is allowed. Use of clock from external timer (16-bit reload timer 0) is allowed.
Data length	7 bits (only asynchronous normal mode) 8 bits
Signaling system	Non Return to Zero (NRZ) system
Reception error detection	Framing error Overrun error Parity error (not detectable in operation mode 1 (multi-processor mode))
Interrupt request	Receive interrupt (reception completed, reception error detected) Transmission interrupt (transmission completed) Ready for expanded intelligent I/O service (EI^{2}OS) in both transmission and reception
Master/slave communication function (asynchronous, multi-processor mode)	Communication between 1 (master) and n (slaves) are available (usable as master only).

Note: Start/stop bit is not added upon clock-synchronous transmission. Data only is transmitted.

Table 12-4. UART Operation Modes

| Operation Mode		Data Length		Synchronization	Stop Bit Length
		With Parity	Without Parity		
0	Asynchronous mode (normal mode)	7-bit or 8-bit		Asynchronous	1- bit or 2-bit *2
1	Multi processor mode	8+1*1	–	Asynchronous	
2	Synchronous mode	8	–	Synchronous	No

−: Disallowed

1: "+1" is an address/data selection bit used for communication control (bit 11 of SCR1 register: A/D).

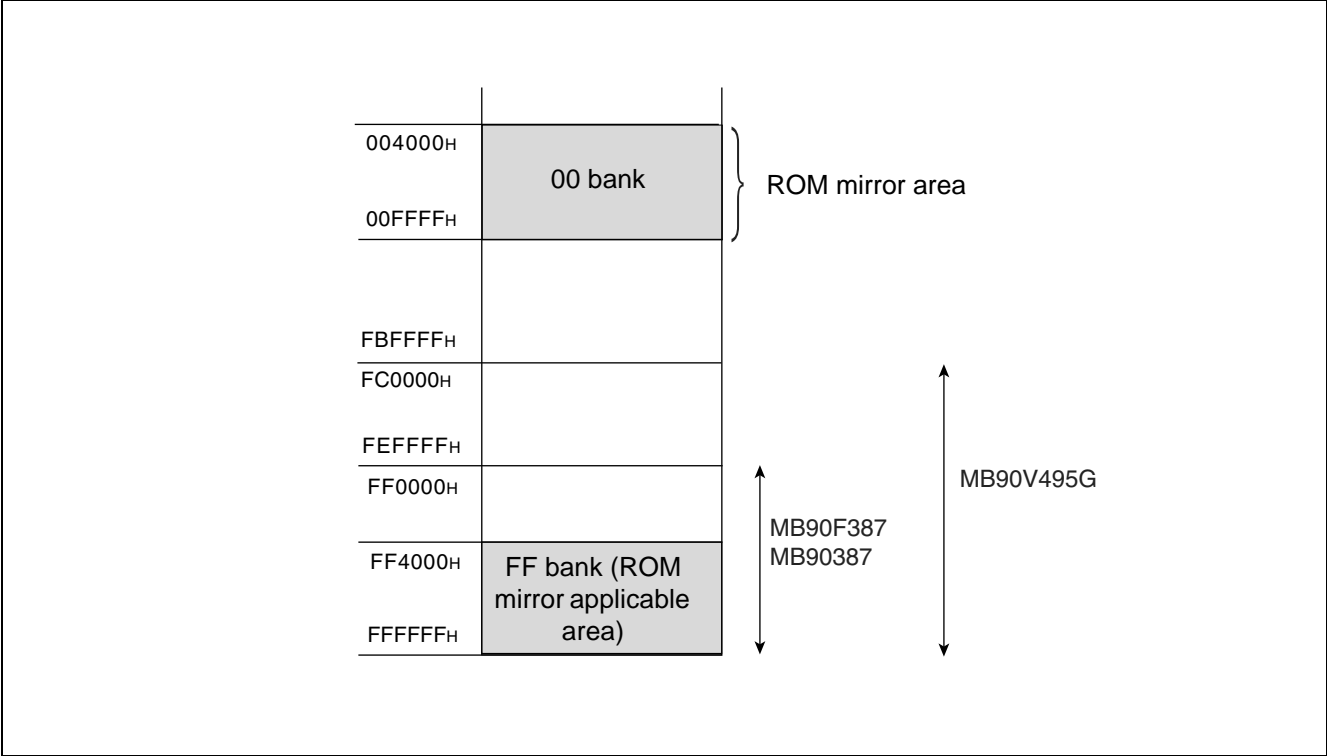2: Only 1 bit is detected as a stop bit on data reception.

12.14 ROM Mirror Function Selection Module Outline

The ROM mirror function selection module sets the data in ROM assigned to FF bank so that the data is read by access to 00 bank.

ROM Mirror Function Selection Module Block Diagram
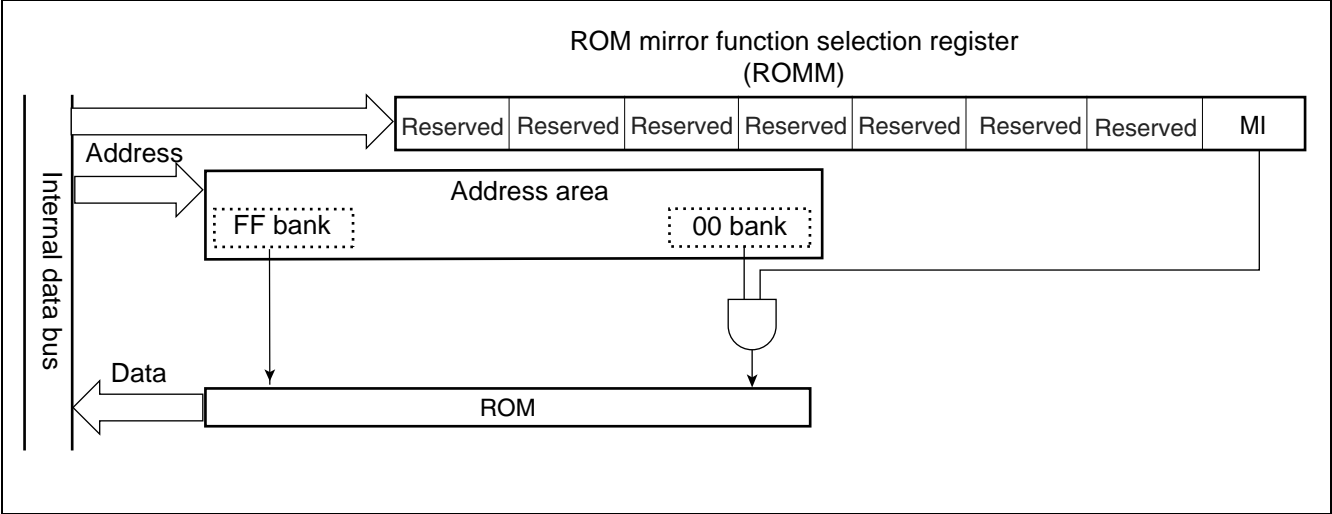
FF Bank Access by ROM Mirror Function

Sector Configuration of 512 Kbit Flash Memory

Flash memory	CPU address	Writer address*
SA0 (32 Kbytes)	FF0000H FF7FFFH	70000H 77FFFH
SA1 (8 Kbytes)	FF8000H FF9FFFH	78000H 79FFFH
SA2 (8 Kbytes)	FFA000H FFBFFFH	7A000H 7BFFFH
SA3 (16 Kbytes)	FFC000H FFFFFFH	7C000H 7FFFFH

*: "Writer address" is an address equivalent to CPU address, which is used when data is written on Flash memory, using parallel writer. When writing/ deleting data with general-purpose writer, the writer address is used for writing and deleting.
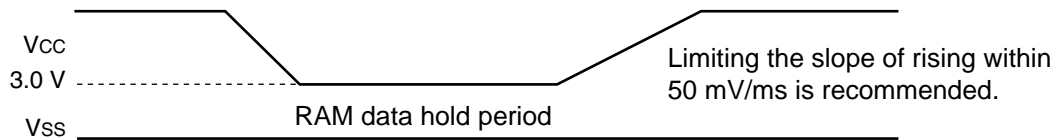
13.4.3 Power-on Reset

(Vcc = 5.0 V ± 10%, Vss = AVss = 0.0 V, Ta = −40 °C to +105 °C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Power supply rise time	t_R	Vcc	–	0.05	30	ms	
Power supply shutdown time	t_{OFF}	Vcc		1	–	ms	Waiting time until power-on
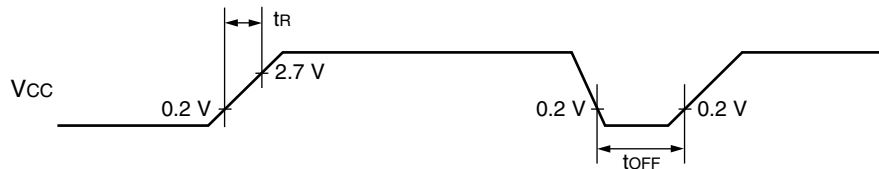
Sudden change of power supply voltage may activate the power-on reset function. When changing power supply voltages during operation, raise the power smoothly by suppressing variation of voltages as shown below. When raising the power, do not use PLL clock. However, if voltage drop is 1V/s or less, use of PLL clock is allowed during operation.

13.4.4 UART Timing

$(V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}, V_{SS} = 0.0 \text{ V}, T_A = -40\ ^\circ\text{C to } +105\ ^\circ\text{C})$

Parameter	Symbol	Pin Name	Conditions	Value Min	Value Max	Unit	Remarks
Serial clock cycle time	t_{SCYC}	SCK1	Internal shift clock mode output pin is: CL = 80 pF+1TTL.	4 t_{CP} *	–	ns	
SCK $\downarrow \rightarrow$ SOT delay time	t_{SLOV}	SCK1, SOT1		–80	+80	ns	
Valid SIN $\rightarrow$ SCK $\uparrow$	t_{IVSH}	SCK1, SIN1		100	–	ns	
SCK $\uparrow \rightarrow$ valid SIN hold time	t_{SHIX}	SCK1, SIN1		60	–	ns	
Serial clock "H" pulse width	t_{SHSL}	SCK1	External shift clock mode output pin is: CL = 80 pF+1TTL.	2 t_{CP} *	–	ns	
Serial clock "L" pulse width	t_{SLSH}	SCK1		2 t_{CP} *	–	ns	
SCK $\downarrow \rightarrow$ SOT delay time	t_{SLOV}	SCK1, SOT1		–	150	ns	
Valid SIN $\rightarrow$ SCK $\uparrow$	t_{IVSH}	SCK1, SIN1		60	–	ns	
SCK $\uparrow \rightarrow$ valid SIN hold time	t_{SHIX}	SCK1, SIN1		60	–	ns	

*: Refer to Clock Timing ratings for t_{CP} (internal operation clock cycle time).

Notes:

■ AC Characteristics in CLK synchronous mode.

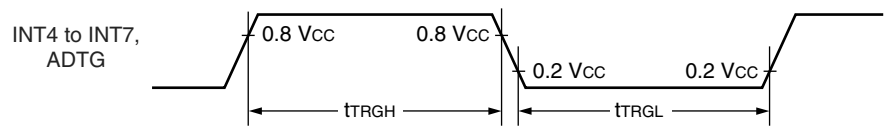■ C_L is a load capacitance value on pins for testing.

• Timer input timing

TIN0, TIN1,
IN0 to IN3

0.8 V$_{CC}$ 0.8 V$_{CC}$

0.2 V$_{CC}$ 0.2 V$_{CC}$

t$_{TIWH}$ t$_{TIWL}$
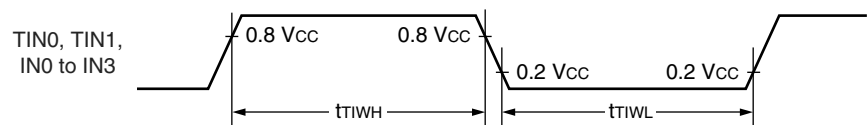
13.4.6 Trigger Input Timing

(V$_{CC}$ = 4.5 V to 5.5 V, V$_{SS}$ = 0.0 V, T$_A$ = −40 °C to +105 °C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t$_{TRGH}$ t$_{TRGL}$	INT4 to INT7, ADTG	–	5 t$_{CP}$ *	–	ns	

*: Refer to Clock Timing ratings for t$_{CP}$ (internal operation clock cycle time).

• Trigger input timing

INT4 to INT7,
ADTG

0.8 V$_{CC}$ 0.8 V$_{CC}$

0.2 V$_{CC}$ 0.2 V$_{CC}$

t$_{TRGH}$ t$_{TRGL}$

(Continued)

(Vcc - Voh) – Ioh

Ta = +25 °C, Vcc = 4.5 V

Vol – Iol

Ta = +25 °C, Vcc = 4.5 V

Vol (mV)

Iol (mA)

H level input voltage/ L level input voltage
Vin – Vcc

Ta = +25 °C

Vin (V)

Vih

Vil

Vcc (V)