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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	F ² MC-16LX
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, SCI, UART/USART
Peripherals	POR, WDT
Number of I/O	36
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90f387spmcr-ge2

Notes When Using No Sub Clock

- If an oscillator is not connected to X0A and X1A pin, apply pull-down resistor to X0A pin and leave X1A pin open.

About Power Supply Pins

- If two or more Vcc and Vss pins exist, the pins that should be at the same potential are connected to each other inside the device. For reducing unwanted emissions and preventing malfunction of strobe signals caused by increase of ground level, however, be sure to connect the Vcc and Vss pins to the power source and the ground externally.
- Pay attention to connect a power supply to Vcc and Vss of MB90385 series device in a lowest-possible impedance.
- Near pins of MB90385 series device, connecting a bypass capacitor is recommended at 0.1 μ F across Vcc pin and Vss pin.

Crystal Oscillator Circuit

- Noises around X0 and X1 pins cause malfunctions on a MB90385 series device. Design a print circuit so that X0 and X1 pins, an crystal oscillator (or a ceramic oscillator), and bypass capacitor to the ground become as close as possible to each other. Furthermore, avoid wires to X0 and X1 pins crossing each other as much as possible.
- Print circuit designing that surrounds X0 and X1 pins with grounding wires, which ensures stable operation, is strongly recommended.

Caution on Operations during PLL Clock Mode

- If the PLL clock mode is selected, the microcontroller attempt to be working with the self-oscillating circuit even when there is no external oscillator or external clock input is stopped. Performance of this operation, however, cannot be guaranteed.

Sequence of Turning on Power of A/D Converter and Applying Analog Input

- Be sure to turn on digital power (Vcc) before applying signals to the A/D converter and applying analog input signals (AN0 to AN7 pins).
- Be sure to turn off the power of A/D converter and analog input before turning off the digital power source.
- Be sure not to apply AVR exceeding AVcc when turning on and off. (No problems occur if analog and digital power is turned on and off simultaneously.)

Handling Pins When A/D Converter is Not Used

- If the A/D converter is not used, connect the pins under the following conditions: "AVcc=AVR=Vcc," and "AVss=Vss"

Note on Turning on Power

- For preventing malfunctions on built-in step-down circuit, maintain a minimum of 50 μ s of voltage rising time (between 0.2 V and 2.7V) when turning on the power.

Stabilization of Supply Voltage

- A sudden change in the supply voltage may cause the device to malfunction even within the specified Vcc supply voltage operating range. Therefore, the Vcc supply voltage should be stabilized.
For reference, the supply voltage should be controlled so that Vcc ripple variations (peak-to-peak values) at commercial frequencies (50 Hz / 60 Hz) fall below 10% of the standard Vcc supply voltage and the coefficient of fluctuation does not exceed 0.1 V/ms at instantaneous power switching.

Address	Register Abbreviation	Register	Read/ Write	Resource	Initial Value
0000B0 _H	ICR00	Interrupt control register 00	R/W	Interrupt controller	00000111 _B
0000B1 _H	ICR01	Interrupt control register 01			00000111 _B
0000B2 _H	ICR02	Interrupt control register 02			00000111 _B
0000B3 _H	ICR03	Interrupt control register 03			00000111 _B
0000B4 _H	ICR04	Interrupt control register 04			00000111 _B
0000B5 _H	ICR05	Interrupt control register 05			00000111 _B
0000B6 _H	ICR06	Interrupt control register 06			00000111 _B
0000B7 _H	ICR07	Interrupt control register 07			00000111 _B
0000B8 _H	ICR08	Interrupt control register 08			00000111 _B
0000B9 _H	ICR09	Interrupt control register 09			00000111 _B
0000BA _H	ICR10	Interrupt control register 10			00000111 _B
0000BB _H	ICR11	Interrupt control register 11			00000111 _B
0000BC _H	ICR12	Interrupt control register 12			00000111 _B
0000BD _H	ICR13	Interrupt control register 13			00000111 _B
0000BE _H	ICR14	Interrupt control register 14			00000111 _B
0000BF _H	ICR15	Interrupt control register 15			00000111 _B
0000C0 _H to 0000FF _H	(Reserved area) *				
001FF0 _H	PADR0	Detection address setting register 0 (low-order)	R/W	Address matching detection function	XXXXXXXX _B
001FF1 _H		Detection address setting register 0 (middle-order)			XXXXXXXX _B
001FF2 _H		Detection address setting register 0 (high-order)			XXXXXXXX _B
001FF3 _H	PADR1	Detection address setting register 1 (low-order)	R/W		XXXXXXXX _B
001FF4 _H		Detection address setting register 1 (middle-order)			XXXXXXXX _B
001FF5 _H		Detection address setting register 1 (high-order)			XXXXXXXX _B
003900 _H	TMR0/ TMRLR0	16-bit timer register 0/16-bit reload register	R,W	16-bit reload timer 0	XXXXXXXX _B
003901 _H					XXXXXXXX _B
003902 _H	TMR1/ TMRLR1	16-bit timer register 1/16-bit reload register	R,W	16-bit reload timer 1	XXXXXXXX _B
003903 _H					XXXXXXXX _B
003904 _H to 00390F _H	(Reserved area) *				

Address	Register Abbreviation	Register	Read/ Write	Resource	Initial Value
003D0D _H	(Reserved area) *				
003D0E _H	TIER	Send completion interrupt permission register	R/W	CAN controller	00000000 _B
003D0F _H	(Reserved area) *				
003D10 _H , 003D11 _H	AMSR	Acceptance mask selection register	R/W	CAN controller	XXXXXXXX _B , XXXXXXXX _B
003D12 _H , 003D13 _H	(Reserved area) *				
003D14 _H to 003D17 _H	AMR0	Acceptance mask register 0	R/W	CAN controller	XXXXXXXX _B to XXXXXXXX _B
003D18 _H to 003D1B _H	AMR1	Acceptance mask register 1	R/W		XXXXXXXX _B to XXXXXXXX _B
003D1C _H to 003DFF _H	(Reserved area) *				
003E00 _H to 003EFF _H	(Reserved area) *				
003FF0 _H to 003FFF _H	(Reserved area) *				

Initial values:

0: Initial value of this bit is "0."

1: Initial value of this bit is "1."

X: Initial value of this bit is undefined.

*: "Reserved area" should not be written anything. Result of reading from "Reserved area" is undefined.

Interrupt Source	EI ² OS Readiness	Interrupt Vector		Interrupt Control Register		Priority* ³
		Number	Address	ICR	Address	
UART1 reception completed	◎	#37	25 _H	FFFF68 _H	ICR13	High ↑
UART1 transmission completed	△	#38	26 _H	FFFF64 _H		
Reserved	×	#39	27 _H	FFFF60 _H	ICR14	
Reserved	×	#40	28 _H	FFFF5C _H		
Flash memory	×	#41	29 _H	FFFF58 _H	ICR15	↓ Low
Delay interrupt generation module	×	#42	2A _H	FFFF54 _H		

○ : Available

× : Unavailable

◎ : Available EI²OS function is provided.

△: Available when a cause of interrupt sharing a same ICR is not used.

- *1:
- Peripheral functions sharing an ICR register have the same interrupt level.
 - If peripheral functions share an ICR register, only one function is available when using expanded intelligent I/O service.
 - If peripheral functions share an ICR register, a function using expanded intelligent I/O service does not allow interrupt by another function.

*2: Input capture 1 corresponds to EI²OS, however, PPG does not. When using EI²OS by input capture 1, interrupt should be disabled for PPG.

*3: Priority when two or more interrupts of a same level occur simultaneously.

12. Peripheral Resources

12.1 I/O Ports

The I/O ports are used as general-purpose input/output ports (parallel I/O ports). The MB60385 series model is provided with 5 ports (34 inputs). The ports function as input/output pins for peripheral functions also.

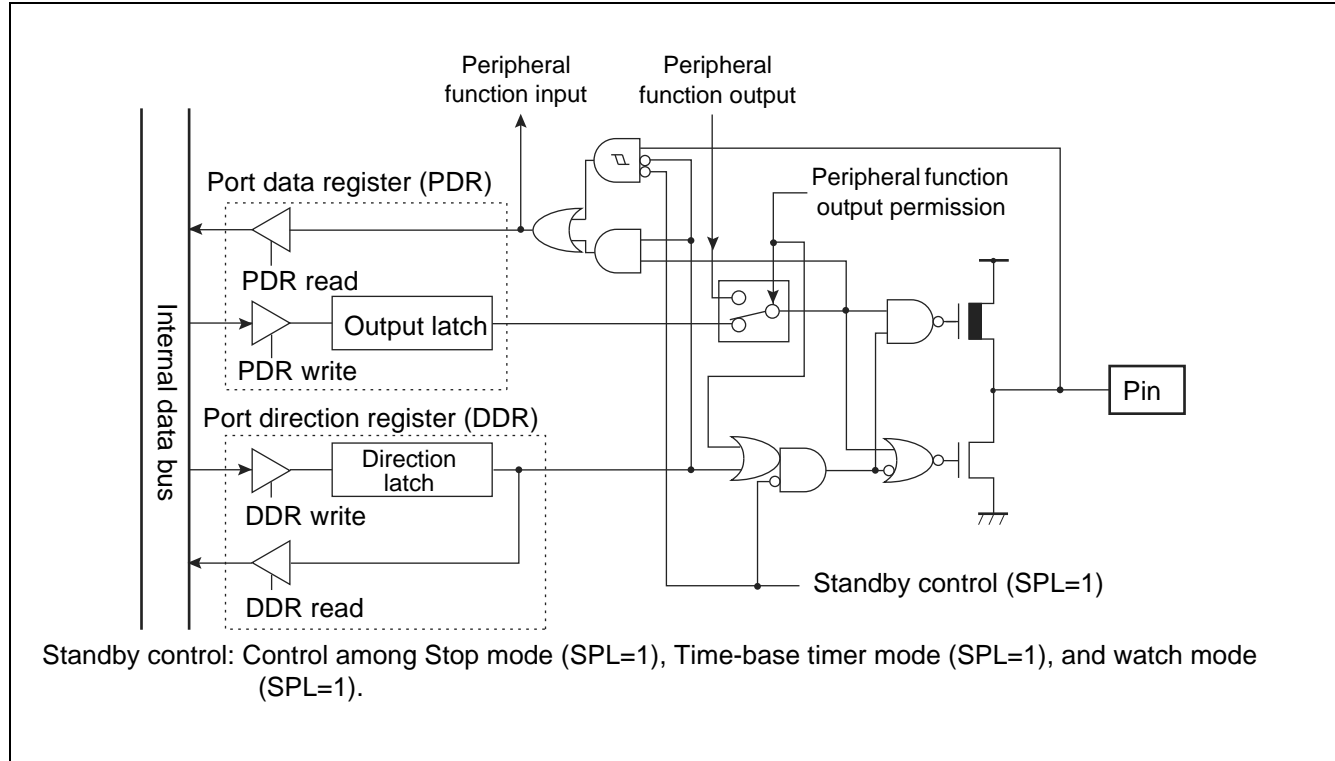
I/O Port Functions

An I/O port, using port data register (PDR), outputs the output data to I/O pin and input a signal input to I/O port. The port direction register (DDR) specifies direction of input/output of I/O pins on a bit-by-bit basis.

The following summarizes functions of the ports and sharing peripheral functions:

- Port 1: General-purpose input/output port, used also for PPG timer output and input capture inputs.
- Port 2: General-purpose input/output port, used also for reload timer input/output and external interrupt input.
- Port 3: General-purpose input/output port, used also for A/D converter activation trigger pin.
- Port 4: General-purpose input/output port, used also for UART input/output and CAN controller send/receive pin.
- Port 5: General-purpose input/output port, used also analog input pin.

Port 4 Pins Block Diagram



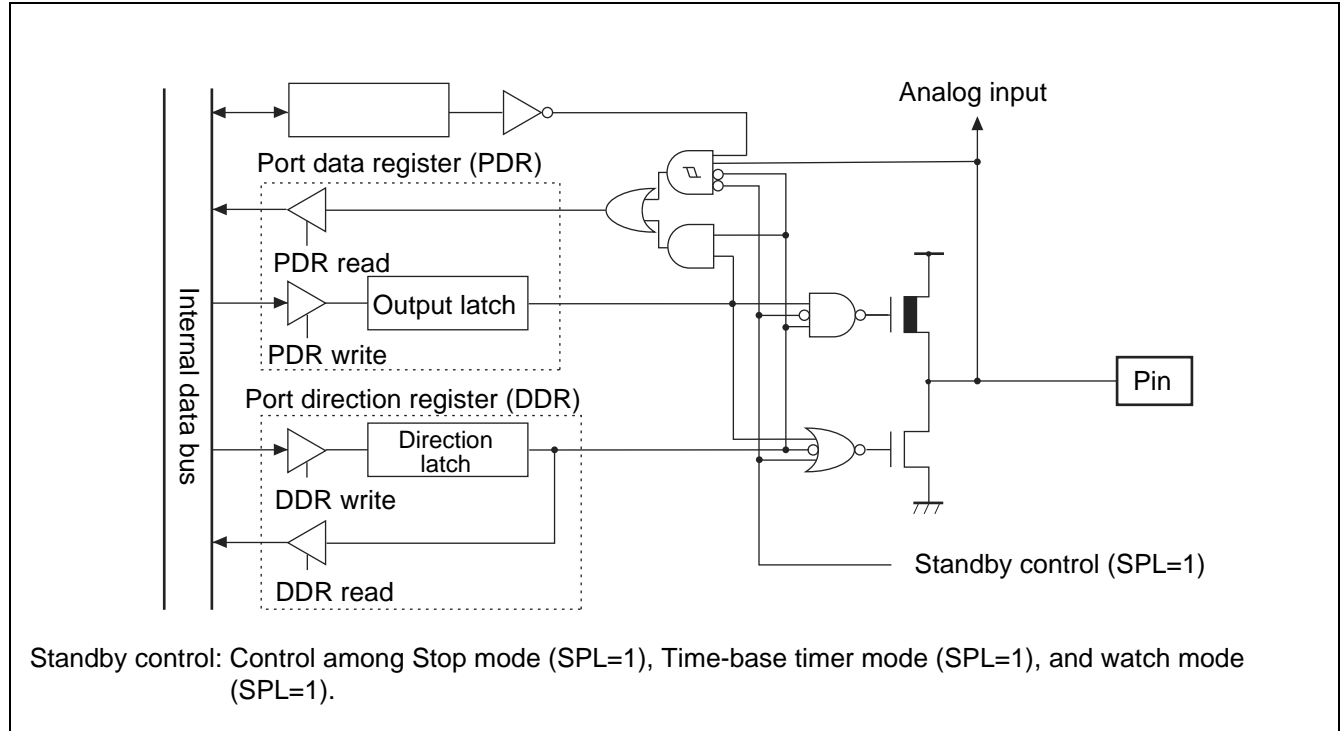
Port 4 Registers

- Port 4 registers include port 4 data register (PDR4) and port 4 direction register (DDR4).
- The bits configuring the register correspond to port 4 pins on a one-to-one basis.

Relation between Port 4 Registers and Pins

Port Name	Bits of Register and Corresponding Pins								
Port 4	PDR4, DDR4	—	—	—	bit4	bit3	bit2	bit1	bit0
	Corresponding pins	—	—	—	P44	P43	P42	P41	P40

Port 5 Pins Block Diagram



Port 5 Registers

- Port 5 registers include port 5 data register (PDR5), port 5 direction register (DDR5), and analog input permission register (ADER).
- Analog input permission register (ADER) allows or disallows input of analog signal to the analog input pin.
- The bits configuring the register correspond to port 5 pins on a one-to-one basis.

Relation between Port 5 Registers and Pins

Port Name	Bits of Register and Corresponding Pins								
Port 5	PDR5, DDR5	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	ADER	ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0
	Corresponding pins	P57	P56	P55	P54	P53	P52	P51	P50

12.2 Time-Base Timer

The time-base time is an 18-bit free-run counter (time-base timer counter) that counts up in synchronization with the main clock (dividing main oscillation clock by 2).

- Four choices of interval time are selectable, and generation of interrupt request is allowed for each interval time.
- Provides operation clock signal to oscillation stabilizing wait timer and peripheral functions.

Interval Timer Function

- When the counter of time-base timer reaches an interval time specified by interval time selection bit (TBTC:TBC1, TBC0), an overflow (carrying-over) occurs (TBTC: TBOF=1) and interrupt request is generated.
- If an interrupt by overflow is permitted (TBTC: TBIE=1), an interrupt is generated when overflow occurs (TBTC: TBOF=1).
- The following four interval time settings are selectable:

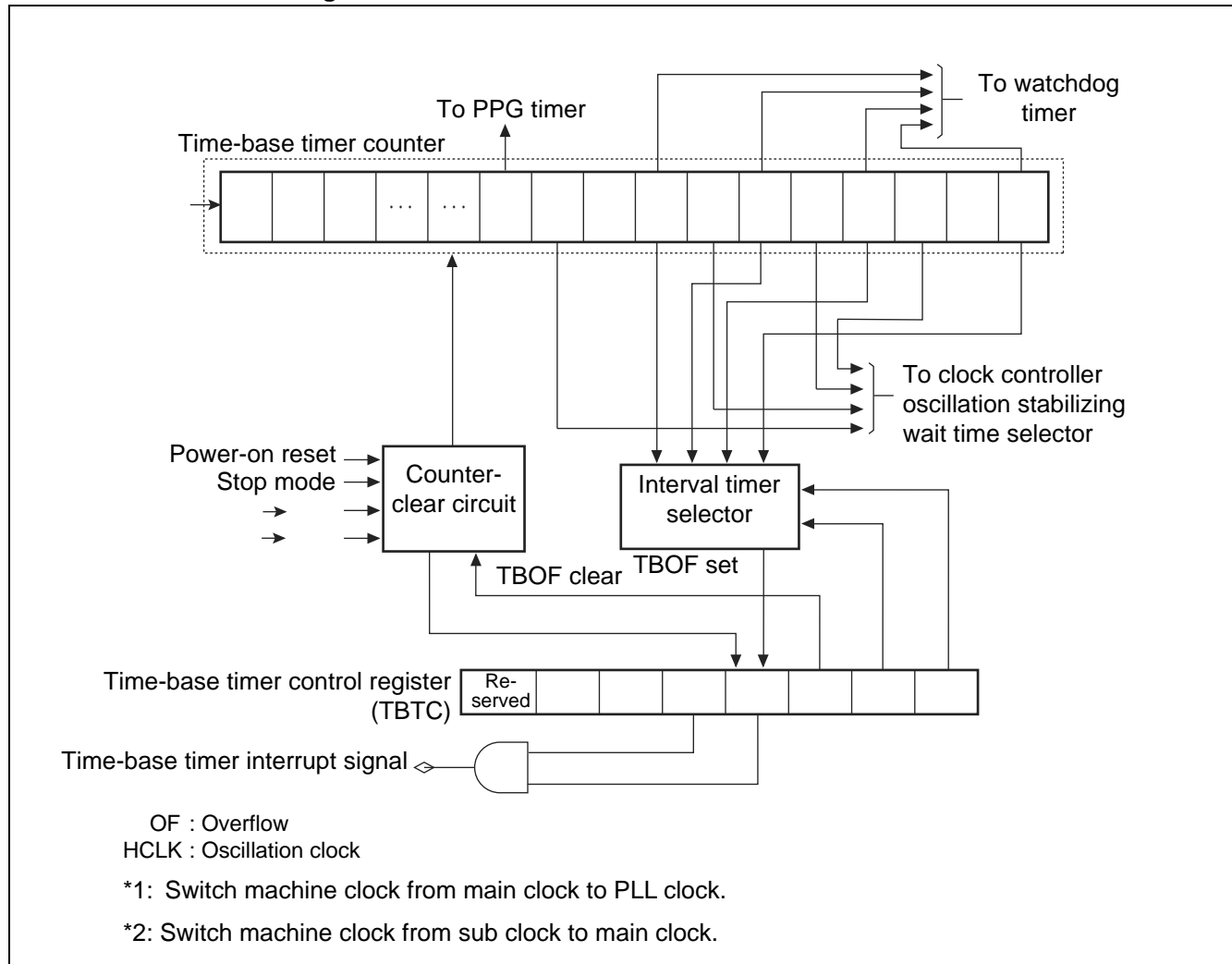
Interval Time of Time-base Timer

Count Clock	Interval Time
2/HCLK (0.5 μ s)	2^{12} /HCLK (Approx. 1.0 ms)
	2^{14} /HCLK (Approx. 4.1 ms)
	2^{16} /HCLK (Approx. 16.4 ms)
	2^{19} /HCLK (Approx. 131.1 ms)

HCLK: Oscillation clock

Values in parentheses “()” are those under operation of 4-MHz oscillation clock.

Time-base Timer Block Diagram



Actual interrupt request number of time-base timer is as follows:

Interrupt request number: #16 (10_H)

12.3 Watchdog Timer

The watchdog timer is a 2-bit counter that uses time-base timer or watch timer as count clock. If the counter is not cleared within an interval time, CPU is reset.

Watchdog Timer Functions

- The watchdog timer is a timer counter that prevents runaway of a program. Once a watchdog timer is activated, the counter of watchdog timer must always be cleared within a specified time of interval. If specified interval time elapses without clearing the counter of a watchdog timer, CPU resetting occurs. This is the function of a watchdog timer.
- The interval time of a watchdog timer is determined by a clock cycle, which is input as a count clock. Watchdog resetting occurs between a minimum time and a maximum time specified.
- The output target of a clock source is specified by the watchdog clock selection bit (WTC: WDSC) in the watch timer control register.
- Interval time of a watchdog timer is specified by the time-base timer output selection bit / watch timer output selection bit (WDTC: WT1, WT0) in the watchdog timer control register.

Interval Timer of Watchdog Timer

Min	Max	Clock Cycle	Min	Max	Clock Cycle
Approx. 3.58 ms	Approx. 4.61 ms	$(2^{14} \pm 2^{11})$ /HCLK	Approx. 0.457 s	Approx. 0.576 s	$(2^{12} \pm 2^9)$ /SCLK
Approx. 14.33 ms	Approx. 18.3 ms	$(2^{16} \pm 2^{13})$ /HCLK	Approx. 3.584 s	Approx. 4.608 s	$(2^{15} \pm 2^{12})$ /SCLK
Approx. 57.23 ms	Approx. 73.73 ms	$(2^{18} \pm 2^{15})$ /HCLK	Approx. 7.168 s	Approx. 9.216 s	$(2^{16} \pm 2^{13})$ /SCLK
Approx. 458.75 ms	Approx. 589.82 ms	$(2^{21} \pm 2^{18})$ /HCLK	Approx. 14.336 s	Approx. 18.432 s	$(2^{17} \pm 2^{14})$ /SCLK

HCLK: Oscillation clock (4 MHz), CSCLK: Sub clock (8.192 kHz)

Notes:

- If the time-base timer is cleared when watchdog timer count clock is used as time base timer output (carry-over signal), watchdog reset time may become longer.
- When using the sub clock as machine clock, be sure to specify watchdog timer clock source selection bit (WDSC) in watch timer control register (WTC) at "0," selecting output of watch timer.

12.7 8/16-bit PPG Timer Outline

The 8/16-bit PPG timer is a 2-channel reload timer module (PPG0 and PPG1) that allows outputting pulses of arbitrary cycle and duty cycle. Combination of the two channels allows selection among the following operations:

- 8-bit PPG output 2-channel independent operation mode
- 16-bit PPG output operation mode
- 8-bit and 8-bit PPG output operation mode

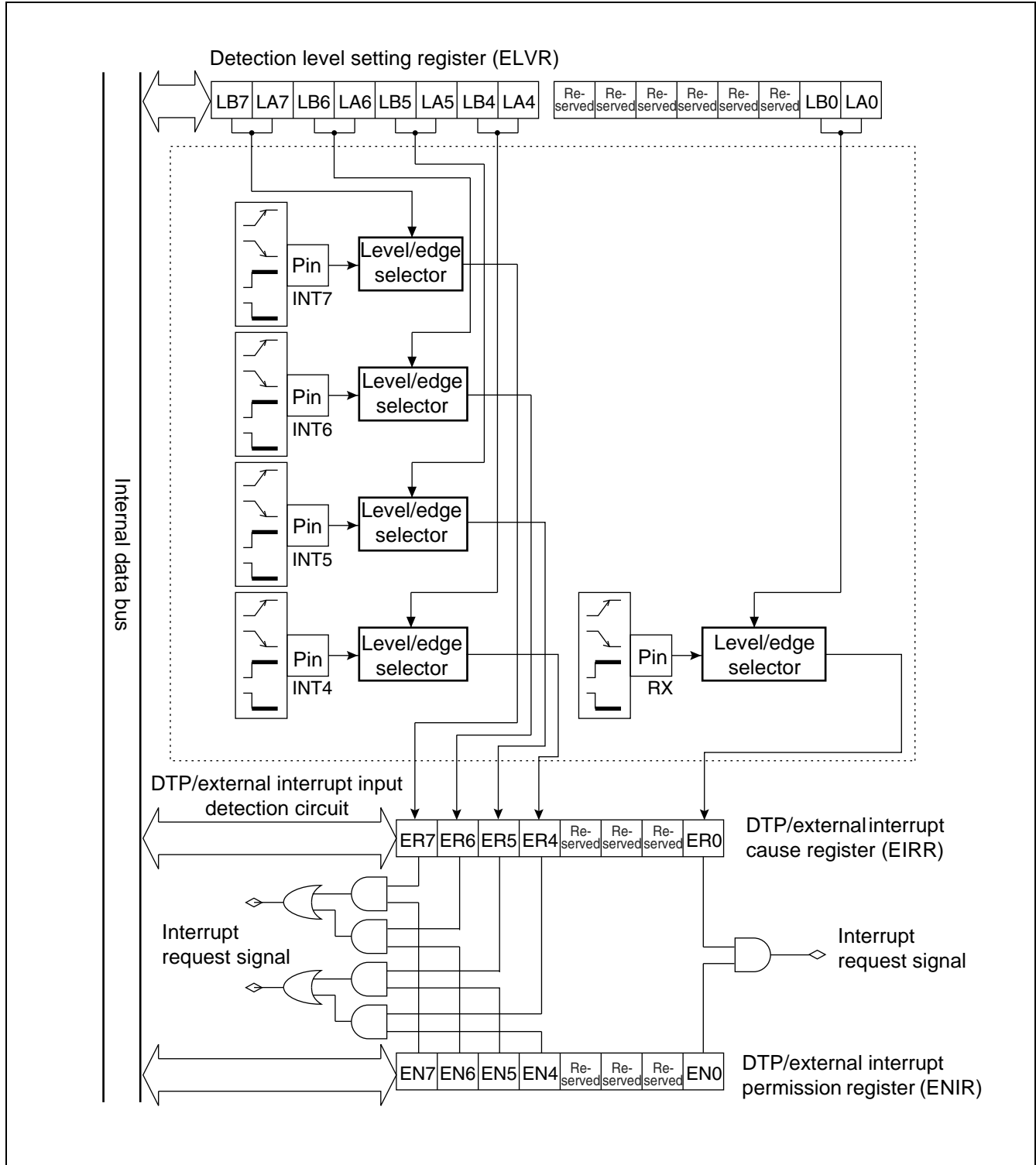
MB90385 series device has two 8/16-bit built-in PPG timers. This section describes functions of PPG0/1. PPG2/3 have the same functions as those of PPG0/1.

Functions of 8/16-bit PPG Timer

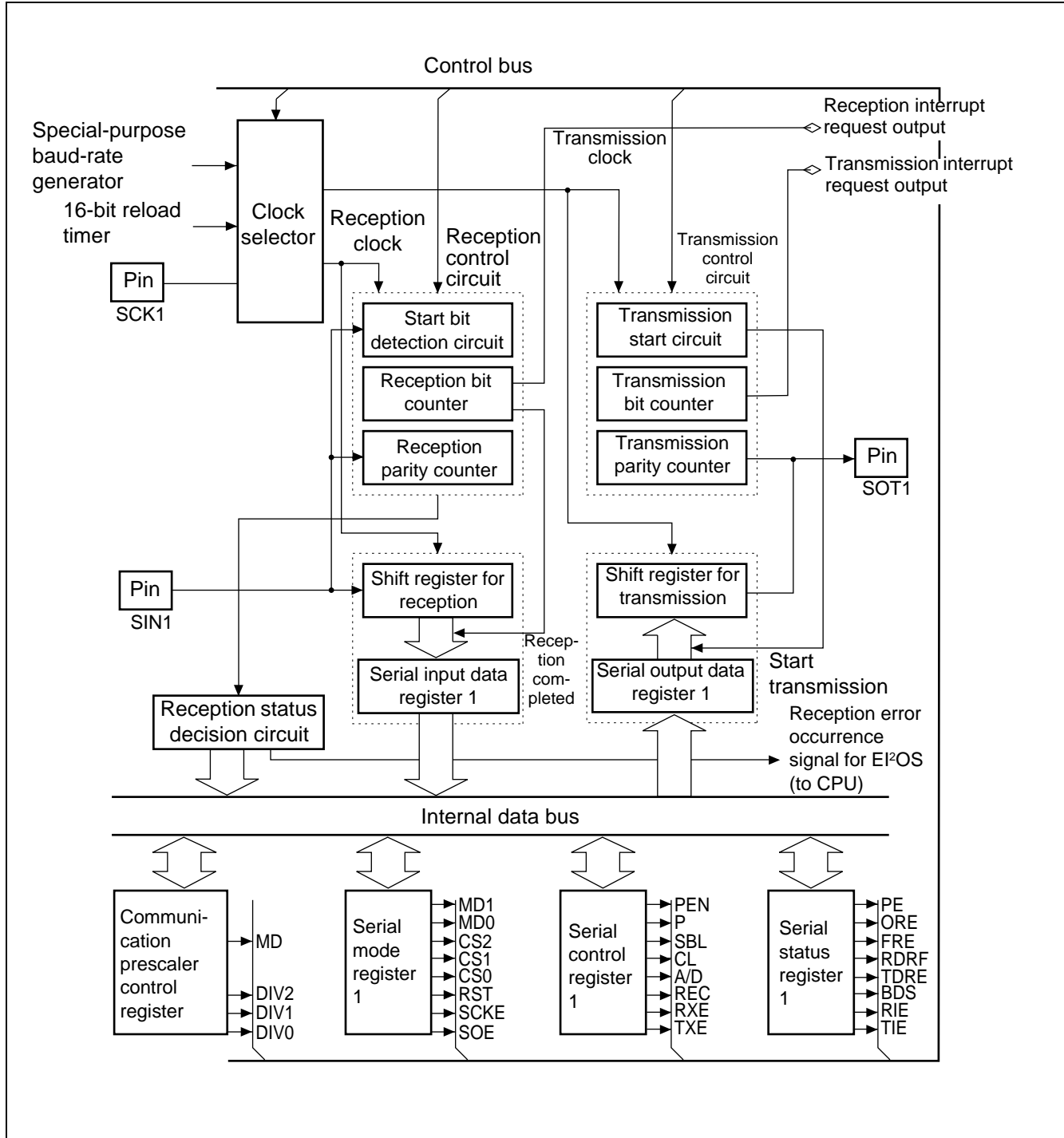
The 8/16-bit PPG timer is composed of four 8-bit reload register (PRLH0/PRLL0, PRLH1/PRLL1) and two PPG down counters (PCNT0, PCNT1).

- Widths of “H” and “L” in output pulse are specifiable independently. Cycle and duty factor of output pulse is specifiable arbitrarily.
- Count clock is selectable among 6 internal clocks.
- The timer is usable as an interval timer, by generating interrupt requests for each interval.
- The time is usable as a D/A converter, with an external circuit.

DTP/External Interrupt/CAN Wakeup Block Diagram



UART Block Diagram



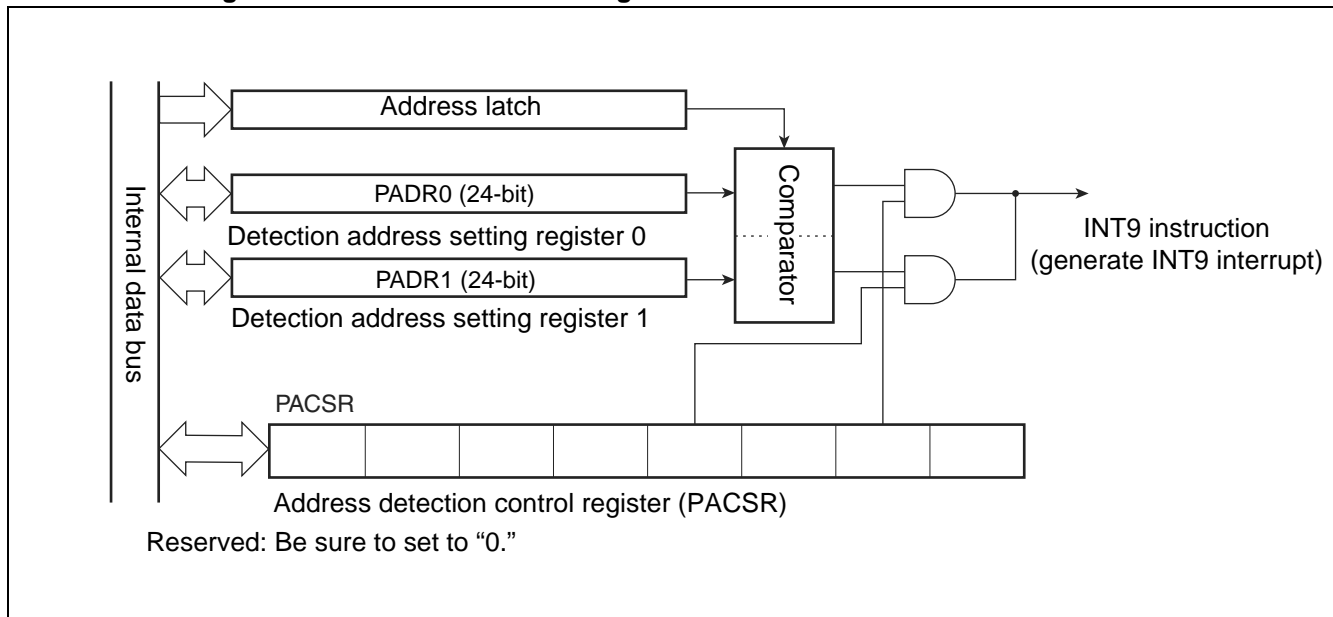
12.13 Address Matching Detection Function Outline

The address matching detection function checks if an address of an instruction to be processed next to a currently-processed instruction is identical with an address specified in the detection address register. If the addresses match with each other, an instruction to be processed next in program is forcibly replaced with INT9 instruction, and process branches to the interrupt process program. Using INT9 interrupt, this function is available for correcting program by batch processing.

Address Matching Detection Function Outline

- An address of an instruction to be processed next to a currently-processed instruction of the program is always retained in an address latch via internal data bus. By the address matching detection function, the address value retained in the address latch is always compared with an address specified in detection address setting register. If the compared address values match with each other, an instruction to be processed next by CPU is forcibly replaced with INT9 instruction, and an interrupt process program is executed.
- Two detection address setting registers are provided (PADR0 and PADR1), and each register is provided with interrupt permission bit. Generation of interrupt, which is caused by address matching between the address retained in address latch and the address specified in address setting register, is permitted and prohibited on a register-by-register basis.

Address Matching Detection Function Block Diagram



- Address latch
Retains address value output to internal data bus.
- Address detection control register (PACSR)
Specifies if interrupt is permitted or prohibited when addresses match with each other.
- Detection address setting (PADR0, PADR1)
Specifies addresses to be compared with values in address latch.

12.15 512 Kbit Flash Memory Outline

The following three methods are provided for data writing and deleting on Flash memory:

1. Parallel writer
2. Serial special-purpose writer
3. Writing/deleting by program execution

This section describes "3. Writing/deleting by program execution."

512 Kbit Flash Memory Outline

The 512 Kbit Flash memory is allocated on FF_H bank of CPU memory map. Using the function of Flash memory interface circuit, the memory allows read access and program access from CPU.

Writing/deleting on Flash memory is performed by instruction from CPU via Flash memory interface. Because rewriting is allowed on mounted memory, modifying program and data is performed efficiently.

Features of 512 Kbit Flash Memory

- 128 K words x 8 bits/64 K words x 16 bits (16 K + 8 K + 8 K + 32 K) sector configuration
- Automatic program algorithm (Embedded Algorithm: Similar to MBM29LV200.)
- Built-in deletion pause/deletion resume function
- Detection of completed writing/deleting by data polling and toggle bits.
- Detection of completed writing/deleting by CPU interrupt.
- Deletion is allowed on a sector-by-sector basis (sectors are combined freely).
- Number of writing/deleting operations (minimum): 10,000 times
- Sector protection
- Expanded sector protection
- Temporal sector unprotection

Note: A function of reading manufacture code and device code is not provided. These codes are not accessible by command either.

Flash Memory Writing/Deleting

- Writing and reading data is not allowed simultaneously on the Flash memory.
- Data writing and deleting on the Flash memory is performed by the processes as follows: Make a copy of program on Flash memory onto RAM. Then, execute the program copied on the RAM.

List of Registers and Reset Values in Flash Memory

Flash memory control status register (FMCS)		bit	7	6	5	4	3	2	1	0
			0	0	0	X	0	0	0	0
x : Undefined										

Sector Configuration

For access from CPU, SA0 to SA3 are allocated in FF bank register.

(V_{CC} = 5.0 V ±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = -40 °C to +105 °C)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current*	I _{CC} L	V _{CC}	V _{CC} = 5.0 V, Internally operating at 8 kHz, subclock operation, T _A = + 25°C	—	0.3	1.2	mA	MB90F387/S
	I _{CC} LS		V _{CC} = 5.0 V, Internally operating at 8 kHz, subclock, sleep mode, T _A = + 25°C	—	40	100	μA	MB90387/S
	I _{CC} T		V _{CC} = 5.0 V, Internally operating at 8 kHz, watch mode, T _A = + 25°C	—	8	25	μA	
	I _{CC} H		Stopping, T _A = + 25°C	—	5	20	μA	
Input capacity	C _{IN}	Other than AV _{CC} , AV _{SS} , AVR, C, V _{CC} , V _{SS}	—	—	5	15	pF	
Pull-up resistor	R _{UP}	RST	—	25	50	100	kΩ	
Pull-down resistor	R _{DOWN}	MD2	—	25	50	100	kΩ	Flash product is not provided with pull-down resistor.

*: Test conditions of power supply current are based on a device using external clock.

13.4 AC Characteristics

13.4.1 Clock Timing

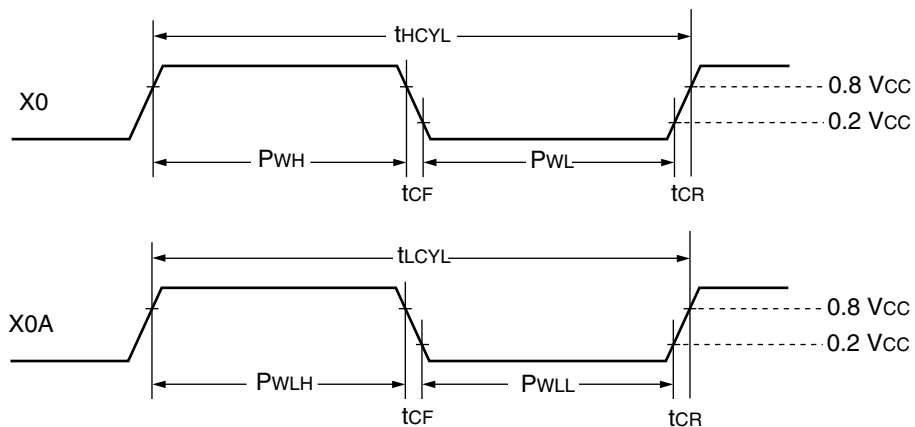
($V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C}$ to $+105\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_c	X0, X1	3	—	8	MHz	When crystal or ceramic resonator is used*2
			3	—	16	MHz	External clock input*1, *2
			4	—	16	MHz	PLL Multiply by 1 *2
			4	—	8	MHz	PLL Multiply by 2 *2
			4	—	5.33	MHz	PLL Multiply by 3 *2
			4	—	4	MHz	PLL Multiply by 4 *2
Clock cycle time	f_{CL}	X0A, X1A	—	32.768	—	kHz	
	t_{HCYL}	X0, X1	125	—	333	ns	
	t_{LCYL}	X0A, X1A	—	30.5	—	μs	
Input clock pulse width	P_{WH}, P_{WL}	X0	10	—	—	ns	Set duty factor at 30% to 70% as a guideline.
	P_{WLH}, P_{WLL}	X0A	—	15.2	—	μs	
Input clock rise time and fall time	t_{CR}, t_{CF}	X0	—	—	5	ns	When external clock is used
Internal operation clock frequency	f_{CP}	—	1.5	—	16	MHz	When main clock is used
	f_{LCP}	—	—	8.192	—	kHz	When sub clock is used
Internal operation clock cycle time	t_{CP}	—	62.5	—	666	ns	When main clock is used
	t_{LCP}	—	—	122.1	—	μs	When sub clock is used

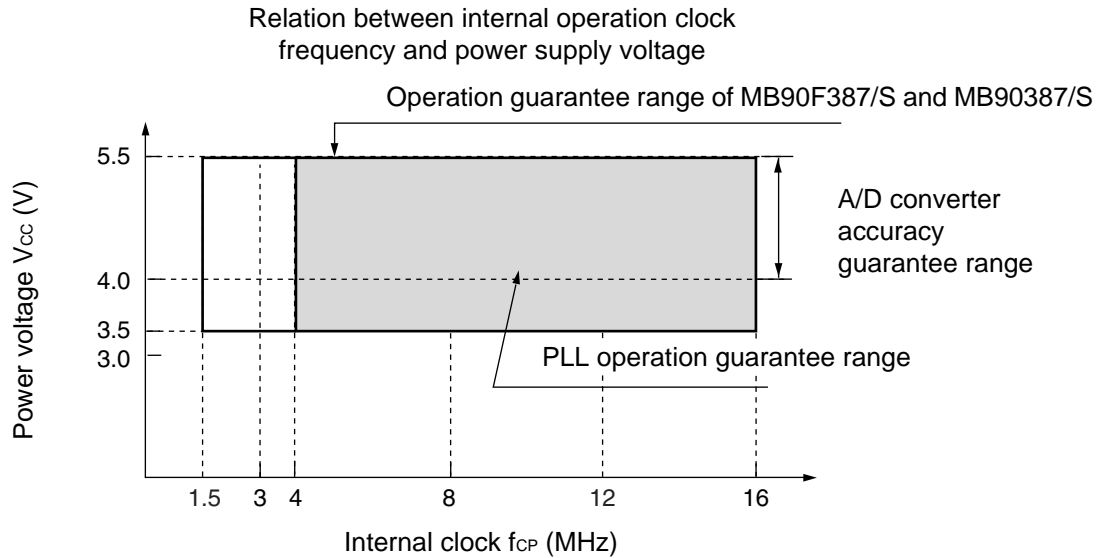
*1: Internal operation clock frequency should not exceed 16 MHz.

*2: When selecting the PLL clock, the range of clock frequency is limited. Use this product within range as mentioned in “Relation among external clock frequency and internal clock frequency”.

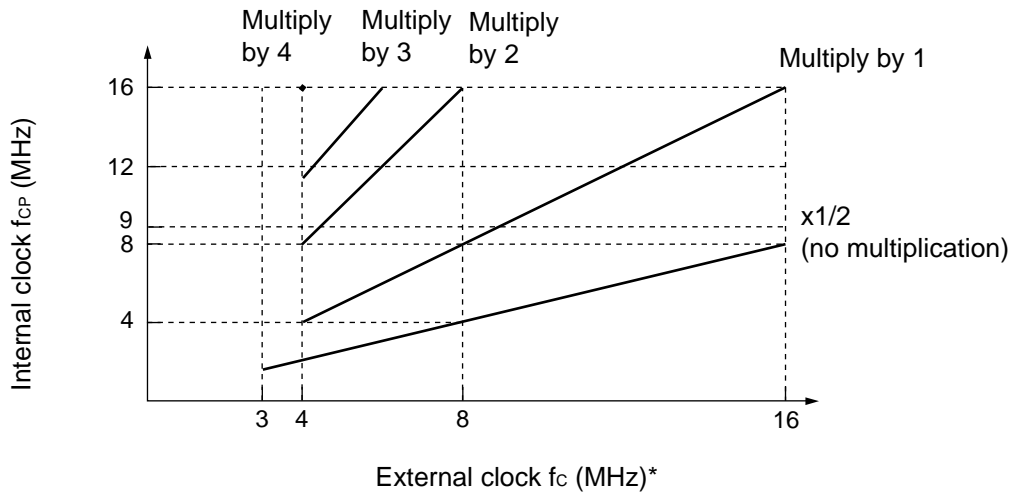
• Clock timing



• PLL operation guarantee range



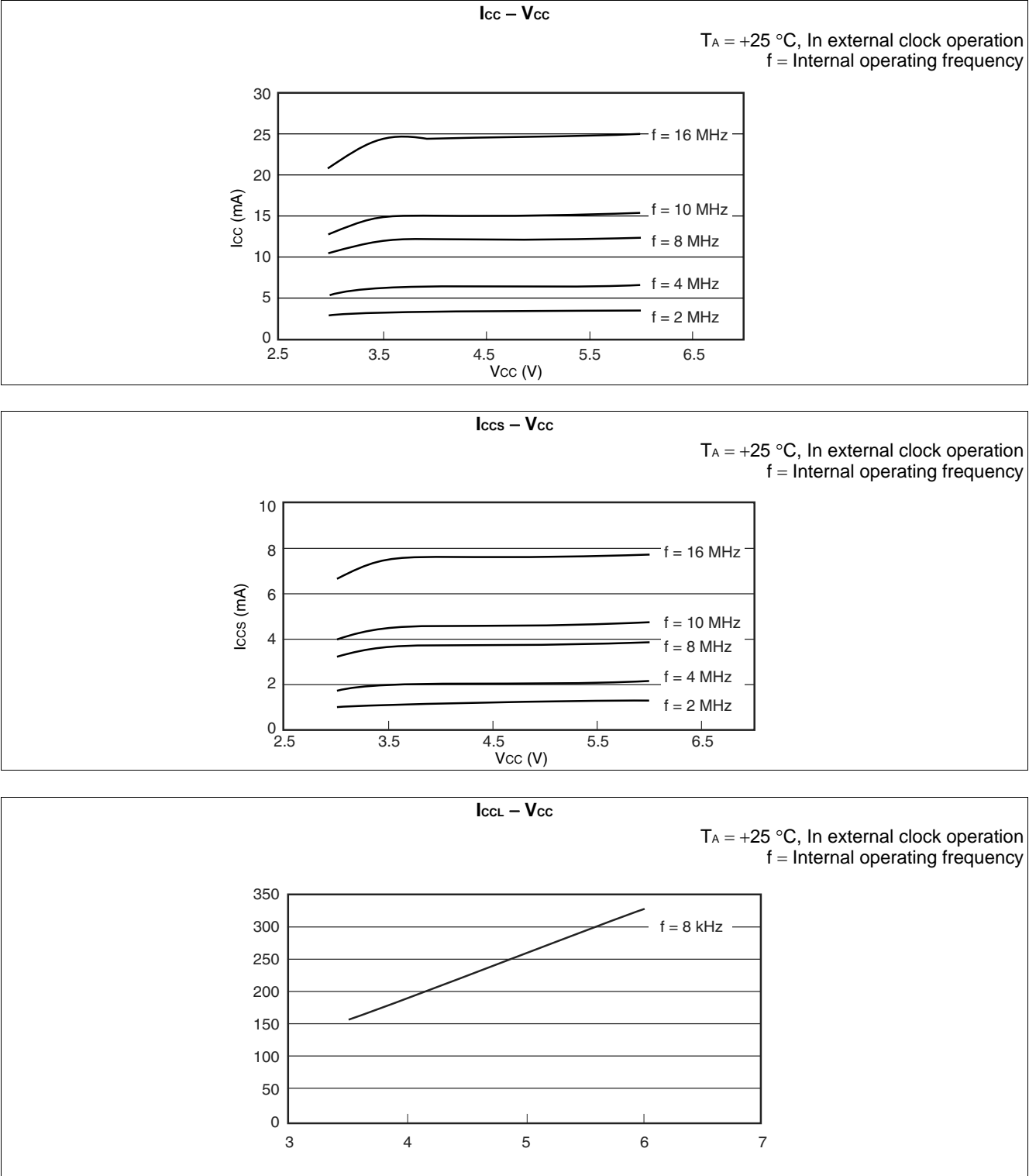
Relation among external clock frequency and internal clock frequency



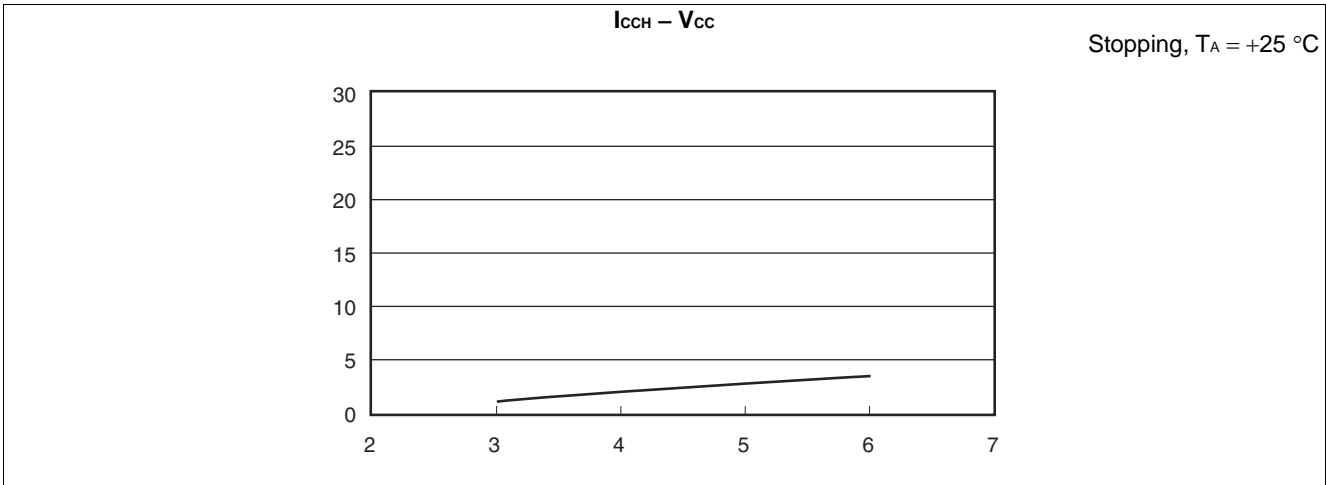
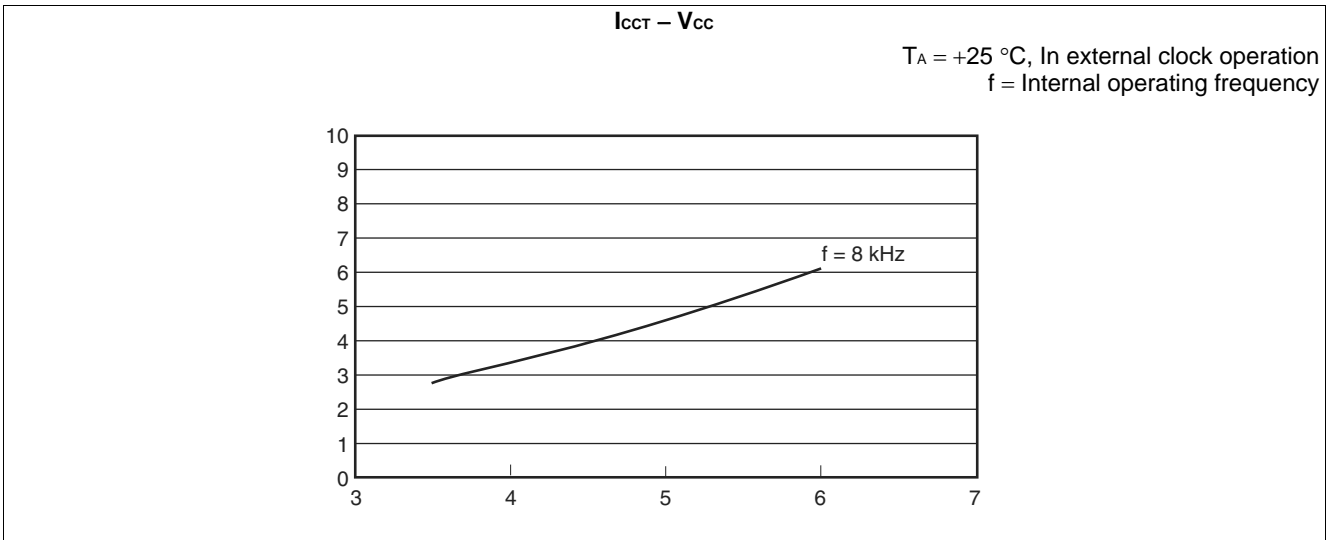
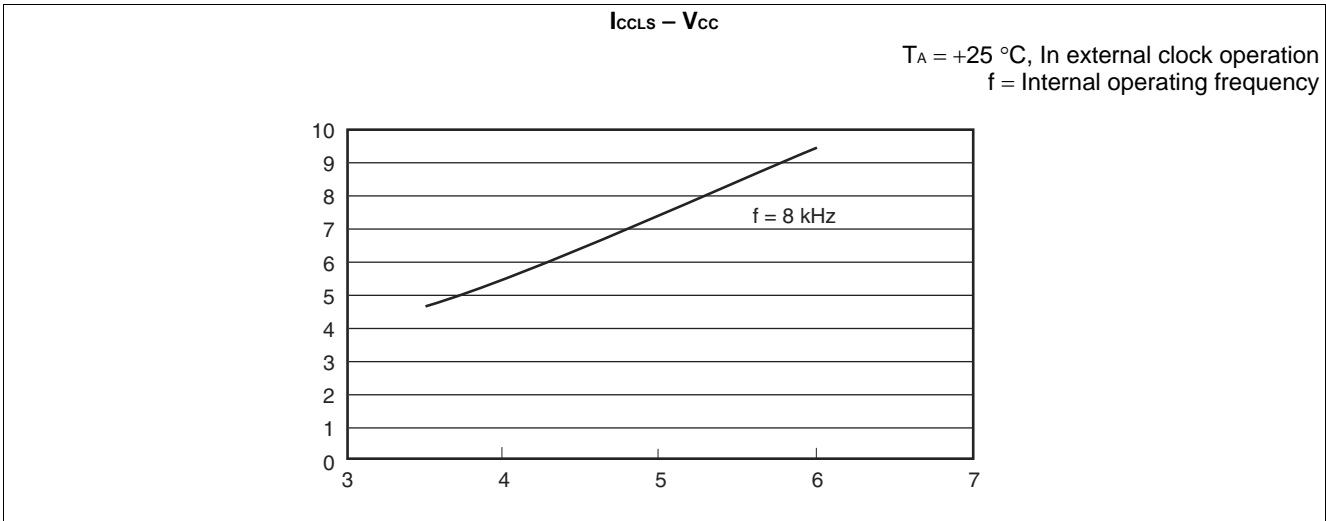
*: f_c is 8 MHz at maximum when crystal or ceramic resonator circuit is used.

14. Example Characteristics

MB90F387



(Continued)



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