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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	F <sup>2</sup> MC-16LX
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, SCI, UART/USART
Peripherals	POR, WDT
Number of I/O	36
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/infineon-technologies/mb90f387spmcr-gse2">https://www.e-xfl.com/product-detail/infineon-technologies/mb90f387spmcr-gse2</a>

## 16-bit Microcontrollers F<sup>2</sup>MC-16LX MB90385 Series

MB90385 series devices are general-purpose high-performance 16-bit micro controllers designed for process control of consumer products, which require high-speed real-time processing. The devices of this series have the built-in full-CAN interface.

The system, inheriting the architecture of F<sup>2</sup>MC family, employs additional instruction ready for high-level languages, expanded addressing mode, enhanced multiply-divide instructions, and enriched bit-processing instructions. Furthermore, employment of 32-bit accumulator achieves processing of long-word data (32 bits).

The peripheral resources of MB90385 series include the following:

8/10-bit A/D converter, UART (SCI), 8/16-bit PPG timer, 16-bit input-output timer (16-bit free-run timer, input capture 0, 1, 2, 3 (ICU)), and CAN controller.

### Features

#### Clock

- Built-in PLL clock frequency multiplication circuit
- Selection of machine clocks (PLL clocks) is allowed among frequency division by two on oscillation clock, and multiplication of 1 to 4 times of oscillation clock (for 4-MHz oscillation clock, 4 MHz to 16 MHz).
- Operation by sub-clock (8.192 kHz) is allowed. (MB90387, MB90F387)
- Minimum execution time of instruction: 62.5 ns (when operating with 4-MHz oscillation clock, and 4-time multiplied PLL clock).

#### 16 Mbyte CPU memory Space

- 24-bit internal addressing

#### Instruction System Best Suited to Controller

- Wide choice of data types (bit, byte, word, and long word)
- Wide choice of addressing modes (23 types)
- Enhanced multiply-divide instructions and RETI instructions
- Enhanced high-precision computing with 32-bit accumulator

#### Instruction System Compatible with High-level Language (C language) and Multitask

- Employing system stack pointer
- Enhanced various pointer indirect instructions
- Barrel shift instructions

#### Increased Processing Speed

- 4-byte instruction queue

#### Powerful Interrupt Function with 8 Levels and 34 Factors

#### Automatic Data Transfer Function Independent of CPU

- Expanded intelligent I/O service function (EI<sup>2</sup> OS): Maximum of 16 channels

#### Low Power Consumption (standby) Mode

- Sleep mode (a mode that halts CPU operating clock)

- Time-base timer mode (a mode that operates oscillation clock, sub clock, time-base timer and watch timer only)
- Watch mode (a mode that operates sub clock and watch timer only)
- Stop mode (a mode that stops oscillation clock and sub clock)
- CPU blocking operation mode

#### Process

- CMOS technology

#### I/O Port

- General-purpose input/output port (CMOS output):  
MB90387, MB90F387: 34 ports (including 4 high-current output ports)  
MB90387S, MB90F387S: 36 ports (including 4 high-current output ports)

#### Timer

- Time-base timer, watch timer, watchdog timer: 1 channel
- 8/16-bit PPG timer: 8-bit x 4 channels, or 16-bit x 2 channels
- 16-bit reload timer: 2 channels
- 16-bit input/output timer
  - 16-bit free run timer: 1 channel
  - 16-bit input capture: (ICU): 4 channelsInterrupt request is issued upon latching a count value of 16-bit free run timer by detection of an edge on pin input.

#### CAN Controller: 1 channel

- Compliant with Ver2.0A and Ver2.0B CAN specifications
- 8 built-in message buffers
- Transmission rate of 10 kbps to 1 Mbps (by 16 MHz machine clock)
- CAN wake-up

#### UART (SCI): 1 channel

- Equipped with full-duplex double buffer
- Clock-asynchronous or clock-synchronous serial transmission is available.

**DTP/External Interrupt: 4 channels, CAN wakeup:  
1 channel**

- Module for activation of expanded intelligent I/O service (EI<sup>2</sup>OS), and generation of external interrupt.

**Delay Interrupt Generator Module**

- Generates interrupt request for task switching.

**8/10-bit A/D Converter: 8 channels**

- Resolution is selectable between 8-bit and 10-bit.
- Activation by external trigger input is allowed.
- Conversion time: 6.125  $\mu$ s (at 16 MHz machine clock, including sampling time)

**Program Patch Function**

- Address matching detection for 2 address pointers.

## 1. Product Lineup

Part Number		MB90F387 MB90F387S	MB90387 MB90387S	MB90V495G
Parameter				
Classification		Flash ROM	Mask ROM	Evaluation product
ROM capacity		64 Kbytes		–
RAM capacity		2 Kbytes		6 Kbytes
Process		CMOS		
Package		LQFP-48 (pin pitch 0.50 mm)		PGA-256
Operating power supply voltage		3.5 V to 5.5 V		4.5 V to 5.5 V
Special power supply for emulator*1		–		None
CPU functions		Number of basic instructions : 351 instructions		
		Instruction bit length : 8 bits and 16 bits		
		Instruction length : 1 byte to 7 bytes		
		Data bit length : 1 bit, 8 bits, 16 bits		
		Minimum instruction execution time: 62.5 ns (at 16 MHz machine clock)		
		Interrupt processing time: 1.5 μs at minimum (at 16 MHz machine clock)		
Low power consumption (standby) mode		Sleep mode / Watch mode / Time-base timer mode / Stop mode / CPU intermittent		
I/O port		General-purpose input/output ports (CMOS output): 34 ports (36 ports*2) including 4 high-current output ports (P14 to P17)		
Time-base timer		18-bit free-run counter Interrupt cycle: 1.024 ms, 4.096 ms, 16.834 ms, 131.072 ms (with oscillation clock frequency at 4 MHz)		
Watchdog timer		Reset generation cycle: 3.58 ms, 14.33 ms, 57.23 ms, 458.75 ms (with oscillation clock frequency at 4 MHz)		
16-bit input/output timer	16-bit free-run timer	Number of channels: 1 Interrupt upon occurrence of overflow		
	Input capture	Number of channels: 4 Retaining free-run timer value set by pin input (rising edge, falling edge, and both edges)		
16-bit reload timer		Number of channels: 2 16-bit reload timer operation Count clock cycle: 0.25 μs, 0.5 μs, 2.0 μs (at 16-MHz machine clock frequency) External event count is allowed.		
Watch timer		15-bit free-run counter Interrupt cycle: 31.25 ms, 62.5 ms, 12 ms, 250 ms, 500 ms, 1.0 s, 2.0 s (with 8.192 kHz sub clock)		
8/16-bit PPG timer		Number of channels: 2 (four 8-bit channels are available also.) PPG operation is allowed with four 8-bit channels or two 16-bit channels. Outputting pulse wave of arbitrary cycle or arbitrary duty is allowed. Count clock: 62.5 ns to 1 μs (with 16 MHz machine clock)		
Delay interrupt generator module		Interrupt generator module for task switching. Used for realtime OS.		
DTP/External interrupt		Number of inputs: 4 Activated by rising edge, falling edge, "H" level or "L" level input. External interrupt or expanded intelligent I/O service (EI <sup>2</sup> OS) is available.		

Part Number Parameter	MB90F387 MB90F387S	MB90387 MB90387S	MB90V495G
8/10-bit A/D converter	Number of channels: 8 Resolution: Selectable 10-bit or 8-bit. Conversion time: 6.125 $\mu$ s (at 16 MHz machine clock, including sampling time) Sequential conversion of two or more successive channels is allowed. (Setting a maximum of 8 channels is allowed.) Single conversion mode: Selected channel is converted only once. Sequential conversion mode: Selected channel is converted repetitively. Halt conversion mode: Conversion of selected channel is stopped and activated alternately.		
UART(SCI)	Number of channels: 1 Clock-synchronous transfer: 62.5 kbps to 2 Mbps Clock-asynchronous transfer: 9,615 bps to 500 kbps Communication is allowed by bi-directional serial communication function and master/slave type connection.		
CAN	Compliant with Ver 2.0A and Ver 2.0B CAN specifications. 8 built-in message buffers. Transmission rate of 10 kbps to 1 Mbps (by 16 MHz machine clock) CAN wake-up		

\*1: Settings of DIP switch S2 for using emulation pod MB2145-507. For details, see MB2145-507 Hardware Manual (2.7 Power Pin solely for Emulator).

\*2: MB90387S, MB90F387S

## 2. Packages And Product Models

Package	MB90F387, MB90F387S	MB90387, MB90387S
LQA048	○	○

○ : Yes ×: No

Note: Refer to Package Dimension for details of the package.

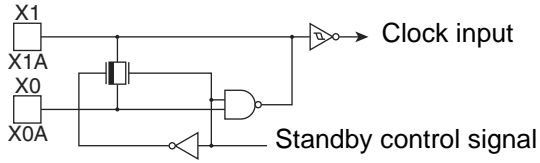
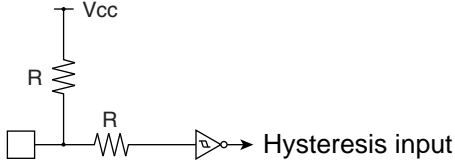
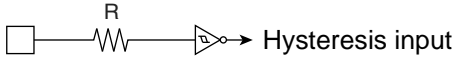
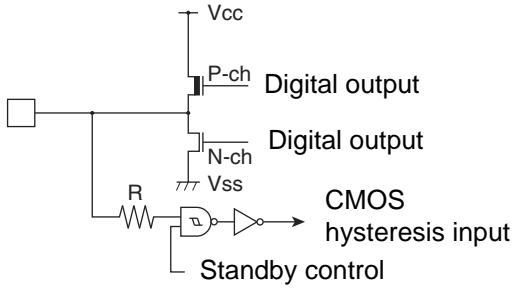
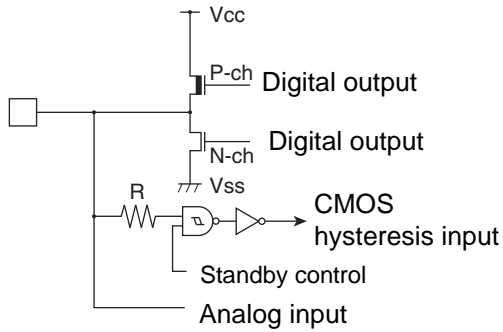
## 3. Product Comparison

### Memory Space

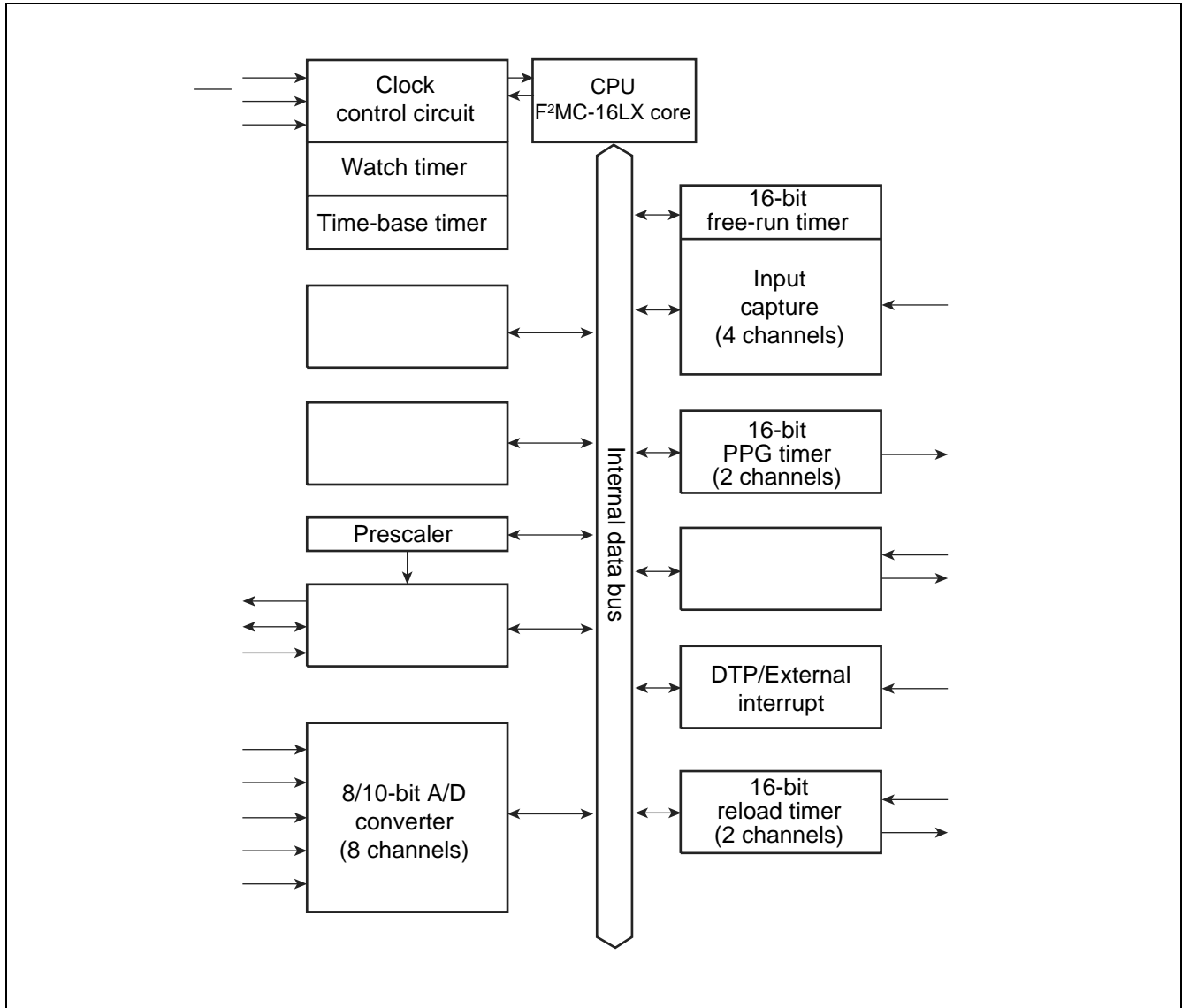
When testing with test product for evaluation, check the differences between the product and a product to be used actually. Pay attention to the following points:

- The MB90V495G has no built-in ROM. However, a special-purpose development tool allows the operations as those of one with built-in ROM. ROM capacity depends on settings on a development tool.
- On MB90V495G, an image from FF4000<sub>H</sub> to FFFFFFF<sub>H</sub> is viewed on 00 bank and an image of FE0000<sub>H</sub> to FF3FFF<sub>H</sub> is viewed only on FE bank and FF bank. (Modified on settings of a development tool.)
- On MB90F387/F387S/387/387S, an image from FF4000<sub>H</sub> to FFFFFFF<sub>H</sub> is viewed on 00 bank and an image of FE0000<sub>H</sub> to FF3FFF<sub>H</sub> is viewed only on FF bank.

## 6. I/O Circuit Type

Type	Circuit	Remarks
A		<ul style="list-style-type: none"> <li>■ High-rate oscillation feedback resistor, approx.1 MΩ</li> <li>■ Low-rate oscillation feedback resistor, approx.10 MΩ</li> </ul>
B		<ul style="list-style-type: none"> <li>■ Hysteresis input with pull-up resistor.</li> <li>■ Pull-up resistor, approx.50 kΩ</li> </ul>
C		<ul style="list-style-type: none"> <li>■ Hysteresis input</li> </ul>
D		<ul style="list-style-type: none"> <li>■ CMOS hysteresis input</li> <li>■ CMOS level output</li> <li>■ Standby control provided</li> </ul>
E		<ul style="list-style-type: none"> <li>■ CMOS hysteresis input</li> <li>■ CMOS level output</li> <li>■ Shared for analog input pin</li> <li>■ Standby control provided</li> </ul>

## 8. Block Diagram



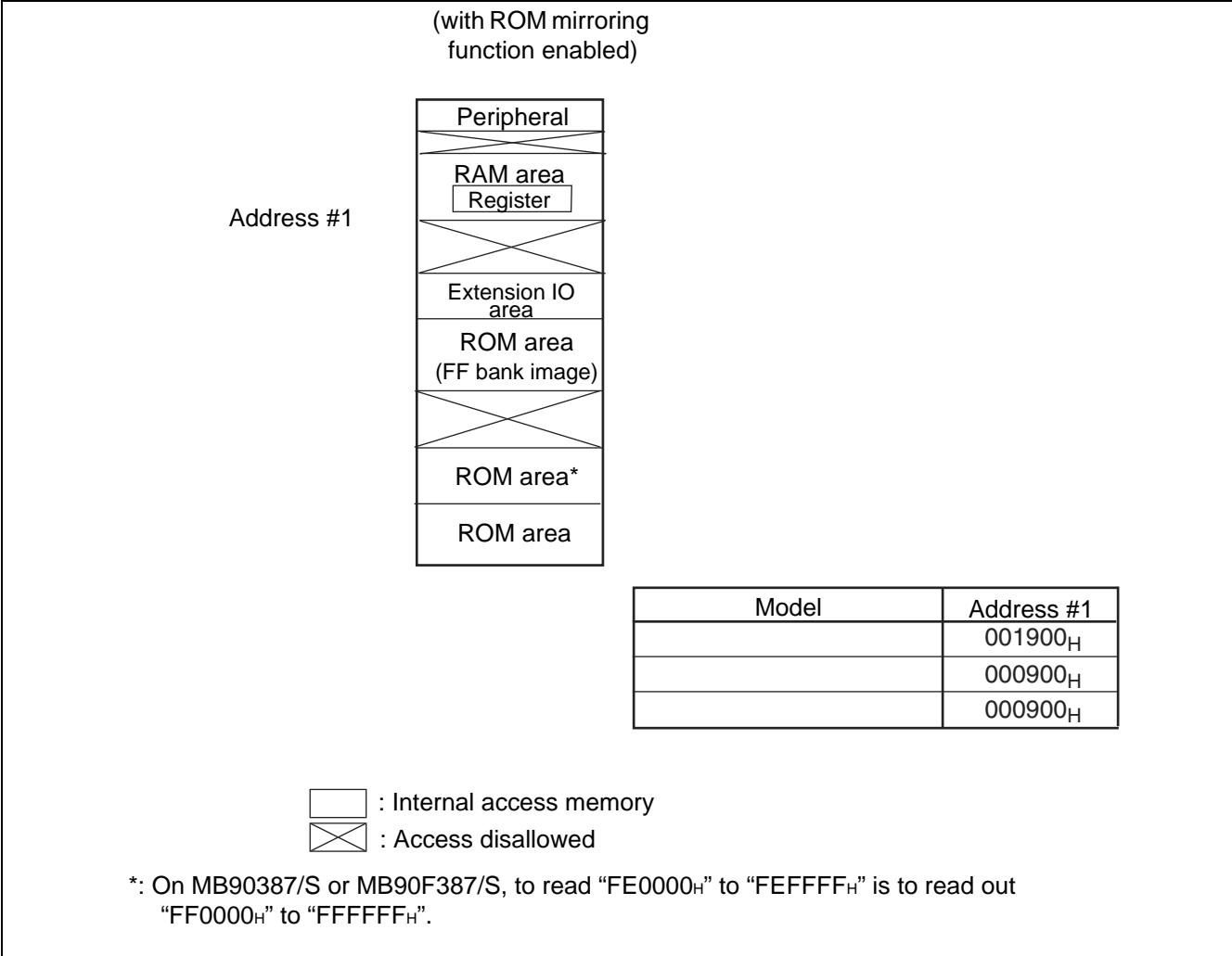
## 9. Memory Map

MB90385 series allows specifying a memory access mode "single chip mode."

### 9.1 Memory Allocation of MB90385

MB90385 series model has 24-bit wide internal address bus and up to 24-bit bus of external address bus. A maximum of 16-Mbyte memory space of external access memory is accessible.

9.2 Memory Map



Note: When internal ROM is operating, F<sup>2</sup>MC-16LX allows viewing ROM data image on FF bank at upper-level of 00 bank. This function is called “mirroring ROM,” which allows effective use of C compiler small model. F<sup>2</sup>MC-16LX assigns the same low order 16-bit address to FF bank and 00 bank, which allows referencing table in ROM without specifying “far” using pointer. For example, when accessing to “00C000<sub>H</sub>”, ROM data at “FFC000<sub>H</sub>” is accessed actually. However, because ROM area of FF bank exceeds 48 Kbytes, viewing all areas is not possible on 00 bank image. Because ROM data of “FF4000<sub>H</sub>” to “FFFFFF<sub>H</sub>” is viewed on “004000<sub>H</sub>” to “00FFFF<sub>H</sub>” image, store a ROM data table in area “FF4000<sub>H</sub>” to “FFFFFF<sub>H</sub>”.



Interrupt Source	EI <sup>2</sup> OS Readiness	Interrupt Vector		Interrupt Control Register		Priority* <sup>3</sup>
		Number	Address	ICR	Address	
UART1 reception completed	⊙	#37	25 <sub>H</sub>	FFFF68 <sub>H</sub>	ICR13	High ↑
UART1 transmission completed	Δ	#38	26 <sub>H</sub>	FFFF64 <sub>H</sub>		
Reserved	×	#39	27 <sub>H</sub>	FFFF60 <sub>H</sub>	ICR14	
Reserved	×	#40	28 <sub>H</sub>	FFFF5C <sub>H</sub>		
Flash memory	×	#41	29 <sub>H</sub>	FFFF58 <sub>H</sub>	ICR15	↓ Low
Delay interrupt generation module	×	#42	2A <sub>H</sub>	FFFF54 <sub>H</sub>		

○ : Available

× : Unavailable

⊙ : Available EI<sup>2</sup>OS function is provided.

Δ: Available when a cause of interrupt sharing a same ICR is not used.

\*1:

- Peripheral functions sharing an ICR register have the same interrupt level.
- If peripheral functions share an ICR register, only one function is available when using expanded intelligent I/O service.
- If peripheral functions share an ICR register, a function using expanded intelligent I/O service does not allow interrupt by another function.

\*2: Input capture 1 corresponds to EI<sup>2</sup>OS, however, PPG does not. When using EI<sup>2</sup>OS by input capture 1, interrupt should be disabled for PPG.

\*3: Priority when two or more interrupts of a same level occur simultaneously.

## 12. Peripheral Resources

### 12.1 I/O Ports

The I/O ports are used as general-purpose input/output ports (parallel I/O ports). The MB60385 series model is provided with 5 ports (34 inputs). The ports function as input/output pins for peripheral functions also.

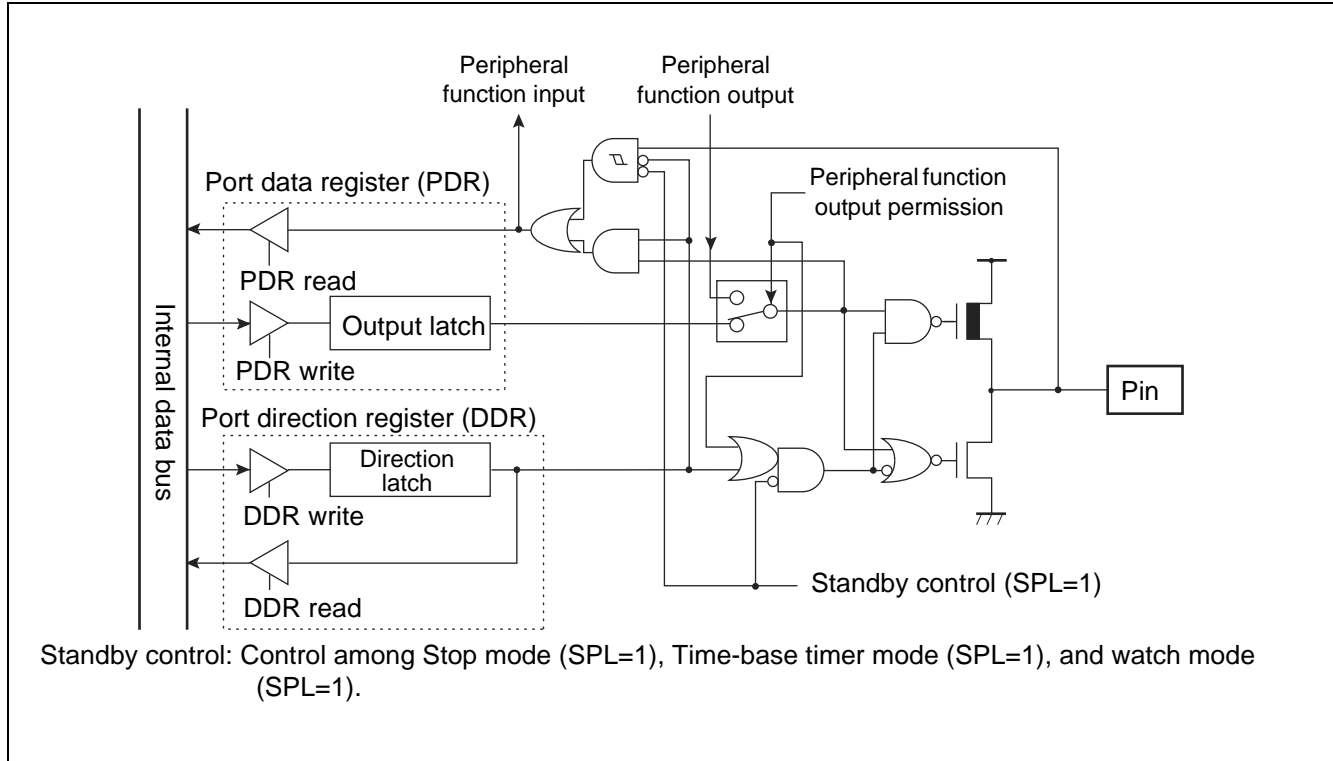
#### I/O Port Functions

An I/O port, using port data register (PDR), outputs the output data to I/O pin and input a signal input to I/O port. The port direction register (DDR) specifies direction of input/output of I/O pins on a bit-by-bit basis.

The following summarizes functions of the ports and sharing peripheral functions:

- Port 1: General-purpose input/output port, used also for PPG timer output and input capture inputs.
- Port 2: General-purpose input/output port, used also for reload timer input/output and external interrupt input.
- Port 3: General-purpose input/output port, used also for A/D converter activation trigger pin.
- Port 4: General-purpose input/output port, used also for UART input/output and CAN controller send/receive pin.
- Port 5: General-purpose input/output port, used also analog input pin.

### Port 4 Pins Block Diagram



### Port 4 Registers

- Port 4 registers include port 4 data register (PDR4) and port 4 direction register (DDR4).
- The bits configuring the register correspond to port 4 pins on a one-to-one basis.

### Relation between Port 4 Registers and Pins

Port Name	Bits of Register and Corresponding Pins								
Port 4	PDR4, DDR4	—	—	—	bit4	bit3	bit2	bit1	bit0
	Corresponding pins	—	—	—	P44	P43	P42	P41	P40

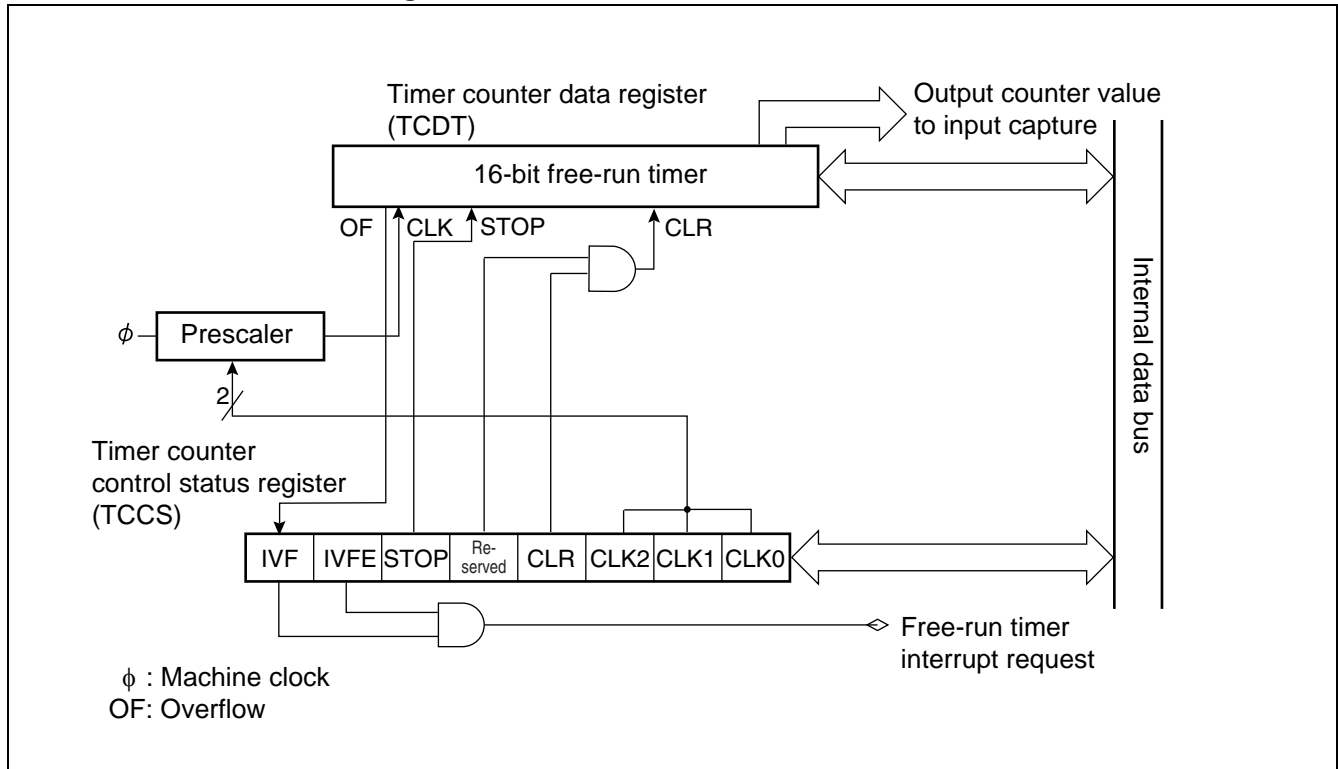
### 16-bit Free-run Timer

Counter value of 16-bit free-run timer is used as reference time (base time) of input capture.

### Input Capture

Input capture detects rising edge, falling edge or both edges and retains a counter value of 16-bit free-run timer. Detection of edge on input signal is allowed to generate interrupt.

### 16-bit Free-run Timer Block Diagram



### Detailed Pin Assignment on Block Diagram

The 16-bit input/output timer includes a 16-bit free-run timer. Interrupt request number of the 16-bit free-run timer is as follows:  
Interrupt request number: 19 (13<sub>H</sub>)

### Prescaler

The prescaler divides a machine clock and provides a counter clock to the 16-bit up counter. Dividing ratio of the machine clock is specified by timer counter control status register (TCCS) among four values.

### Timer Counter Data Register (TCDT)

The timer counter data register is a 16-bit up counter. A current counter value of the 16-bit free-run timer is read. Writing a value during halt of the counter allows setting an arbitrary counter value.

## 12.6 Watch Timer Outline

The watch timer is a 15-bit free-run counter that increments in synchronization with sub clock.

- Interval time is selectable among 7 choices, and generation of interrupt request is allowed for each interval.
- Provides operation clock to the subclock oscillation stabilizing wait timer and watchdog timer.
- Always uses subclock as a count clock regardless of settings of clock selection register (CKSCR).

### Interval Timer Function

- In the watch timer, a bit corresponding to the interval time overflows (carry-over) when an interval time, which is specified by interval time selection bit, is reached. Then overflow flag bit is set (WTC: WTOF=1).
- If an interrupt by overflow is permitted (WTC: WTIE=1), an interrupt request is generated upon setting an overflow flag bit.
- Interval time of watch timer is selectable among the following seven choices:

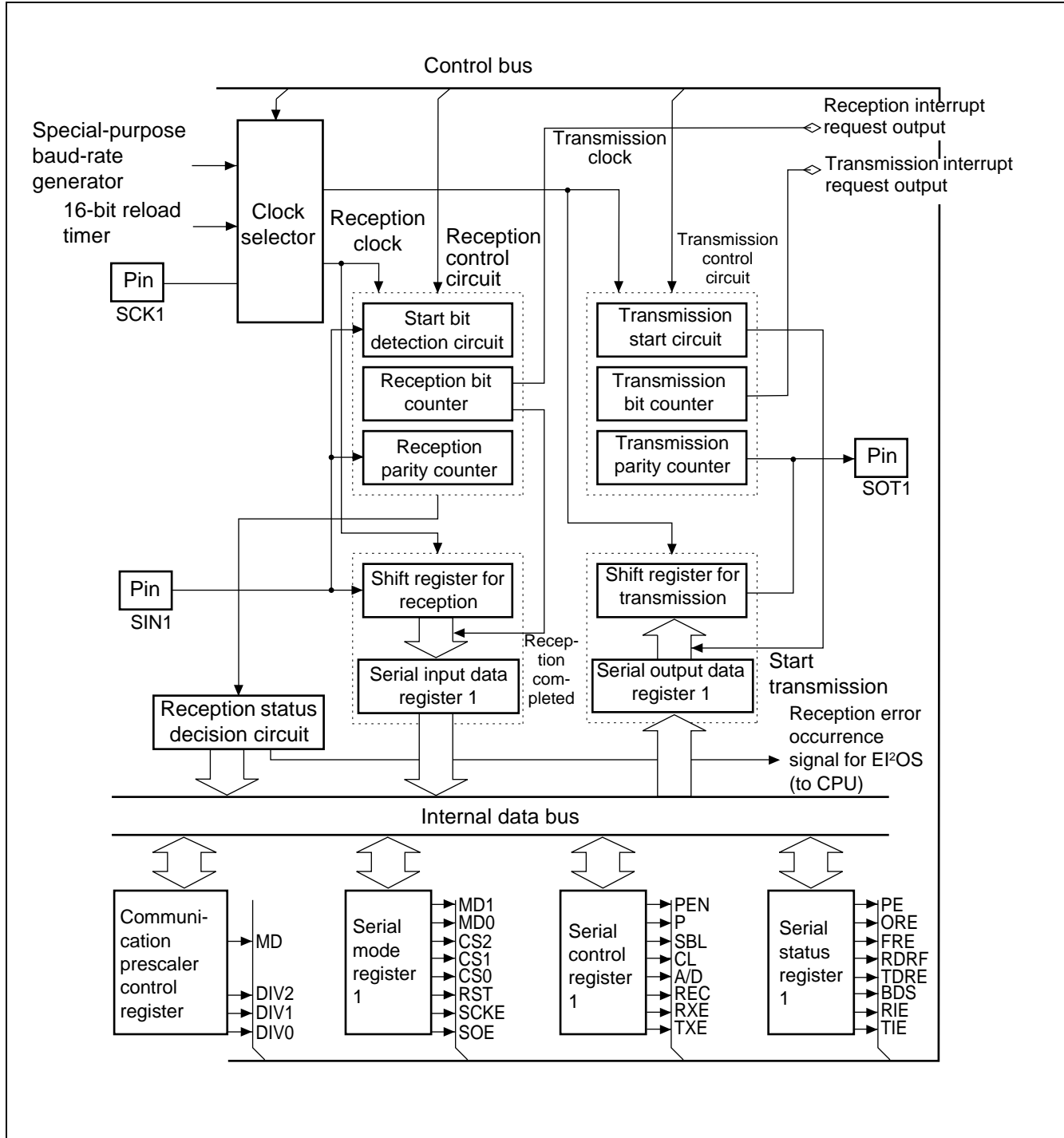
### Interval Time of Watch Timer

Sub Clock Cycle	Interval Time
1/SCLK (122 $\mu$ s)	$2^8$ /SCLK (31.25 ms)
	$2^9$ /SCLK (62.5 ms)
	$2^{10}$ /SCLK (125 ms)
	$2^{11}$ /SCLK (250 ms)
	$2^{12}$ /SCLK (500 ms)
	$2^{13}$ /SCLK (1.0 s)
	$2^{14}$ /SCLK (2.0 s)

SCLK: Sub clock frequency

Values in parentheses “( )” are calculation when operating with 8.192 kHz clock.

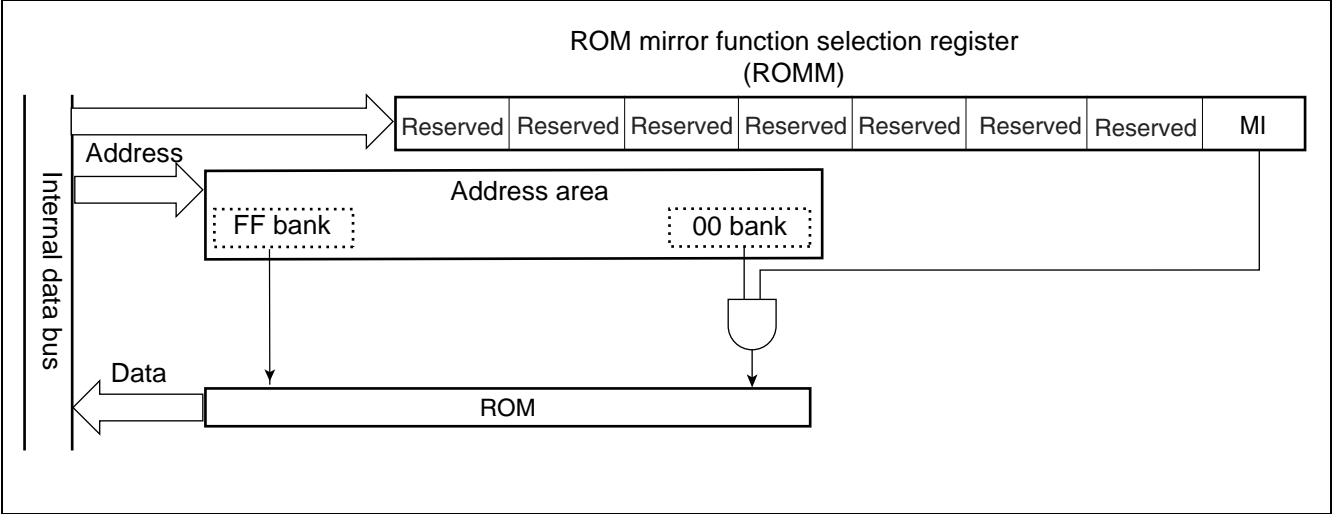
UART Block Diagram



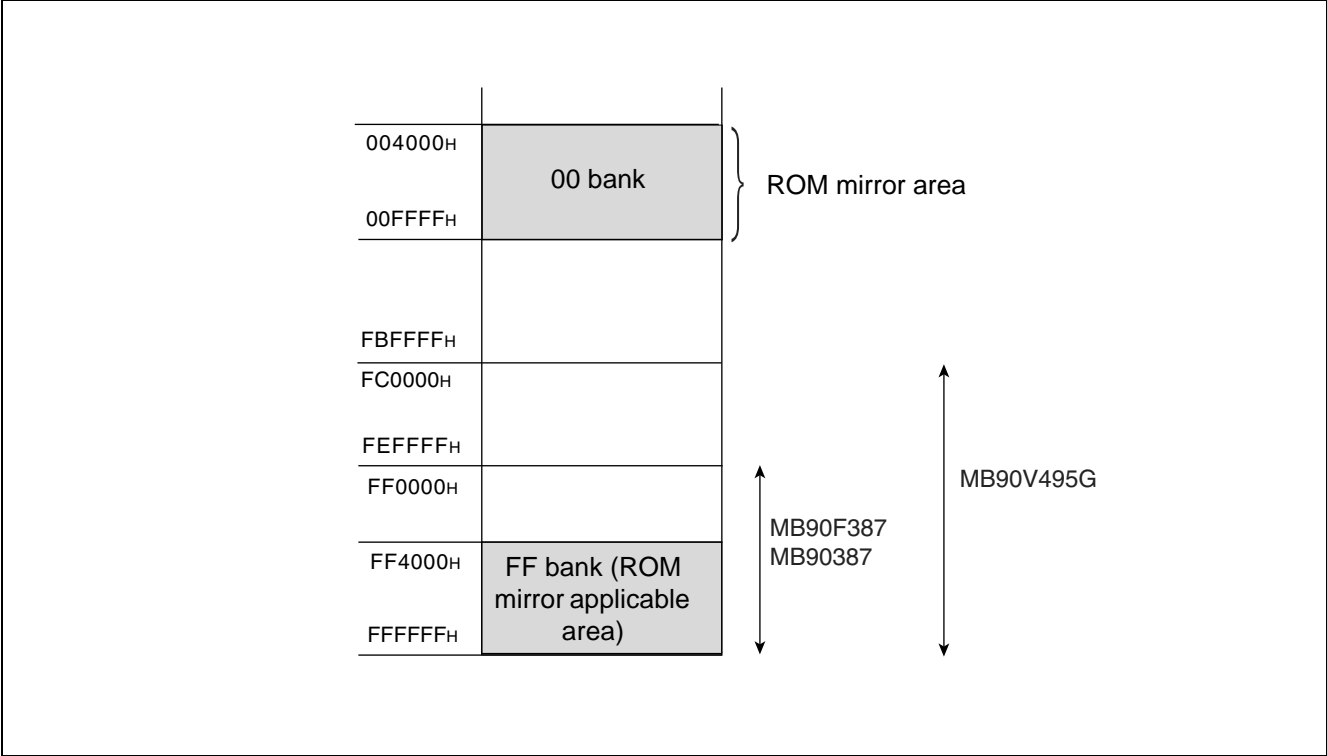
12.14 ROM Mirror Function Selection Module Outline

The ROM mirror function selection module sets the data in ROM assigned to FF bank so that the data is read by access to 00 bank.

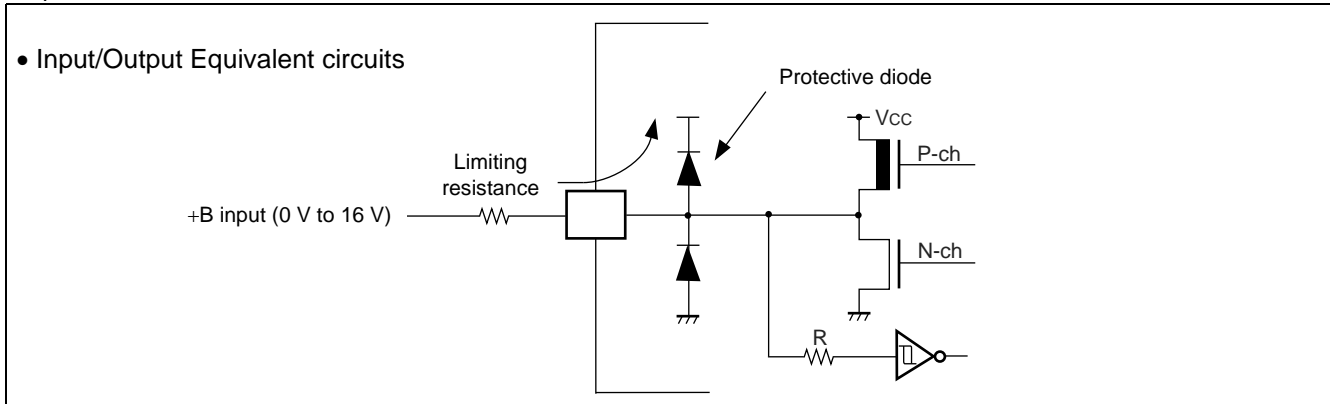
ROM Mirror Function Selection Module Block Diagram



FF Bank Access by ROM Mirror Function



- Use within recommended operating conditions.
- Use at DC voltage (current).
- The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V<sub>CC</sub> pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on reset.
- Care must be taken not to leave the +B input pin open.
- Note that analog system input/output pins other than the A/D input pins (LCD drive pins, comparator input pins, etc.) cannot accept +B signal input.
- Sample recommended circuits:



**WARNING:** Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

#### 13.4.4 UART Timing

( $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ ,  $V_{SS} = 0.0\text{ V}$ ,  $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ )

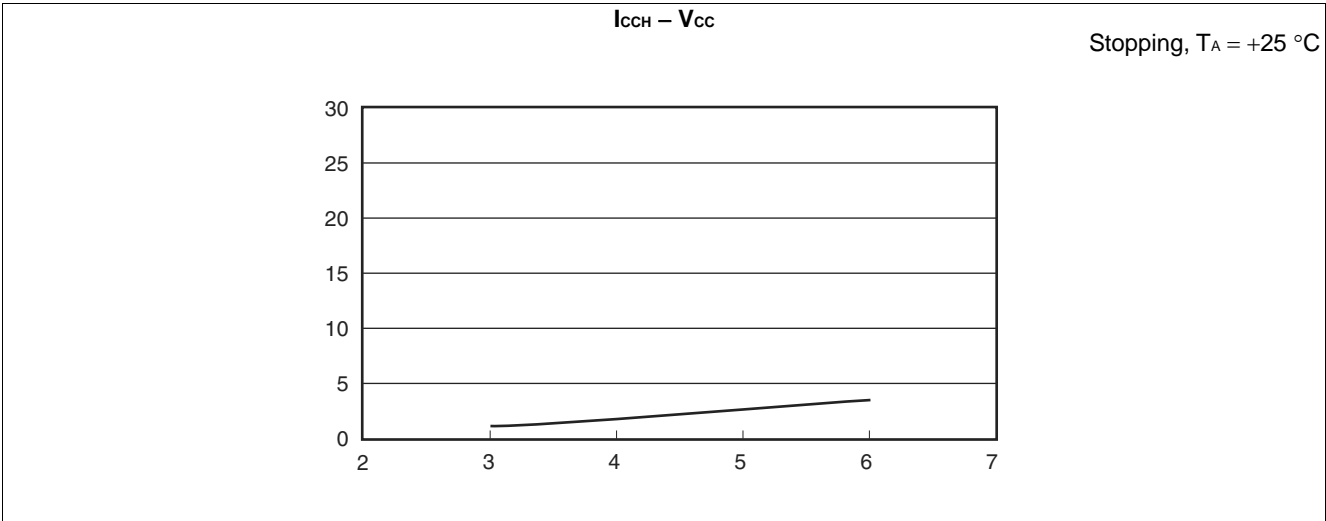
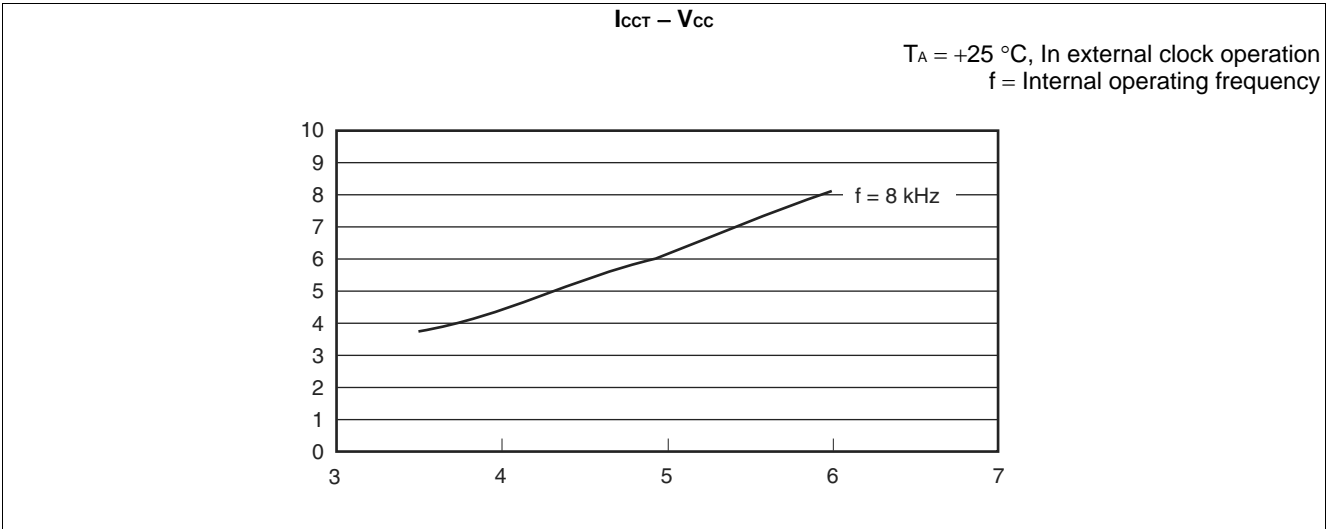
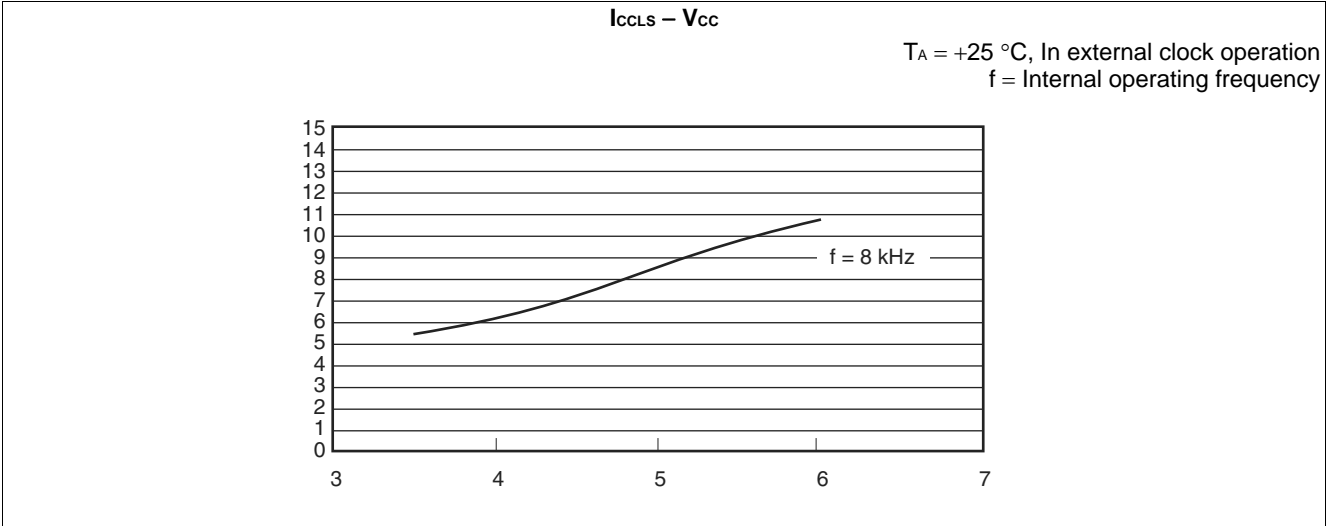
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	$t_{SCYC}$	SCK1	Internal shift clock mode output pin is: CL = 80 pF+1TTL.	$4\ t_{CP}^*$	–	ns	
SCK ↓ → SOT delay time	$t_{SLOV}$	SCK1, SOT1		–80	+80	ns	
Valid SIN → SCK ↑	$t_{IVSH}$	SCK1, SIN1		100	–	ns	
SCK ↑ → valid SIN hold time	$t_{SHIX}$	SCK1, SIN1		60	–	ns	
Serial clock “H” pulse width	$t_{SHSL}$	SCK1	External shift clock mode output pin is: CL = 80 pF+1TTL.	$2\ t_{CP}^*$	–	ns	
Serial clock “L” pulse width	$t_{SLSH}$	SCK1		$2\ t_{CP}^*$	–	ns	
SCK ↓ → SOT delay time	$t_{SLOV}$	SCK1, SOT1		–	150	ns	
Valid SIN → SCK ↑	$t_{IVSH}$	SCK1, SIN1		60	–	ns	
SCK ↑ → valid SIN hold time	$t_{SHIX}$	SCK1, SIN1		60	–	ns	

\*: Refer to Clock Timing ratings for  $t_{CP}$  (internal operation clock cycle time).

Notes:

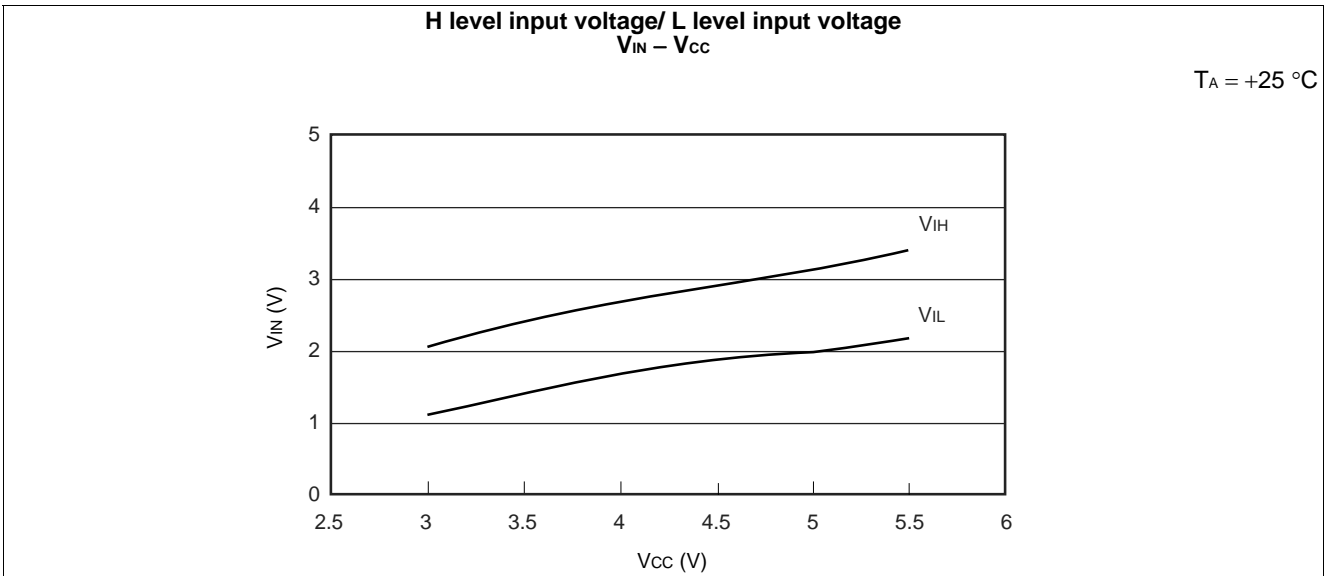
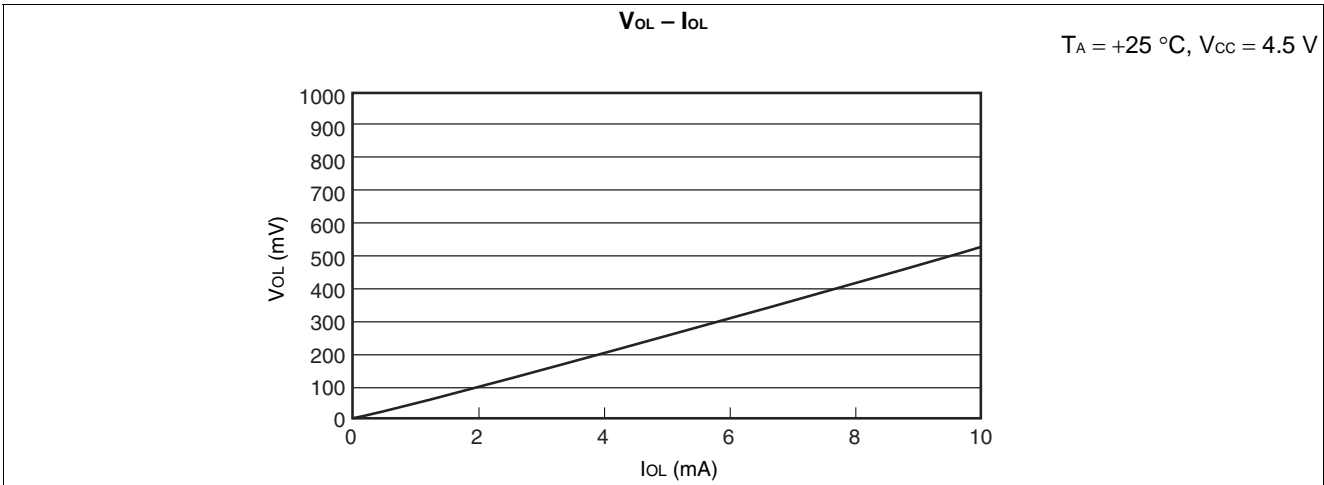
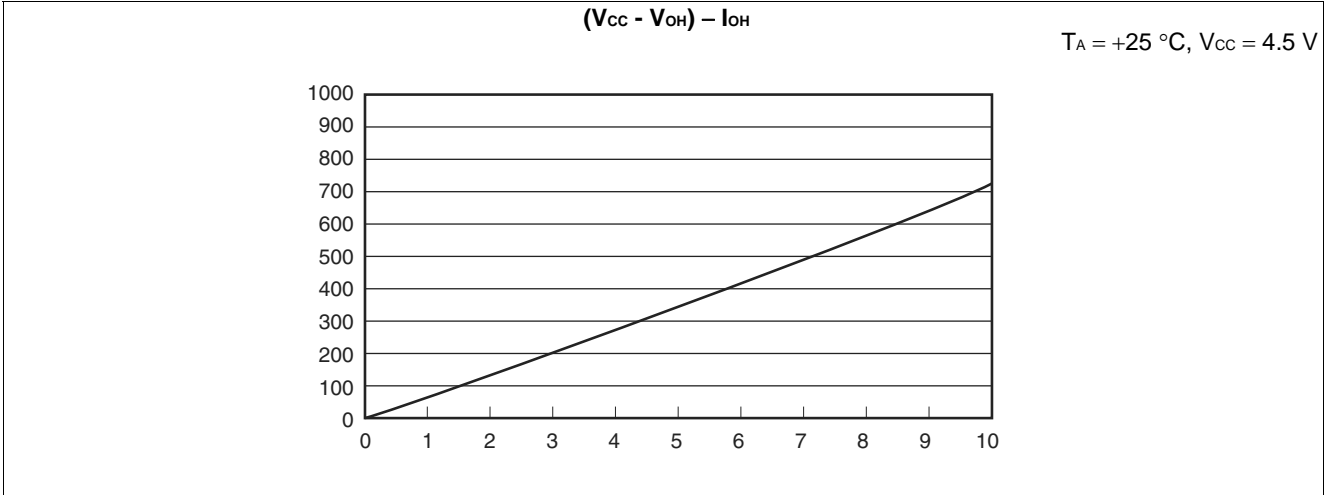
- AC Characteristics in CLK synchronous mode.
- $C_L$  is a load capacitance value on pins for testing.

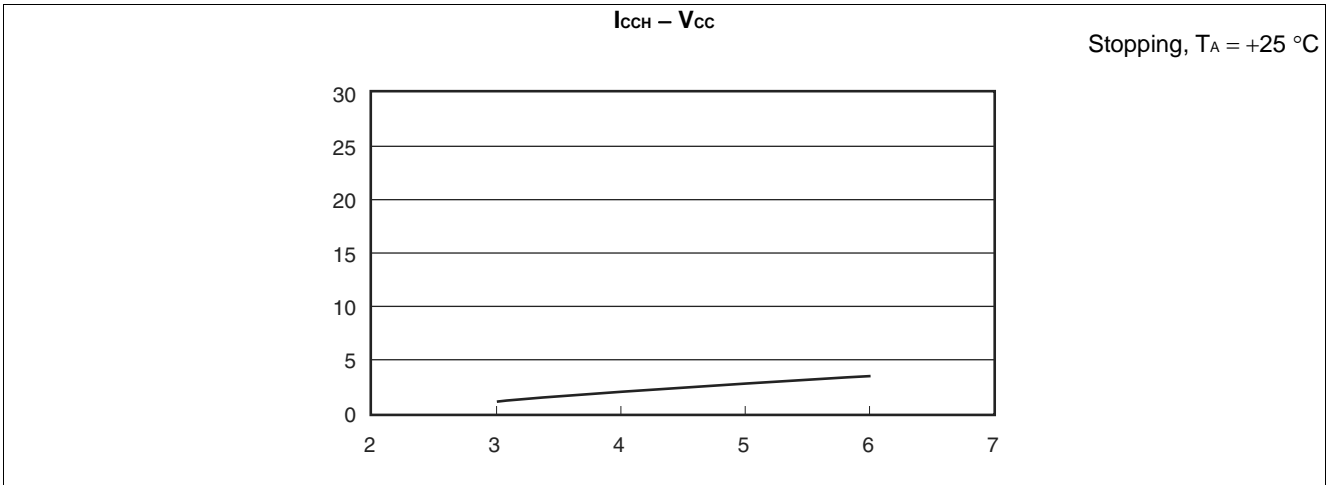
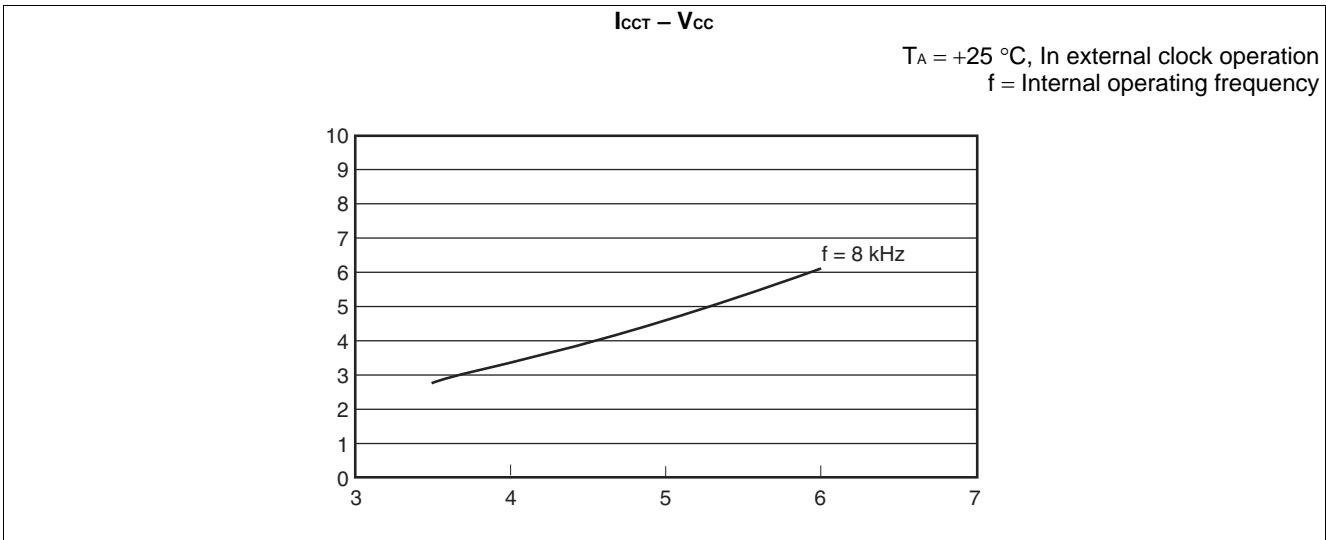
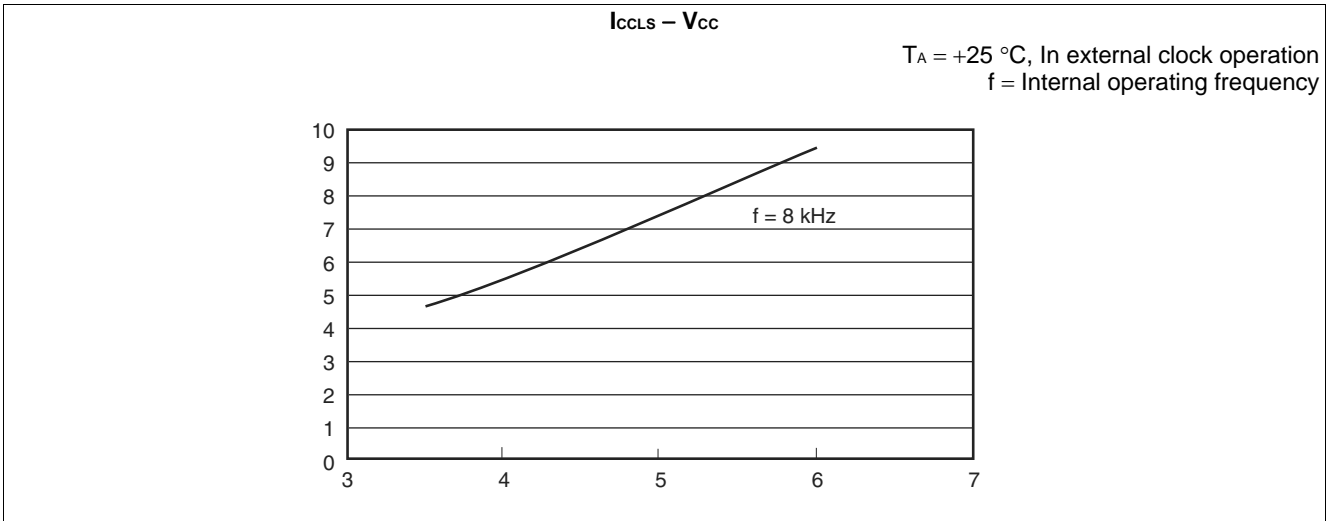




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## Document History

Document Title: MB90387/387S/F387/F387S, MB90V495G, 16-bit Microcontrollers F <sup>2</sup> MC-16LX MB90385 Series Document Number:002-07765				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	—	AKIH	12/19/2008	Migrated to Cypress and assigned document number 002-07765. No change to document contents or format.
*A	6059071	SSAS	02/05/2018	Updated to Cypress template Package: FPT-48P-M26 --> LQA048

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### Technical Support

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