Infineon Technologies - MB90F387SPMT-GS-9001 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, SCI, UART/USART
Peripherals	POR, WDT
Number of I/O	36
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90f387spmt-gs-9001

MB90387/387S/F387/F387S
MB90V495G

16-bit Microcontrollers
F²MC-16LX MB90385 Series

MB90385 series devices are general-purpose high-performance 16-bit micro controllers designed for process control of consumer products, which require high-speed real-time processing. The devices of this series have the built-in full-CAN interface.
The system, inheriting the architecture of F²MC family, employs additional instruction ready for high-level languages, expanded addressing mode, enhanced multiply-divide instructions, and enriched bit-processing instructions. Furthermore, employment of 32-bit accumulator achieves processing of long-word data (32 bits).
The peripheral resources of MB90385 series include the following:
8/10-bit A/D converter, UART (SCI), 8/16-bit PPG timer, 16-bit input-output timer (16-bit free-run timer, input capture 0, 1, 2, 3 (ICU)), and CAN controller.

Features

Clock

- Built-in PLL clock frequency multiplication circuit
- Selection of machine clocks (PLL clocks) is allowed among frequency division by two on oscillation clock, and multiplication of 1 to 4 times of oscillation clock (for 4-MHz oscillation clock, 4 MHz to 16 MHz).
- Operation by sub-clock (8.192 kHz) is allowed. (MB90387, MB90F387)
- Minimum execution time of instruction: 62.5 ns (when operating with 4-MHz oscillation clock, and 4-time multiplied PLL clock).

16 Mbyte CPU memory Space

- 24-bit internal addressing

Instruction System Best Suited to Controller

- Wide choice of data types (bit, byte, word, and long word)
- Wide choice of addressing modes (23 types)
- Enhanced multiply-divide instructions and RETI instructions
- Enhanced high-precision computing with 32-bit accumulator

Instruction System Compatible with High-level Language (C language) and Multitask

- Employing system stack pointer
- Enhanced various pointer indirect instructions
- Barrel shift instructions

Increased Processing Speed

- 4-byte instruction queue

Powerful Interrupt Function with 8 Levels and 34 Factors

Automatic Data Transfer Function Independent of CPU

- Expanded intelligent I/O service function (EI² OS): Maximum of 16 channels

Low Power Consumption (standby) Mode

- Sleep mode (a mode that halts CPU operating clock)
- Time-base timer mode (a mode that operates oscillation clock, sub clock, time-base timer and watch timer only)
- Watch mode (a mode that operates sub clock and watch timer only)
- Stop mode (a mode that stops oscillation clock and sub clock)
- CPU blocking operation mode

Process

- CMOS technology

I/O Port

- General-purpose input/output port (CMOS output):

  MB90387, MB90F387: 34 ports (including 4 high-current output ports)
  MB90387S, MB90F387S: 36 ports (including 4 high-current output ports)

Timer

- Time-base timer, watch timer, watchdog timer: 1 channel
- 8/16-bit PPG timer: 8-bit x 4 channels, or 16-bit x 2 channels
- 16-bit reload timer: 2 channels
- 16-bit input/output timer
  - ❒ 16-bit free run timer: 1 channel
  - ❒ 16-bit input capture: (ICU): 4 channels

  Interrupt request is issued upon latching a count value of 16-bit free run timer by detection of an edge on pin input.

CAN Controller: 1 channel

- Compliant with Ver2.0A and Ver2.0B CAN specifications
- 8 built-in message buffers
- Transmission rate of 10 kbps to 1 Mbps (by 16 MHz machine clock)
- CAN wake-up

UART (SCI): 1 channel

- Equipped with full-duplex double buffer
- Clock-asynchronous or clock-synchronous serial transmission is available.

Parameter \ Part Number	MB90F387 MB90F387S	MB90387 MB90387S	MB90V495G
8/10-bit A/D converter	Number of channels: 8 Resolution: Selectable 10-bit or 8-bit. Conversion time: 6.125 μs (at 16 MHz machine clock, including sampling time) Sequential conversion of two or more successive channels is allowed. (Setting a maximum of 8 channels is allowed.) Single conversion mode: Selected channel is converted only once. Sequential conversion mode: Selected channel is converted repetitively. Halt conversion mode: Conversion of selected channel is stopped and activated alternately.		
UART(SCI)	Number of channels: 1 Clock-synchronous transfer: 62.5 kbps to 2 Mbps Clock-asynchronous transfer: 9,615 bps to 500 kbps Communication is allowed by bi-directional serial communication function and master/slave type connection.		
CAN	Compliant with Ver 2.0A and Ver 2.0B CAN specifications. 8 built-in message buffers. Transmission rate of 10 kbps to 1 Mbps (by 16 MHz machine clock) CAN wake-up		

*1: Settings of DIP switch S2 for using emulation pod MB2145-507. For details, see MB2145-507 Hardware Manual (2.7 Power Pin solely for Emulator).

*2: MB90387S, MB90F387S

2. Packages And Product Models

Package	MB90F387, MB90F387S	MB90387, MB90387S
LQA048	◯	◯

◯: Yes ×: No

Note: Refer to Package Dimension for details of the package.

3. Product Comparison

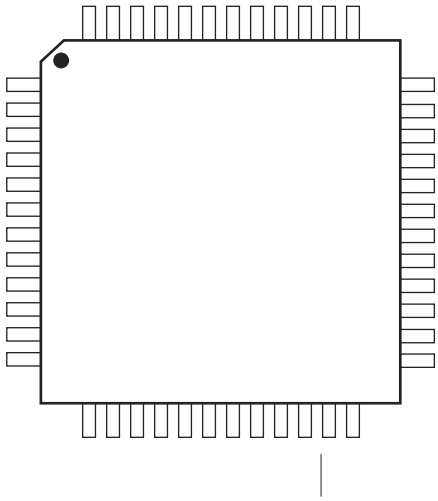
Memory Space

When testing with test product for evaluation, check the differences between the product and a product to be used actually. Pay attention to the following points:

- The MB90V495G has no built-in ROM. However, a special-purpose development tool allows the operations as those of one with built-in ROM. ROM capacity depends on settings on a development tool.
- On MB90V495G, an image from $FF4000_H$ to $FFFFFF_H$ is viewed on 00 bank and an image of $FE0000_H$ to $FF3FFF_H$ is viewed only on FE bank and FF bank. (Modified on settings of a development tool.)
- On MB90F387/F387S/387/387S, an image from $FF4000_H$ to $FFFFFF_H$ is viewed on 00 bank and an image of $FE0000_H$ to $FF3FFF_H$ is viewed only on FF bank.

4. Pin Assignment

(Top View)



(LQA048)

*: MB90387, MB90F387 : X1A, X0A
MB90387S, MB90F387S: P36, P35

Interrupt Source	EI²OS Readiness	Interrupt Vector			Interrupt Control Register		Priority*3
		Number		Address	ICR	Address	
UART1 reception completed	◎	#37	25H	FFFF68H	ICR13	0000BDH*1	High
UART1 transmission completed	Δ	#38	26H	FFFF64H			↑
Reserved	×	#39	27H	FFFF60H	ICR14	0000BEH*1	
Reserved	×	#40	28H	FFFF5CH			
Flash memory	×	#41	29H	FFFF58H	ICR15	0000BFH*1	↓
Delay interrupt generation module	×	#42	2AH	FFFF54H			Low

○ : Available

× : Unavailable

◎ : Available EI²OS function is provided.

Δ: Available when a cause of interrupt sharing a same ICR is not used.

*1:

- ❒ Peripheral functions sharing an ICR register have the same interrupt level.
- ❒ If peripheral functions share an ICR register, only one function is available when using expanded intelligent I/O service.
- ❒ If peripheral functions share an ICR register, a function using expanded intelligent I/O service does not allow interrupt by another function.

*2: Input capture 1 corresponds to EI²OS, however, PPG does not. When using EI²OS by input capture 1, interrupt should be disabled for PPG.

*3:Priority when two or more interrupts of a same level occur simultaneously.

12. Peripheral Resources

12.1 I/O Ports

The I/O ports are used as general-purpose input/output ports (parallel I/O ports). The MB60385 series model is provided with 5 ports (34 inputs). The ports function as input/output pins for peripheral functions also.

I/O Port Functions

An I/O port, using port data resister (PDR), outputs the output data to I/O pin and input a signal input to I/O port. The port direction register (DDR) specifies direction of input/output of I/O pins on a bit-by-bit basis.

The following summarizes functions of the ports and sharing peripheral functions:

■ Port 1: General-purpose input/output port, used also for PPG timer output and input capture inputs.

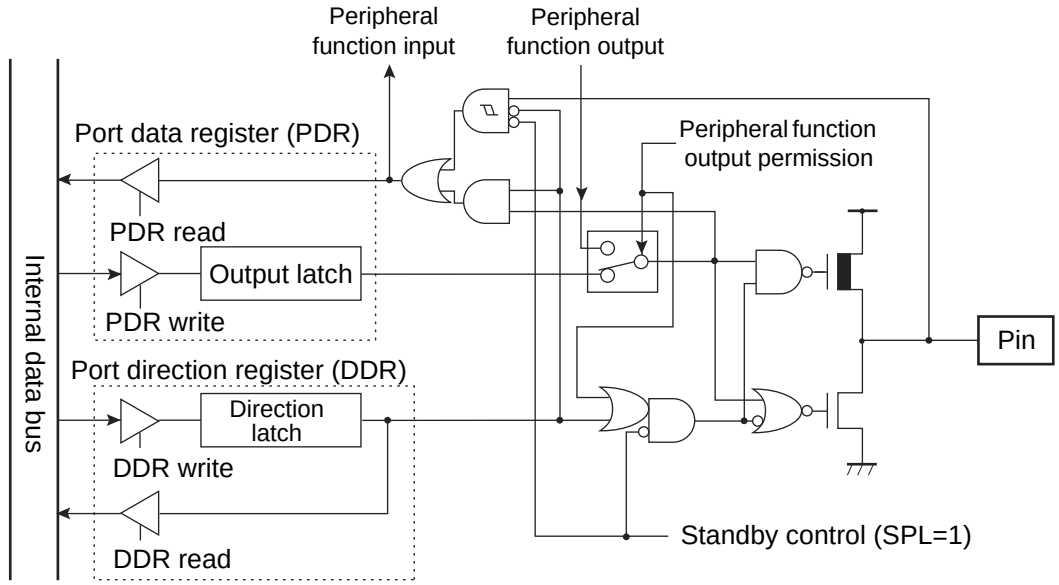
■ Port 2: General-purpose input/output port, used also for reload timer input/output and external interrupt input.

■ Port 3: General-purpose input/output port, used also for A/D converter activation trigger pin.

■ Port 4: General-purpose input/output port, used also for UART input/output and CAN controller send/receive pin.

■ Port 5: General-purpose input/output port, used also analog input pin.

Port 1 Pins Block Diagram (single-chip mode)



Standby control: Control among Stop mode (SPL=1), Time-base timer mode (SPL=1), and watch mode (SPL=1).

Port 1 Registers (single-chip mode)

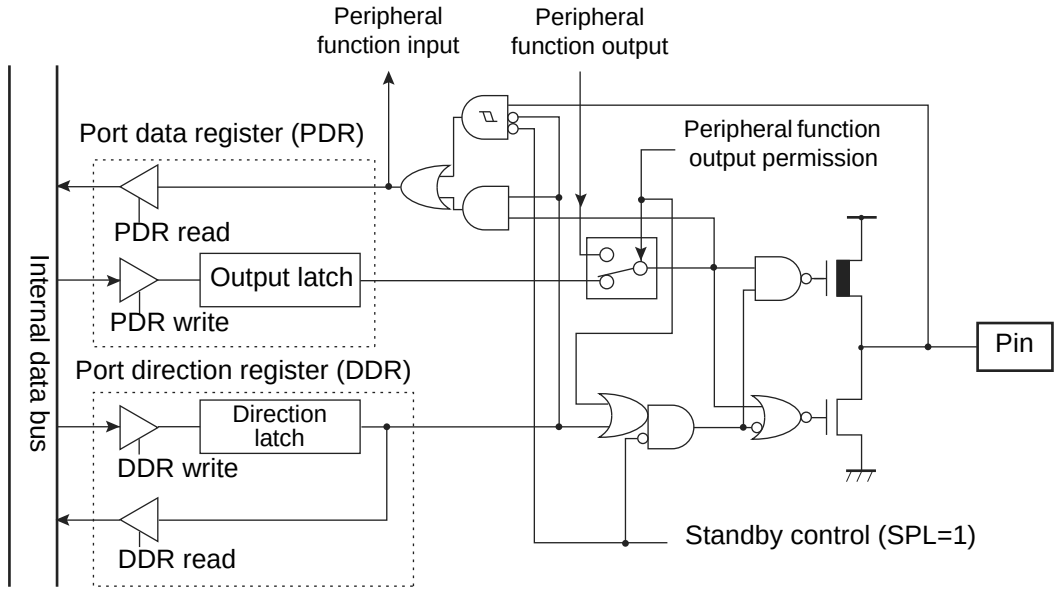
■ Port 1 registers include port 1 data register (PDR1) and port 1 direction register (DDR1).

■ The bits configuring the register correspond to port 1 pins on a one-to-one basis.

Relation between Port 1 Registers and Pins

Port Name	Bits of Register and Corresponding Pins								
Port 1	PDR1, DDR1	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	Corresponding pins	P17	P16	P15	P14	P13	P12	P11	P10

Port 2 Pins Block Diagram (general-purpose input/output port)



Standby control: Control among Stop mode (SPL=1), Time-base timer mode (SPL=1), and watch mode (SPL=1).

Port 2 Registers

■ Port 2 registers include port 2 data register (PDR2) and port 2 direction register (DDR2).

■ The bits configuring the register correspond to port 2 pins on a one-to-one basis.

Relation between Port 2 Registers and Pins

Port Name	Bits of Register and Corresponding Pins									
Port 2	PDR2,DDR2	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	Corresponding pins	P27	P26	P25	P24	P23	P22	P21	P20

12.2 Time-Base Timer

The time-base time is an 18-bit free-run counter (time-base timer counter) that counts up in synchronization with the main clock (dividing main oscillation clock by 2).

- Four choices of interval time are selectable, and generation of interrupt request is allowed for each interval time.
- Provides operation clock signal to oscillation stabilizing wait timer and peripheral functions.

Interval Timer Function

- When the counter of time-base timer reaches an interval time specified by interval time selection bit (TBTC:TBC1, TBC0), an overflow (carrying-over) occurs (TBTC: TBOF=1) and interrupt request is generated.
- If an interrupt by overflow is permitted (TBTC: TBIE=1), an interrupt is generated when overflow occurs (TBTC: TBOF=1).
- The following four interval time settings are selectable:

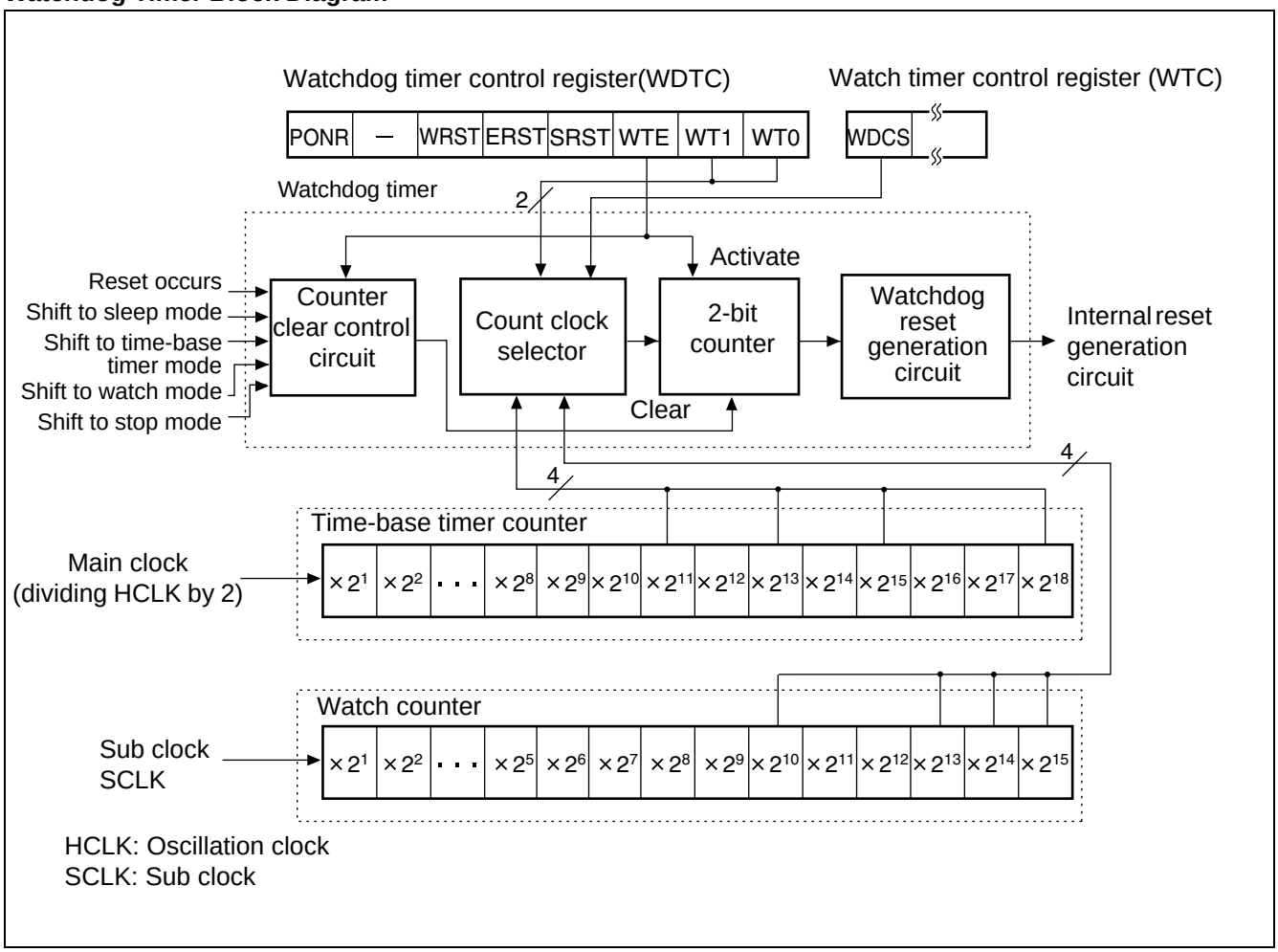
Interval Time of Time-base Timer

Count Clock	Interval Time
2/HCLK (0.5 μs)	2^{12}/HCLK (Approx. 1.0 ms)
	2^{14}/HCLK (Approx. 4.1 ms)
	2^{16}/HCLK (Approx. 16.4 ms)
	2^{19}/HCLK (Approx. 131.1 ms)

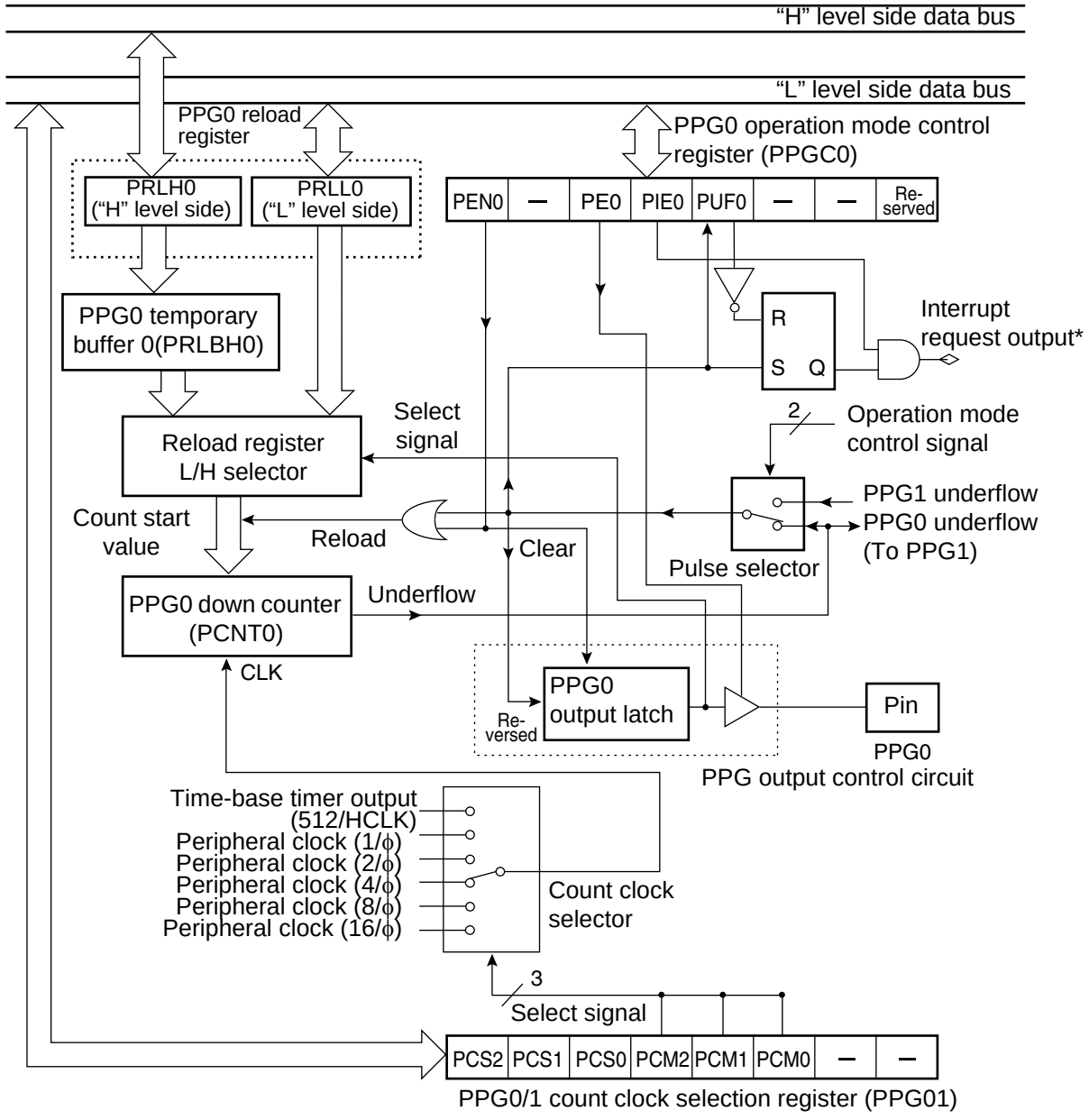
HCLK: Oscillation clock

Values in parentheses “( )” are those under operation of 4-MHz oscillation clock.

Watchdog Timer Block Diagram



8/16-bit PPG Timer 0 Block Diagram



– : Undefined
Reserved: Reserved bit
HCLK : Oscillation clock frequency
ϕ : Machine clock frequency
* : Interrupt output of 8/16-bit PPG timer 0 is incorporated into one by the OR circuit against interrupt output of 8/16-bit PPG timer 1.

12.10 8/10-bit A/D Converter

The 8/10-bit A/D converter converts an analog input voltage into 8-bit or 10/bit digital value, using the RC-type successive approximation conversion method.

- Input signal is selected among 8 channels of analog input pins.
- Activation trigger is selected among software trigger, internal timer output, and external trigger.

Functions of 8/10-bit A/D Converter

The 8/10-bit A/D converter converts an analog voltage (input voltage) input to analog input pin into an 8-bit or 10-bit digital value (A/D conversion).

The 8/10-bit A/D converter has the following functions:

- A/D conversion takes a minimum of 6.12 μs* for 1 channel, including sampling time. (A/D conversion)
- Sampling of one channel takes a minimum of 2.0 μs*.
- RC-type successive approximation conversion method, with sample & hold circuit is used for conversion.
- Resolution of either 8 bits or 10 bits is specifiable.
- A maximum of 8 channels of analog input pins are allowed for use.
- Generation of interrupt request is allowed, by storing A/D conversion result in A/D data register.
- Activation of EI^{2}OS is allowed upon occurrence of an interrupt request. With use of EI^{2}OS, data loss is avoided even if A/D conversion is performed successively.
- An activation trigger is selectable among software trigger, internal timer output, and external trigger (fall edge).

: When operating with 16 MHz machine clock

8/10-bit A/D Converter Conversion Mode

Conversion Mode	Description
Singular conversion mode	The A/D conversion is performed form a start channel to an end channel sequentially. Upon completion of A/D conversion on an end channel, A/D conversion function stops.
Sequential conversion mode	The A/D conversion is performed form a start channel to an end channel sequentially. Upon completion of A/D conversion on an end channel, A/D conversion function resumes from the start channel.
Pausing conversion mode	The A/D conversion is performed by pausing at each channel. Upon completion of A/D conversion on an end channel, A/D conversion and pause functions resume from the start channel.

12.11 UART Outline

UART is a general-purpose serial data communication interface for synchronous and asynchronous communication using external devices.

- Provided with bi-directional communication function for both clock-synchronous and clock-asynchronous modes.
- Provided with master/slave communication function (multi-processor mode). (Only master side is available.)
- Interrupt request is generated upon completion of reception, completion of transmission and detection of reception error.
- Ready for expanded intelligent service, EI^{2}OS.

Table 12-3. UART Functions

	Description
Data buffer	Full-duplex double buffer
Transmission mode	Clock synchronous (No start/stop bit, no parity bit) Clock asynchronous (start-stop synchronous)
Baud rate	Built-in special-purpose baud-rate generator. Setting is selectable among 8 values. Input of external values is allowed. Use of clock from external timer (16-bit reload timer 0) is allowed.
Data length	7 bits (only asynchronous normal mode) 8 bits
Signaling system	Non Return to Zero (NRZ) system
Reception error detection	Framing error Overrun error Parity error (not detectable in operation mode 1 (multi-processor mode))
Interrupt request	Receive interrupt (reception completed, reception error detected) Transmission interrupt (transmission completed) Ready for expanded intelligent I/O service (EI^{2}OS) in both transmission and reception
Master/slave communication function (asynchronous, multi-processor mode)	Communication between 1 (master) and n (slaves) are available (usable as master only).

Note: Start/stop bit is not added upon clock-synchronous transmission. Data only is transmitted.

Table 12-4. UART Operation Modes

Operation Mode		Data Length		Synchronization	Stop Bit Length
		With Parity	Without Parity		
0	Asynchronous mode (normal mode)	7-bit or 8-bit		Asynchronous	1- bit or 2-bit *2
1	Multi processor mode	8+1*1	–	Asynchronous	
2	Synchronous mode	8	–	Synchronous	No

–: Disallowed

1: “+1” is an address/data selection bit used for communication control (bit 11 of SCR1 register: A/D).

2: Only 1 bit is detected as a stop bit on data reception.

13. Electrical Characteristics

13.1 Absolute Maximum Rating

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	
	AV_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	$V_{CC} = AV_{CC}$*2
	AVR	V_{SS} – 0.3	V_{SS} + 6.0	V	$AV_{CC} \geq AVR$*2
Input voltage*1	V_I	V_{SS} – 0.3	V_{SS} + 6.0	V	*3
Output voltage*1	V_O	V_{SS} – 0.3	V_{SS} + 6.0	V	*3
Maximum clamp current	I_{CLAMP}	– 2.0	+ 2.0	mA	*7
Total maximum clamp current	$\Sigma \mid I_{CLAMP} \mid$	–	20	mA	*7
“L” level maximum output current	I_{OL1}	–	15	mA	Normal output*4
	I_{OL2}	–	40	mA	High-current output*4
“L” level average output current	I_{OLAV1}	–	4	mA	Normal output*5
	I_{OLAV2}	–	30	mA	High-current output*5
“L” level maximum total output current	ΣI_{OL1}	–	125	mA	Normal output
	ΣI_{OL2}	–	160	mA	High-current output
“L” level average total output current	ΣI_{OLAV1}	–	40	mA	Normal output*6
	ΣI_{OLAV2}	–	40	mA	High-current output*6
“H” level maximum output current	I_{OH1}	–	–15	mA	Normal output*4
	I_{OH2}	–	–40	mA	High-current output*4
“H” level average output current	I_{OHAV1}	–	–4	mA	Normal output*5
	I_{OHAV2}	–	–30	mA	High-current output*5
“H” level maximum total output current	ΣI_{OH1}	–	–125	mA	Normal output
	ΣI_{OH2}	–	–160	mA	High-current output
“H” level average total output current	ΣI_{OHAV1}	–	–40	mA	Normal output*6
	ΣI_{OHAV2}	–	–40	mA	High-current output*6
Power consumption	P_D	–	245	mW	
Operating temperature	T_A	–40	+105	°C	
Storage temperature	Tstg	–55	+150	°C	

*1: The parameter is based on $V_{SS} = AV_{SS} = 0.0$ V.

*2: AVcc and AVR should not exceed Vcc.

*3: V_I and V_O should not exceed Vcc + 0.3 V. However if the maximum current to/from an input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating.

*4: A peak value of an applicable one pin is specified as a maximum output current.

*5: An average current value of an applicable one pin within 100 ms is specified as an average output current. (Average value is found by multiplying operating current by operating rate.)

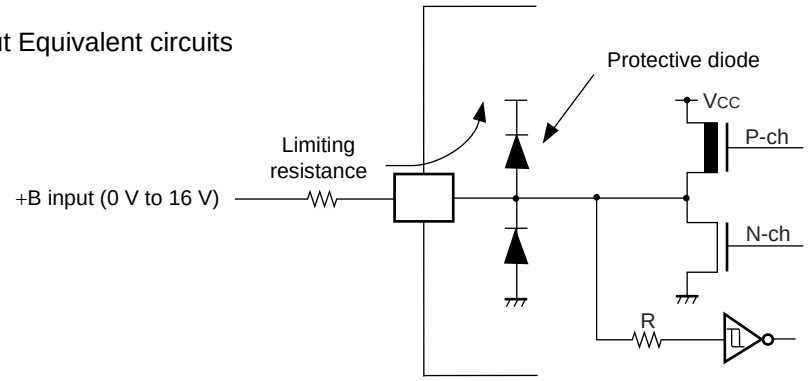
*6: An average current value of all pins within 100 ms is specified as an average total output current. (Average value is found by multiplying operating current by operating rate.)

*7:

■ Applicable to pins: P10 to P17, P20 to P27, P30 to P33, P35*, P36*, P37, P40 to P44, P50 to P57
*: P35 and P36 are MB90387S and MB90F387S only.

- Use within recommended operating conditions.
- Use at DC voltage (current).
- The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on reset.
- Care must be taken not to leave the +B input pin open.
- Note that analog system input/output pins other than the A/D input pins (LCD drive pins, comparator input pins, etc.) cannot accept +B signal input.
- Sample recommended circuits:

• Input/Output Equivalent circuits



WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

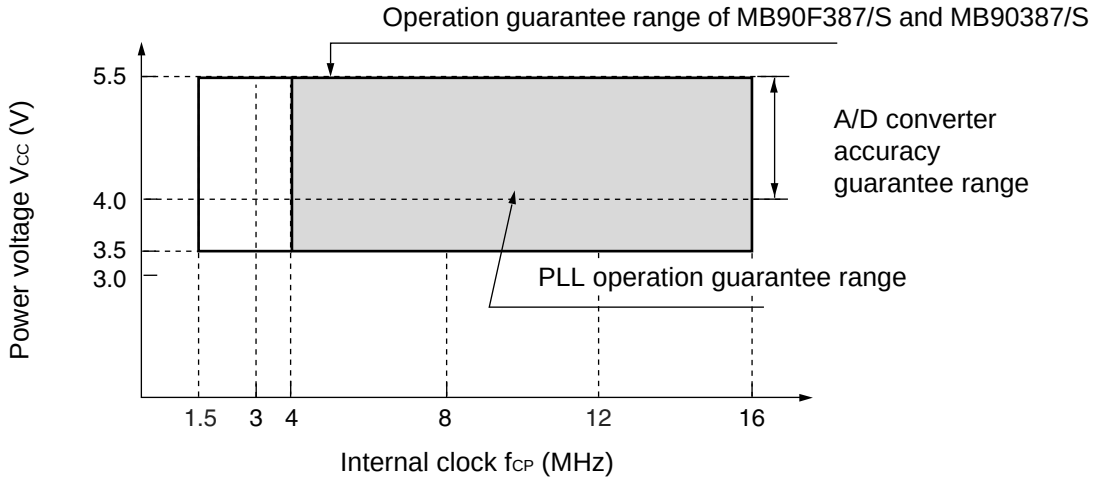
13.3 DC Characteristics

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

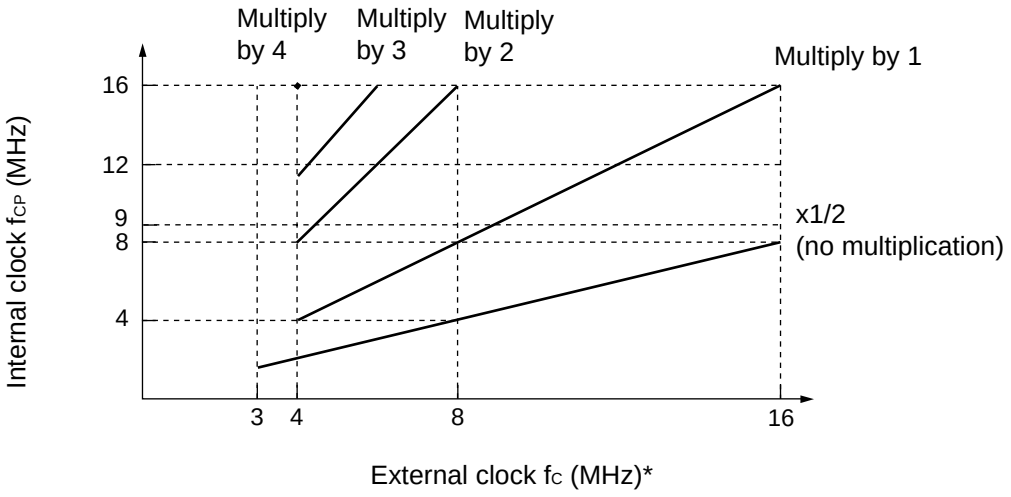
Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IHS}	CMOS hysteresis input pin	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	
	V_{IHM}	MD input pin	—	V_{CC} – 0.3	—	V_{CC} + 0.3	V	
"L" level input voltage	V_{ILS}	CMOS hysteresis input pin	—	V_{SS} – 0.3	—	0.2 V_{CC}	V	
	V_{ILM}	MD input pin	—	V_{SS} – 0.3	—	V_{SS} + 0.3	V	
"H" level output voltage	V_{OH1}	Pins other than P14 to P17	V_{CC} = 4.5 V, I_{OH} = –4.0 mA	V_{CC} – 0.5	—	—	V	
	V_{OH2}	P14 to P17	V_{CC} = 4.5 V, I_{OH} = –14.0 mA	V_{CC} – 0.5	—	—	V	
"L" level output voltage	V_{OL1}	Pins other than P14 to P17	V_{CC} = 4.5 V, I_{OL} = 4.0 mA	—	—	0.4	V	
	V_{OL2}	P14 to P17	V_{CC} = 4.5 V, I_{OL} = 20.0 mA	—	—	0.4	V	
Input leak current	I_{IL}	All input pins	V_{CC} = 5.5 V, V_{SS} < V_I < V_{CC}	–5	—	+5	µA	
Power supply current*	I_{CC}	V_{CC}	V_{CC} = 5.0 V, Internally operating at 16 MHz, normal operation.	—	25	30	mA	
			V_{CC} = 5.0 V, Internally operating at 16 MHz, writing on Flash memory.	—	45	50	mA	MB90F387/S
			V_{CC} = 5.0 V, Internally operating at 16 MHz, deleting on Flash memory.	—	45	50	mA	MB90F387/S
	I_{CCS}		V_{CC} = 5.0 V, Internally operating at 16 MHz, sleeping.	—	8	12	mA	
	I_{CTS}		V_{CC} = 5.0 V, Internally operating at 2 MHz, transition from main clock mode, in time-base timer mode.	—	0.75	1.0	mA	MB90F387/S
					0.2	0.35		MB90387/S

• PLL operation guarantee range

Relation between internal operation clock frequency and power supply voltage



Relation among external clock frequency and internal clock frequency

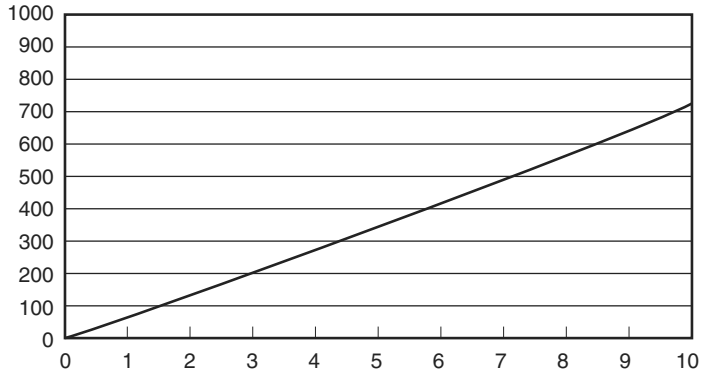


*: fc is 8 MHz at maximum when crystal or ceramic resonator circuit is used.

(Continued)

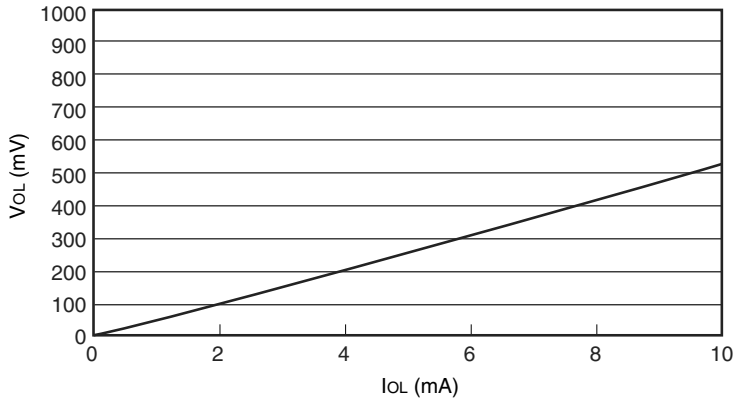
(V_{CC} - V_{OH}) – I_{OH}

T_A = +25 °C, V_{CC} = 4.5 V



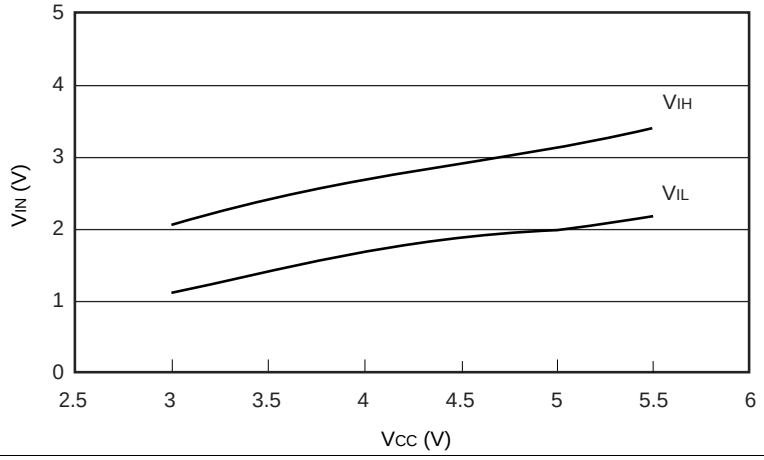
V_{OL} – I_{OL}

T_A = +25 °C, V_{CC} = 4.5 V



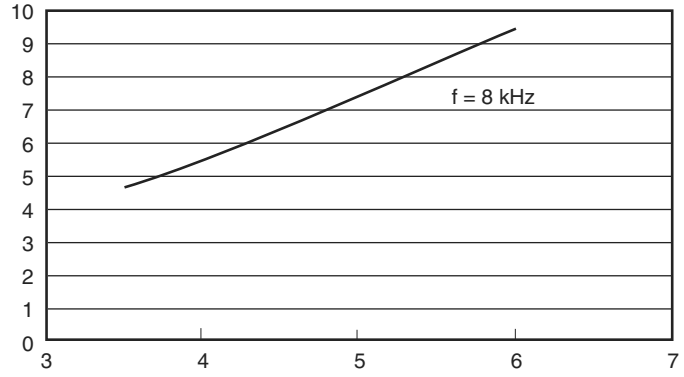
H level input voltage/ L level input voltage
V_{IN} – V_{CC}

T_A = +25 °C



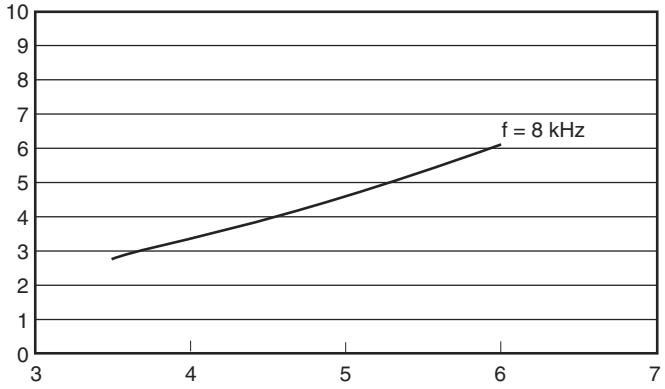
I_{CCLS} – V_{CC}

T_A = +25 °C, In external clock operation
f = Internal operating frequency



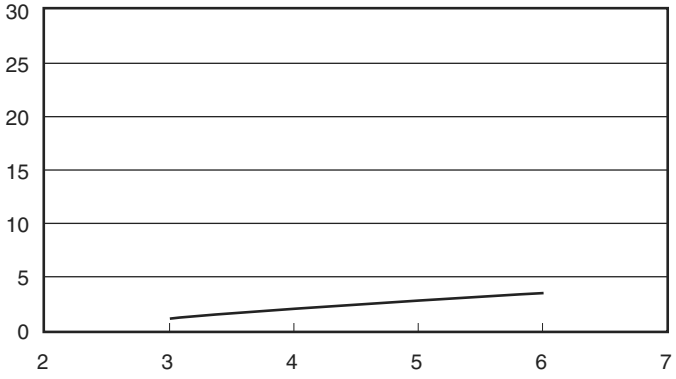
I_{CCT} – V_{CC}

T_A = +25 °C, In external clock operation
f = Internal operating frequency



I_{CCH} – V_{CC}

Stopping, T_A = +25 °C

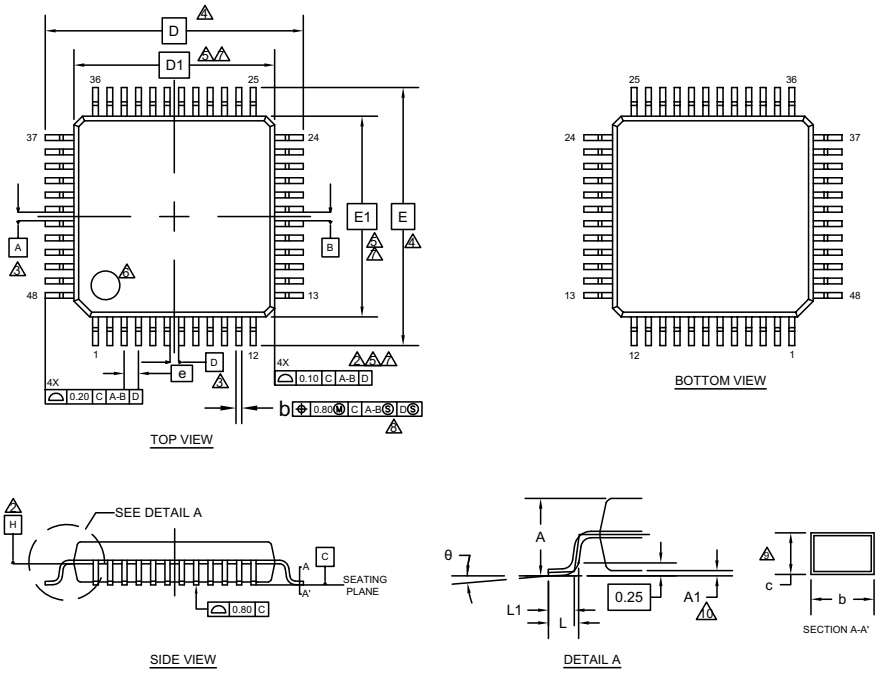


(Continued)

15. Ordering Information

Part Number	Package	Remarks
MB90F387PMT MB90387PMT MB90F387SPMT MB90387SPMT	48-pin plastic LQFP (LQA048)	

16. Package Dimension



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.00	—	0.20
b	0.15	—	0.27
c	0.09	—	0.20
D	9.00 BSC		
D1	7.00 BSC		
e	0.50 BSC		
E	9.00 BSC		
E1	7.00 BSC		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
θ	0°	—	8°

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-13731 **

PACKAGE OUTLINE, 48 LEAD LQFP
7.0X7.0X1.7 MM LQA048 REV**

Document History

Document Title: MB90387/387S/F387/F387S, MB90V495G, 16-bit Microcontrollers F²MC-16LX MB90385 Series Document Number:002-07765				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	—	AKIH	12/19/2008	Migrated to Cypress and assigned document number 002-07765. No change to document contents or format.
*A	6059071	SSAS	02/05/2018	Updated to Cypress template Package: FPT-48P-M26 --> LQA048