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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, SCI, UART/USART
Peripherals	POR, WDT
Number of I/O	36
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90f387spmt-gs-9002

Parameter \ Part Number	MB90F387 MB90F387S	MB90387 MB90387S	MB90V495G
8/10-bit A/D converter	Number of channels: 8 Resolution: Selectable 10-bit or 8-bit. Conversion time: 6.125 μs (at 16 MHz machine clock, including sampling time) Sequential conversion of two or more successive channels is allowed. (Setting a maximum of 8 channels is allowed.) Single conversion mode: Selected channel is converted only once. Sequential conversion mode: Selected channel is converted repetitively. Halt conversion mode: Conversion of selected channel is stopped and activated alternately.		
UART(SCI)	Number of channels: 1 Clock-synchronous transfer: 62.5 kbps to 2 Mbps Clock-asynchronous transfer: 9,615 bps to 500 kbps Communication is allowed by bi-directional serial communication function and master/slave type connection.		
CAN	Compliant with Ver 2.0A and Ver 2.0B CAN specifications. 8 built-in message buffers. Transmission rate of 10 kbps to 1 Mbps (by 16 MHz machine clock) CAN wake-up		

*1: Settings of DIP switch S2 for using emulation pod MB2145-507. For details, see MB2145-507 Hardware Manual (2.7 Power Pin solely for Emulator).

*2: MB90387S, MB90F387S

2. Packages And Product Models

Package	MB90F387, MB90F387S	MB90387, MB90387S
LQA048	◯	◯

◯: Yes ×: No

Note: Refer to Package Dimension for details of the package.

3. Product Comparison

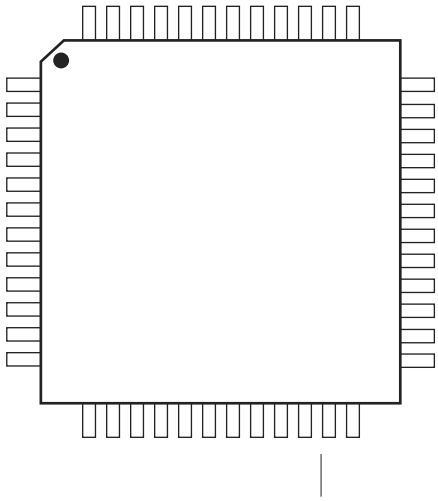
Memory Space

When testing with test product for evaluation, check the differences between the product and a product to be used actually. Pay attention to the following points:

- The MB90V495G has no built-in ROM. However, a special-purpose development tool allows the operations as those of one with built-in ROM. ROM capacity depends on settings on a development tool.
- On MB90V495G, an image from $FF4000_H$ to $FFFFFF_H$ is viewed on 00 bank and an image of $FE0000_H$ to $FF3FFF_H$ is viewed only on FE bank and FF bank. (Modified on settings of a development tool.)
- On MB90F387/F387S/387/387S, an image from $FF4000_H$ to $FFFFFF_H$ is viewed on 00 bank and an image of $FE0000_H$ to $FF3FFF_H$ is viewed only on FF bank.

4. Pin Assignment

(Top View)



(LQA048)

*: MB90387, MB90F387 : X1A, X0A
MB90387S, MB90F387S: P36, P35

Address	Register Abbreviation	Register	Read/ Write	Resource	Initial Value
000083H	(Reserved area) *				
000084H	TCANR	Send cancel register	W	CAN controller	00000000B
000085H	(Reserved area) *				
000086H	TCR	Send completion register	R/W	CAN controller	00000000B
000087H	(Reserved area) *				
000088H	RCR	Receive completion register	R/W	CAN controller	00000000B
000089H	(Reserved area) *				
00008AH	RRTRR	Receive RTR register	R/W	CAN controller	00000000B
00008BH	(Reserved area) *				
00008CH	ROVRR	Receive overrun register	R/W	CAN controller	00000000B
00008DH	(Reserved area) *				
00008EH	RIER	Receive completion interrupt permission register	R/W	CAN controller	00000000B
00008FH to 00009DH	(Reserved area) *				
00009EH	PACSR	Address detection control register	R/W	Address matching detection function	00000000B
00009FH	DIRR	Delay interrupt request generation/ release register	R/W	Delay interrupt generation module	XXXXXXX0B
0000A0H	LPMCR	Lower power consumption mode control register	W,R/W	Lower power consumption mode	00011000B
0000A1H	CKSCR	Clock selection register	R,R/W	Clock	11111100B
0000A2H to 0000A7H	(Reserved area) *				
0000A8H	WDTC	Watchdog timer control register	R,W	Watchdog timer	XXXXX111B
0000A9H	TBTC	Time-base timer control register	R/W,W	Time-base timer	1XX00100B
0000AAH	WTC	Watch timer control register	R,R/W	Watch timer	1X001000B
0000ABH to 0000ADH	(Reserved area) *				
0000AEH	FMCS	Flash memory control status register	R,W,R/W	512k-bit Flash memory	000X0000B
0000AFH	(Reserved area) *				

Address	Register Abbreviation	Register	Read/ Write	Resource	Initial Value
0000B0H	ICR00	Interrupt control register 00	R/W	Interrupt controller	00000111B
0000B1H	ICR01	Interrupt control register 01			00000111B
0000B2H	ICR02	Interrupt control register 02			00000111B
0000B3H	ICR03	Interrupt control register 03			00000111B
0000B4H	ICR04	Interrupt control register 04			00000111B
0000B5H	ICR05	Interrupt control register 05			00000111B
0000B6H	ICR06	Interrupt control register 06			00000111B
0000B7H	ICR07	Interrupt control register 07			00000111B
0000B8H	ICR08	Interrupt control register 08			00000111B
0000B9H	ICR09	Interrupt control register 09			00000111B
0000BAH	ICR10	Interrupt control register 10			00000111B
0000BBH	ICR11	Interrupt control register 11			00000111B
0000BCH	ICR12	Interrupt control register 12			00000111B
0000BDH	ICR13	Interrupt control register 13			00000111B
0000BEH	ICR14	Interrupt control register 14			00000111B
0000BFH	ICR15	Interrupt control register 15			00000111B
0000C0H to 0000FFH	(Reserved area) *				
001FF0H	PADR0	Detection address setting register 0 (low-order)	R/W	Address matching detection function	XXXXXXXXB
001FF1H		Detection address setting register 0 (middle-order)			XXXXXXXXB
001FF2H		Detection address setting register 0 (high-order)			XXXXXXXXB
001FF3H	PADR1	Detection address setting register 1 (low-order)	R/W		XXXXXXXXB
001FF4H		Detection address setting register 1 (middle-order)			XXXXXXXXB
001FF5H		Detection address setting register 1 (high-order)			XXXXXXXXB
003900H	TMR0/ TMRLR0	16-bit timer register 0/16-bit reload register	R,W	16-bit reload timer 0	XXXXXXXXB
003901H					XXXXXXXXB
003902H	TMR1/ TMRLR1	16-bit timer register 1/16-bit reload register	R,W	16-bit reload timer 1	XXXXXXXXB
003903H					XXXXXXXXB
003904H to 00390FH	(Reserved area) *				

Address	Register Abbreviation	Register	Read/ Write	Resource	Initial Value
003C38H, 003C39H	DLCR4	DLC register 4	R/W	CAN controller	XXXXXXXXB, XXXXXXXXB
003C3AH, 003C3BH	DLCR5	DLC register 5	R/W		XXXXXXXXB, XXXXXXXXB
003C3CH, 003C3DH	DLCR6	DLC register 6	R/W		XXXXXXXXB, XXXXXXXXB
003C3EH, 003C3FH	DLCR7	DLC register 7	R/W		XXXXXXXXB, XXXXXXXXB
003C40H to 003C47H	DTR0	Data register 0	R/W		XXXXXXXXB to XXXXXXXXB
003C48H to 003C4FH	DTR1	Data register 1	R/W		XXXXXXXXB to XXXXXXXXB
003C50H to 003C57H	DTR2	Data register 2	R/W		XXXXXXXXB to XXXXXXXXB
003C58H to 003C5FH	DTR3	Data register 3	R/W		XXXXXXXXB to XXXXXXXXB
003C60H to 003C67H	DTR4	Data register 4	R/W		XXXXXXXXB to XXXXXXXXB
003C68H to 003C6FH	DTR5	Data register 5	R/W		XXXXXXXXB to XXXXXXXXB
003C70H to 003C77H	DTR6	Data register 6	R/W		XXXXXXXXB to XXXXXXXXB
003C78H to 003C7FH	DTR7	Data register 7	R/W		XXXXXXXXB to XXXXXXXXB
003C80H to 003CFFH	(Reserved area) *				
003D00H, 003D01H	CSR	Control status register	R/W, R	CAN controller	0XXXX001B, 00XXX000B
003D02H	LEIR	Last event display register	R/W		000XX000B
003D03H	(Reserved area) *				
003D04H, 003D05H	RTEC	Send/receive error counter	R	CAN controller	00000000B, 00000000B
003D06H, 003D07H	BTR	Bit timing register	R/W		11111111B, X1111111B
003D08H	IDER	IDE register	R/W		XXXXXXXXB
003D09H	(Reserved area) *				
003D0AH	TRTRR	Send RTR register	R/W	CAN controller	00000000B
003D0BH	(Reserved area) *				
003D0CH	RFWTR	Remote frame receive wait register	R/W	CAN controller	XXXXXXXXB

Address	Register Abbreviation	Register	Read/ Write	Resource	Initial Value
003D0D$_H$	(Reserved area) *				
003D0E$_H$	TIER	Send completion interrupt permission register	R/W	CAN controller	00000000$_B$
003D0F$_H$	(Reserved area) *				
003D10$_H$, 003D11$_H$	AMSR	Acceptance mask selection register	R/W	CAN controller	XXXXXXXX$_B$, XXXXXXXX$_B$
003D12$_H$, 003D13$_H$	(Reserved area) *				
003D14$_H$ to 003D17$_H$	AMR0	Acceptance mask register 0	R/W	CAN controller	XXXXXXXX$_B$ to XXXXXXXX$_B$
003D18$_H$ to 003D1B$_H$	AMR1	Acceptance mask register 1	R/W		XXXXXXXX$_B$ to XXXXXXXX$_B$
003D1C$_H$ to 003DFF$_H$	(Reserved area) *				
003E00$_H$ to 003EFF$_H$	(Reserved area) *				
003FF0$_H$ to 003FFF$_H$	(Reserved area) *				

Initial values:

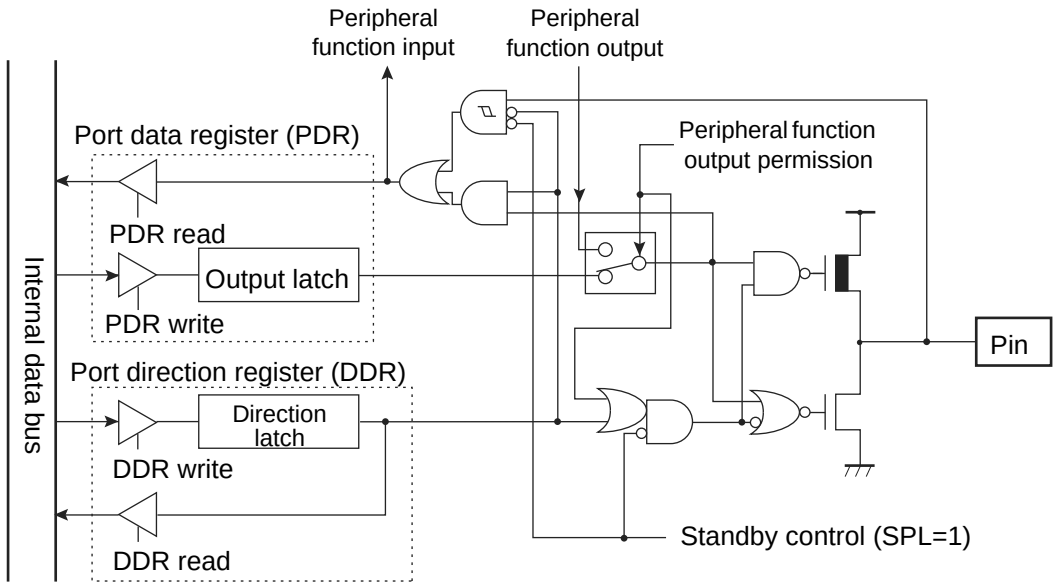
0: Initial value of this bit is “0.”

1: Initial value of this bit is “1.”

X: Initial value of this bit is undefined.

*: “Reserved area” should not be written anything. Result of reading from “Reserved area” is undefined.

Port 3 Pins Block Diagram (general-purpose input/output port)



Standby control: Control among Stop mode (SPL=1), Time-base timer mode (SPL=1), and watch mode (SPL=1).

Port 3 Registers

■ Port 3 registers include port 3 data register (PDR3) and port 3 direction register (DDR3).

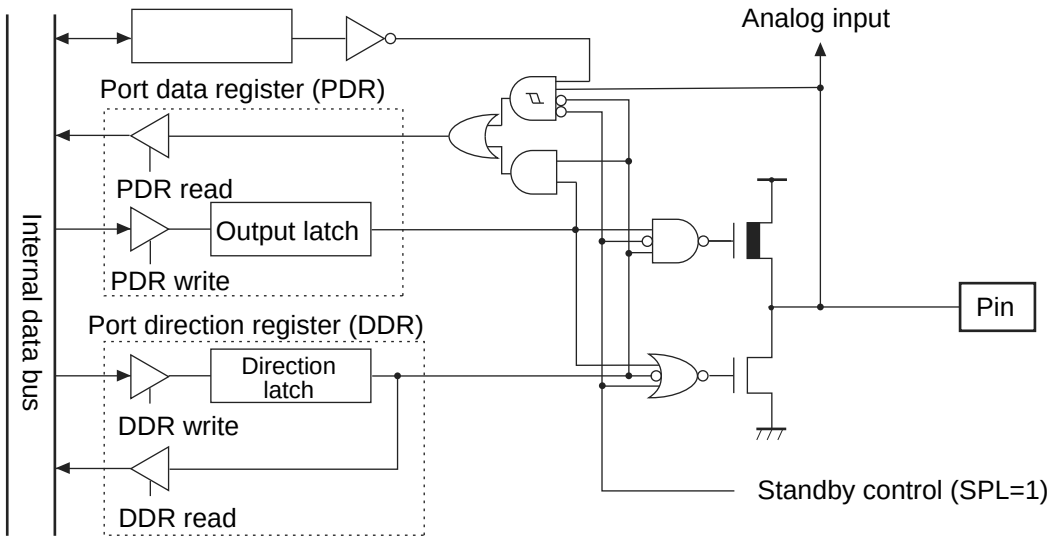
■ The bits configuring the register correspond to port 3 pins on a one-to-one basis.

Relation between Port 3 Registers and Pins

Port Name	Bits of Register and Corresponding Pins								
Port 3	PDR3, DDR3	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	Corresponding pins	P37	P36*	P35*	–	P33	P32	P31	P30

*: P35 and P36 do not exist on MB90387and MB90F387.

Port 5 Pins Block Diagram



Standby control: Control among Stop mode (SPL=1), Time-base timer mode (SPL=1), and watch mode (SPL=1).

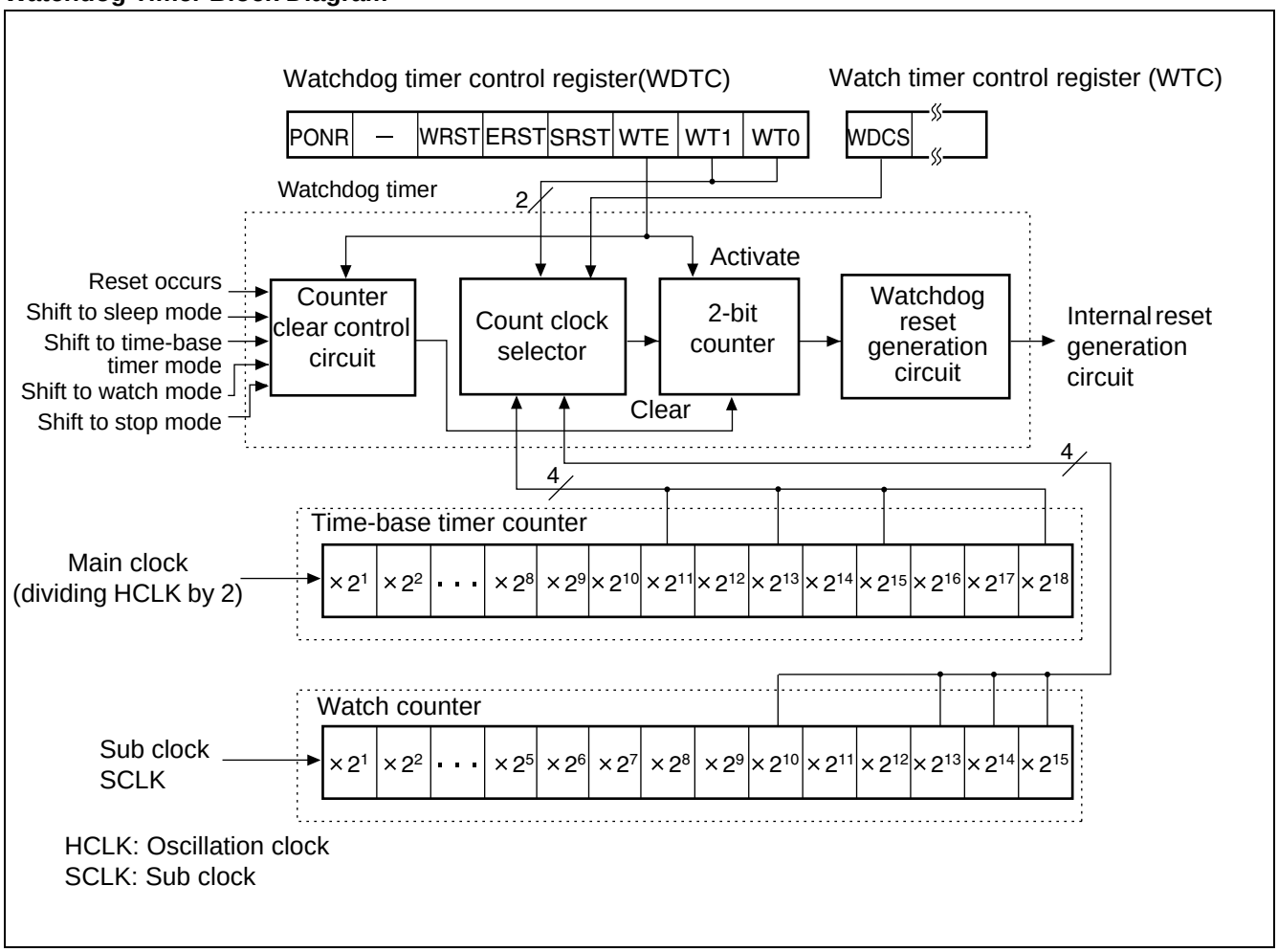
Port 5 Registers

- Port 5 registers include port 5 data register (PDR5), port 5 direction register (DDR5), and analog input permission register (ADER).
- Analog input permission register (ADER) allows or disallows input of analog signal to the analog input pin.
- The bits configuring the register correspond to port 5 pins on a one-to-one basis.

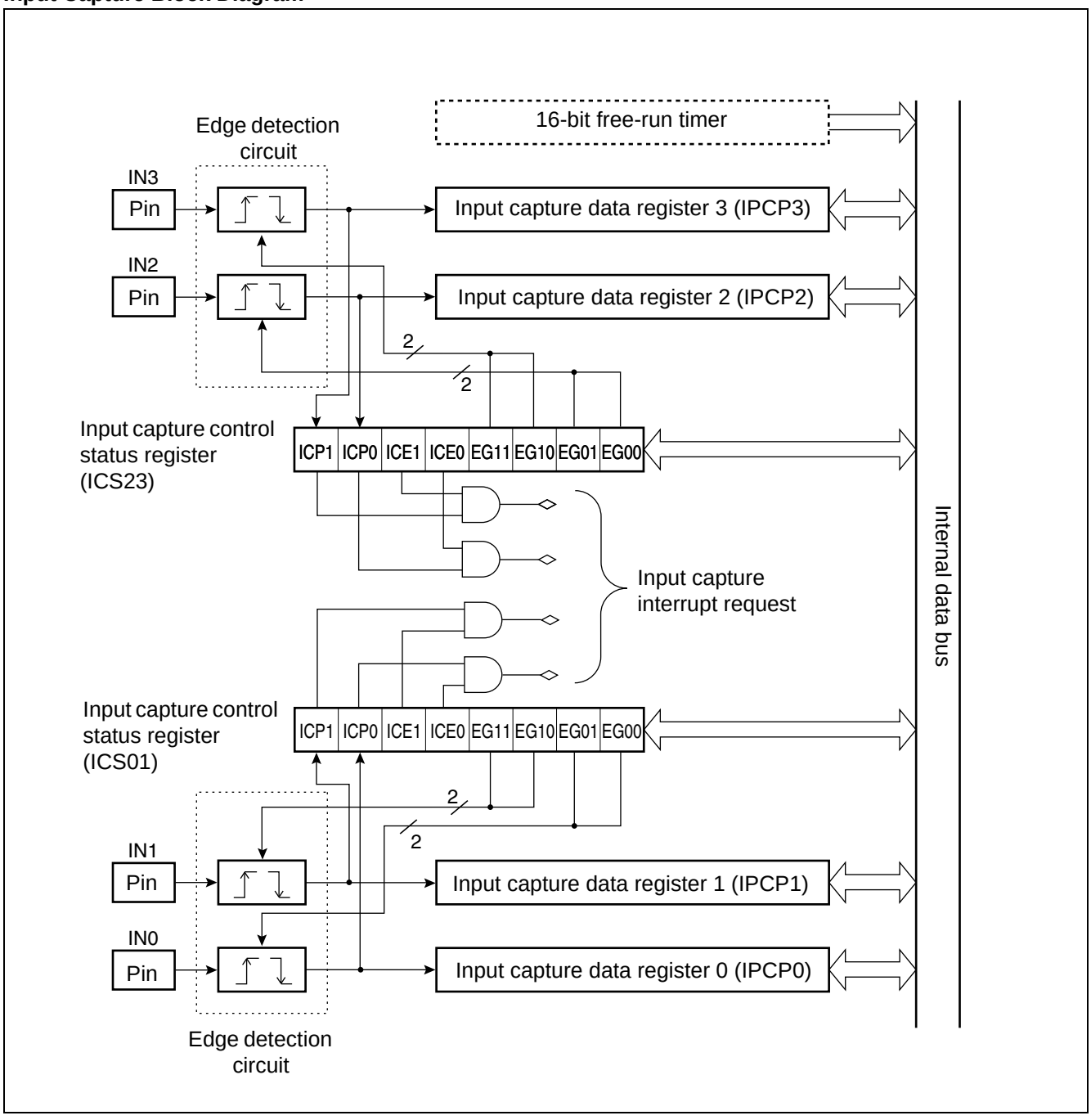
Relation between Port 5 Registers and Pins

Port Name	Bits of Register and Corresponding Pins								
Port 5	PDR5, DDR5	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	ADER	ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0
	Corresponding pins	P57	P56	P55	P54	P53	P52	P51	P50

Watchdog Timer Block Diagram



Input Capture Block Diagram



12.10 8/10-bit A/D Converter

The 8/10-bit A/D converter converts an analog input voltage into 8-bit or 10/bit digital value, using the RC-type successive approximation conversion method.

- Input signal is selected among 8 channels of analog input pins.
- Activation trigger is selected among software trigger, internal timer output, and external trigger.

Functions of 8/10-bit A/D Converter

The 8/10-bit A/D converter converts an analog voltage (input voltage) input to analog input pin into an 8-bit or 10-bit digital value (A/D conversion).

The 8/10-bit A/D converter has the following functions:

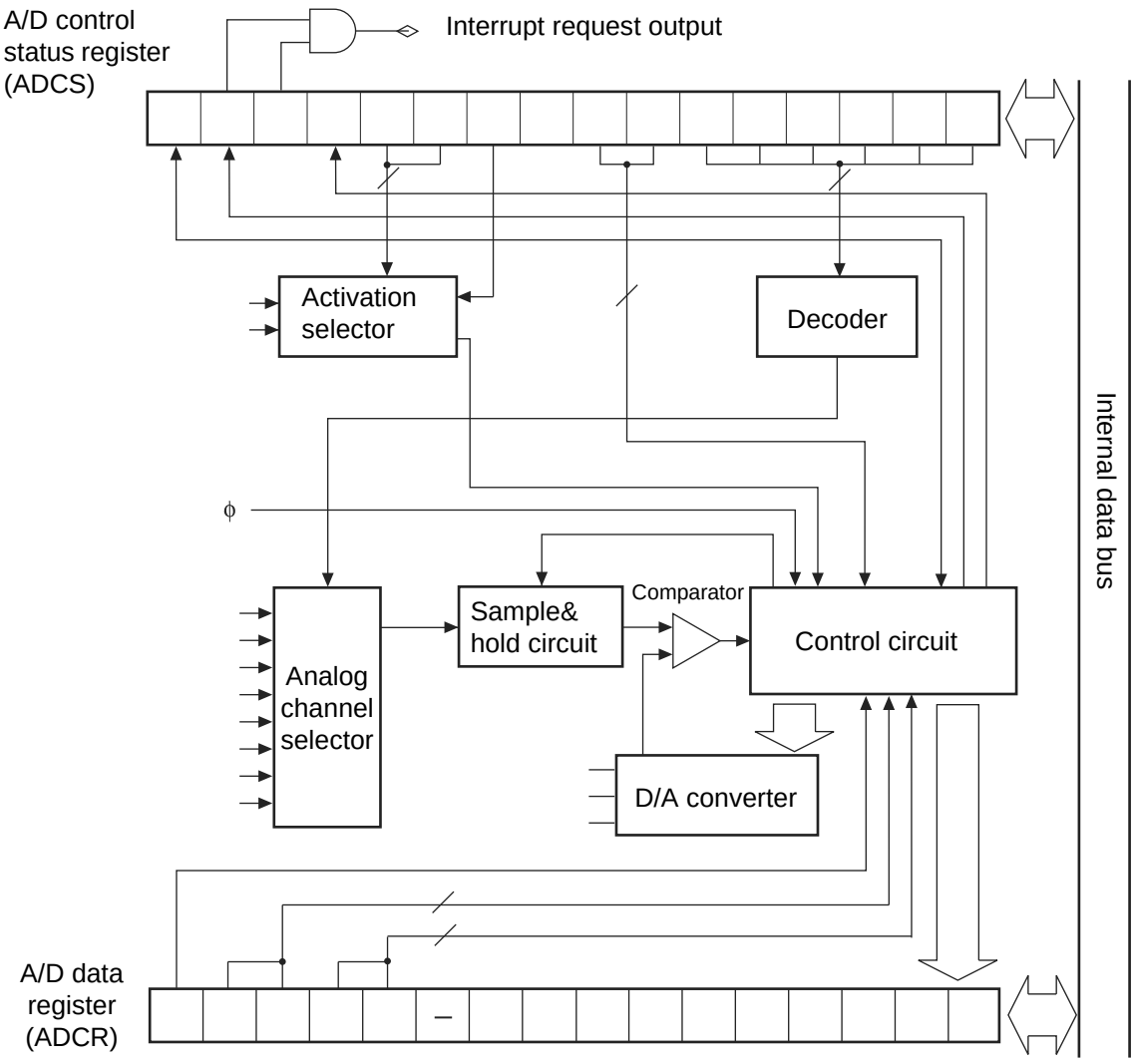
- A/D conversion takes a minimum of 6.12 μs* for 1 channel, including sampling time. (A/D conversion)
- Sampling of one channel takes a minimum of 2.0 μs*.
- RC-type successive approximation conversion method, with sample & hold circuit is used for conversion.
- Resolution of either 8 bits or 10 bits is specifiable.
- A maximum of 8 channels of analog input pins are allowed for use.
- Generation of interrupt request is allowed, by storing A/D conversion result in A/D data register.
- Activation of EI^{2}OS is allowed upon occurrence of an interrupt request. With use of EI^{2}OS, data loss is avoided even if A/D conversion is performed successively.
- An activation trigger is selectable among software trigger, internal timer output, and external trigger (fall edge).

: When operating with 16 MHz machine clock

8/10-bit A/D Converter Conversion Mode

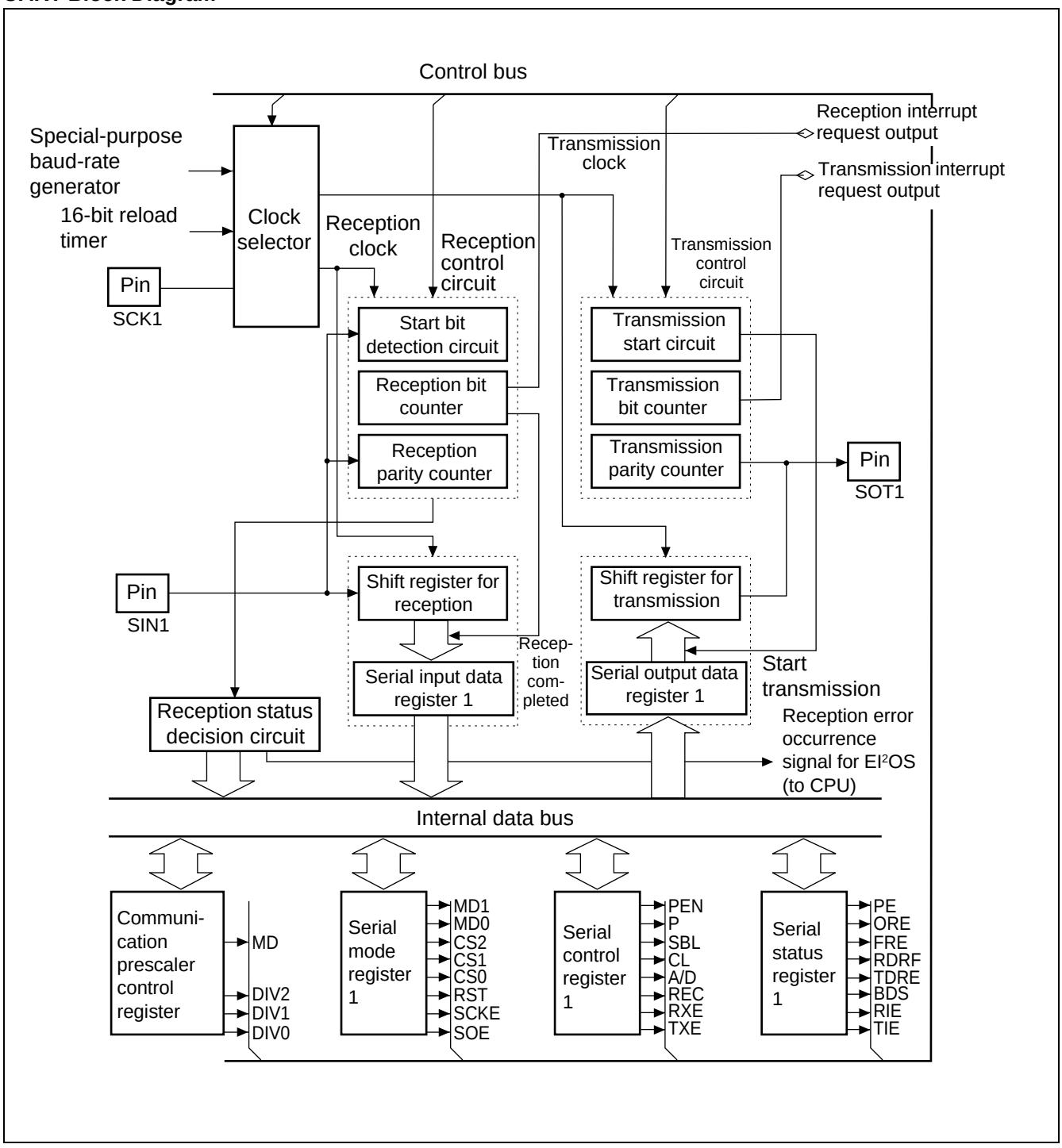
Conversion Mode	Description
Singular conversion mode	The A/D conversion is performed form a start channel to an end channel sequentially. Upon completion of A/D conversion on an end channel, A/D conversion function stops.
Sequential conversion mode	The A/D conversion is performed form a start channel to an end channel sequentially. Upon completion of A/D conversion on an end channel, A/D conversion function resumes from the start channel.
Pausing conversion mode	The A/D conversion is performed by pausing at each channel. Upon completion of A/D conversion on an end channel, A/D conversion and pause functions resume from the start channel.

8/10-bit A/D Converter Block Diagram



TO : Internal timer output
– : Not defined
Reserved: Be sure to set to “0”
ϕ : Machine clock

UART Block Diagram



12.12 CAN Controller

The Controller Area Network (CAN) is a serial communication protocol compliant with CANVer2.0A and Ver2.0B. The protocol allows data transmission and reception in both standard frame format and expanded frame format.

Features of CAN Controller

- CAN controller format is compliant with CANVer2.0A and Ver2.0B.
- The protocol allows data transmission and reception in standard frame format and expanded frame format.
- Automatic transmission of data frame by remote frame reception is allowed.
- Baud rate ranges from 10 kbps to 1 Mbps (with 16-MHz machine clock).

Table 12-5. Data Transmission Baud Rate

Machine Clock	Baud Rate (Max)
16 MHz	1 Mbps
12 MHz	1 Mbps
8 MHz	1 Mbps
4 MHz	500 kbps
2 MHz	250 kbps

- Provided with 8 transmission/reception message buffers.
- Transmission/reception is allowed at ID 11 bit in standard format, and at ID 29 bit in expanded frame format.
- Specifying 0 byte to 8 bytes is allowed in message data.
- Multi-level message buffer configuration is allowed.
- CAN controller has two built-in acceptance masks. Mask settings are independently allowed for the two acceptance masks on reception IDs.
- The two acceptance masks allow reception in standard frame format and expanded frame format.
- For types of masking, all-bit comparison, all-bit masking, and partial masking with acceptance mask register 0/1, are specifiable.

13. Electrical Characteristics

13.1 Absolute Maximum Rating

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	
	AV_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	$V_{CC} = AV_{CC}$*2
	AVR	V_{SS} – 0.3	V_{SS} + 6.0	V	$AV_{CC} \geq AVR$*2
Input voltage*1	V_I	V_{SS} – 0.3	V_{SS} + 6.0	V	*3
Output voltage*1	V_O	V_{SS} – 0.3	V_{SS} + 6.0	V	*3
Maximum clamp current	I_{CLAMP}	– 2.0	+ 2.0	mA	*7
Total maximum clamp current	$\Sigma \mid I_{CLAMP} \mid$	–	20	mA	*7
“L” level maximum output current	I_{OL1}	–	15	mA	Normal output*4
	I_{OL2}	–	40	mA	High-current output*4
“L” level average output current	I_{OLAV1}	–	4	mA	Normal output*5
	I_{OLAV2}	–	30	mA	High-current output*5
“L” level maximum total output current	ΣI_{OL1}	–	125	mA	Normal output
	ΣI_{OL2}	–	160	mA	High-current output
“L” level average total output current	ΣI_{OLAV1}	–	40	mA	Normal output*6
	ΣI_{OLAV2}	–	40	mA	High-current output*6
“H” level maximum output current	I_{OH1}	–	–15	mA	Normal output*4
	I_{OH2}	–	–40	mA	High-current output*4
“H” level average output current	I_{OHAV1}	–	–4	mA	Normal output*5
	I_{OHAV2}	–	–30	mA	High-current output*5
“H” level maximum total output current	ΣI_{OH1}	–	–125	mA	Normal output
	ΣI_{OH2}	–	–160	mA	High-current output
“H” level average total output current	ΣI_{OHAV1}	–	–40	mA	Normal output*6
	ΣI_{OHAV2}	–	–40	mA	High-current output*6
Power consumption	P_D	–	245	mW	
Operating temperature	T_A	–40	+105	°C	
Storage temperature	Tstg	–55	+150	°C	

*1: The parameter is based on $V_{SS} = AV_{SS} = 0.0$ V.

*2: AVcc and AVR should not exceed Vcc.

*3: V_I and V_O should not exceed Vcc + 0.3 V. However if the maximum current to/from an input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating.

*4: A peak value of an applicable one pin is specified as a maximum output current.

*5: An average current value of an applicable one pin within 100 ms is specified as an average output current. (Average value is found by multiplying operating current by operating rate.)

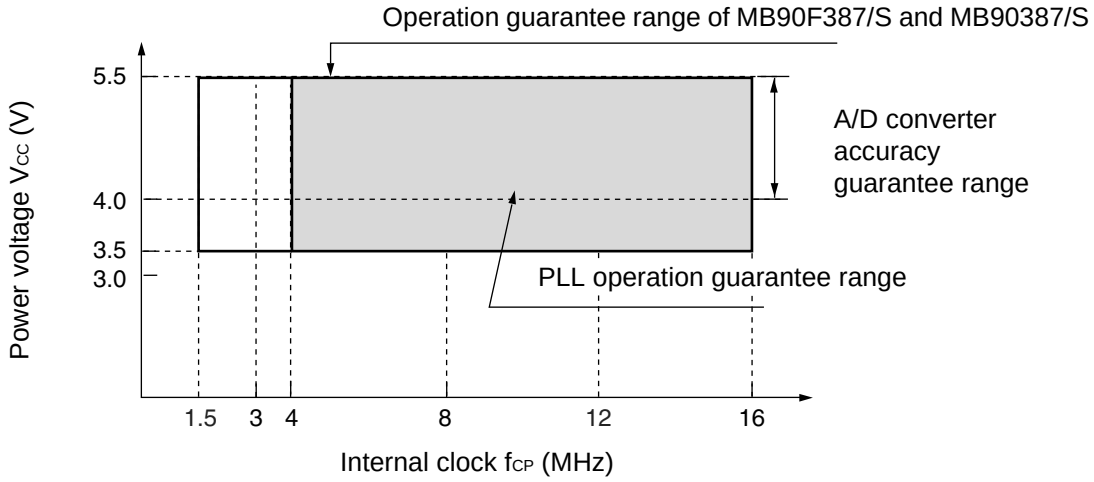
*6: An average current value of all pins within 100 ms is specified as an average total output current. (Average value is found by multiplying operating current by operating rate.)

*7:

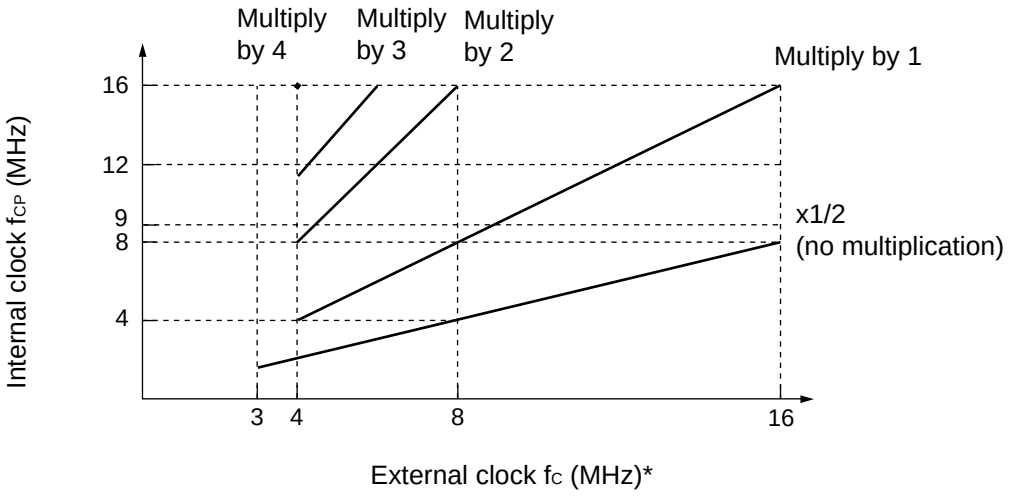
■ Applicable to pins: P10 to P17, P20 to P27, P30 to P33, P35*, P36*, P37, P40 to P44, P50 to P57
*: P35 and P36 are MB90387S and MB90F387S only.

• PLL operation guarantee range

Relation between internal operation clock frequency and power supply voltage



Relation among external clock frequency and internal clock frequency

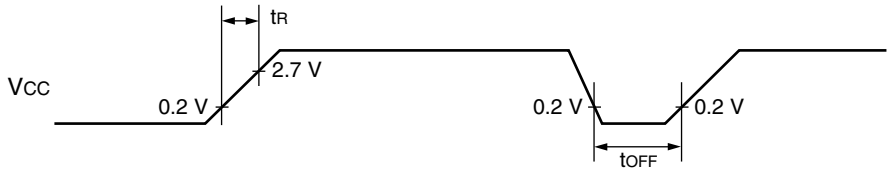


*: fc is 8 MHz at maximum when crystal or ceramic resonator circuit is used.

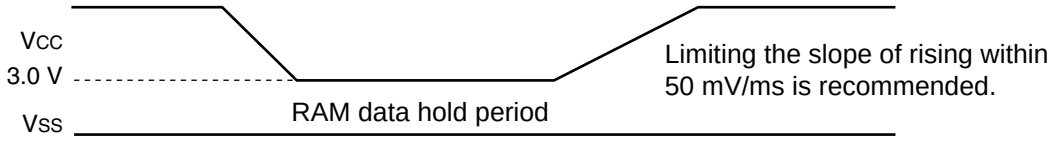
13.4.3 Power-on Reset

(V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Power supply rise time	t_R	V_{CC}	–	0.05	30	ms	
Power supply shutdown time	t_{OFF}	V_{CC}		1	–	ms	Waiting time until power-on

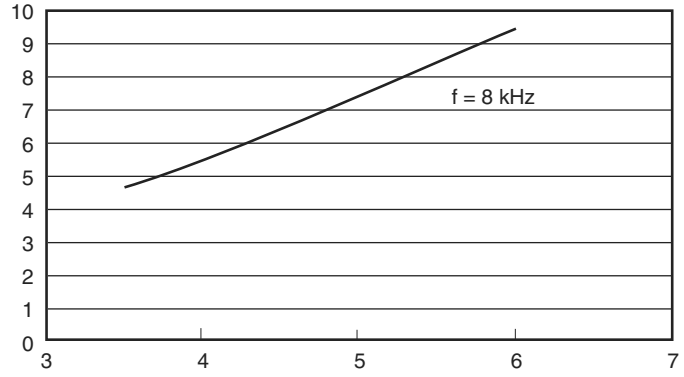


Sudden change of power supply voltage may activate the power-on reset function. When changing power supply voltages during operation, raise the power smoothly by suppressing variation of voltages as shown below. When raising the power, do not use PLL clock. However, if voltage drop is 1V/s or less, use of PLL clock is allowed during operation.



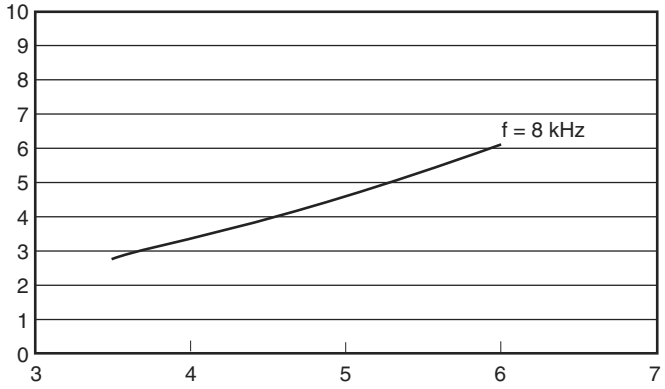
I_{CCLS} – V_{CC}

T_A = +25 °C, In external clock operation
f = Internal operating frequency



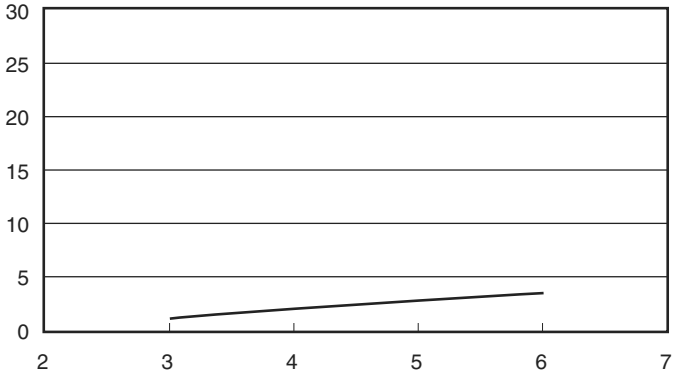
I_{CCT} – V_{CC}

T_A = +25 °C, In external clock operation
f = Internal operating frequency



I_{CCH} – V_{CC}

Stopping, T_A = +25 °C

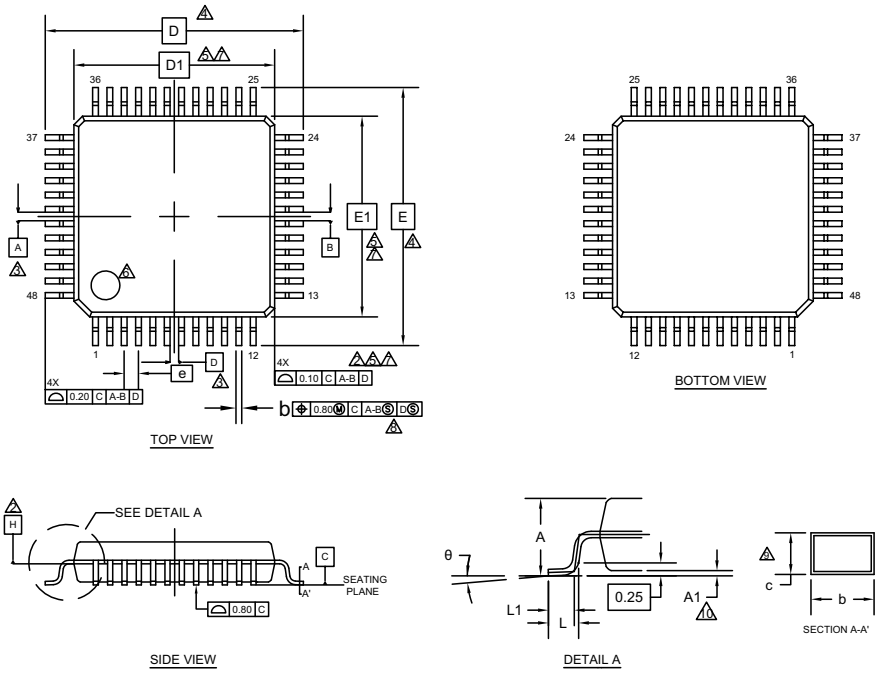


(Continued)

15. Ordering Information

Part Number	Package	Remarks
MB90F387PMT MB90387PMT MB90F387SPMT MB90387SPMT	48-pin plastic LQFP (LQA048)	

16. Package Dimension



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.00	—	0.20
b	0.15	—	0.27
c	0.09	—	0.20
D	9.00 BSC		
D1	7.00 BSC		
e	0.50 BSC		
E	9.00 BSC		
E1	7.00 BSC		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
θ	0°	—	8°

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-13731 **

PACKAGE OUTLINE, 48 LEAD LQFP
7.0X7.0X1.7 MM LQA048 REV**