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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	F ² MC-16LX
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, SCI, UART/USART
Peripherals	POR, WDT
Number of I/O	36
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90f387spmt-gs-n2e1

**DTP/External Interrupt: 4 channels, CAN wakeup:
1 channel**

- Module for activation of expanded intelligent I/O service (EI²OS), and generation of external interrupt.

Delay Interrupt Generator Module

- Generates interrupt request for task switching.

8/10-bit A/D Converter: 8 channels

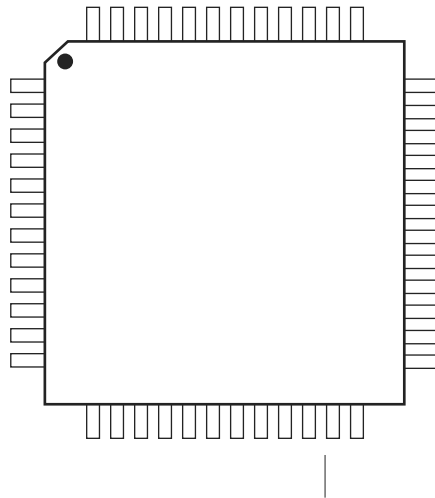
- Resolution is selectable between 8-bit and 10-bit.
- Activation by external trigger input is allowed.
- Conversion time: 6.125 μ s (at 16 MHz machine clock, including sampling time)

Program Patch Function

- Address matching detection for 2 address pointers.

4. Pin Assignment

(Top View)



(LQA048)

*: MB90387, MB90F387 : X1A, X0A
MB90387S, MB90F387S: P36, P35

Notes When Using No Sub Clock

- If an oscillator is not connected to X0A and X1A pin, apply pull-down resistor to X0A pin and leave X1A pin open.

About Power Supply Pins

- If two or more Vcc and Vss pins exist, the pins that should be at the same potential are connected to each other inside the device. For reducing unwanted emissions and preventing malfunction of strobe signals caused by increase of ground level, however, be sure to connect the Vcc and Vss pins to the power source and the ground externally.
- Pay attention to connect a power supply to Vcc and Vss of MB90385 series device in a lowest-possible impedance.
- Near pins of MB90385 series device, connecting a bypass capacitor is recommended at 0.1 μ F across Vcc pin and Vss pin.

Crystal Oscillator Circuit

- Noises around X0 and X1 pins cause malfunctions on a MB90385 series device. Design a print circuit so that X0 and X1 pins, an crystal oscillator (or a ceramic oscillator), and bypass capacitor to the ground become as close as possible to each other. Furthermore, avoid wires to X0 and X1 pins crossing each other as much as possible.
- Print circuit designing that surrounds X0 and X1 pins with grounding wires, which ensures stable operation, is strongly recommended.

Caution on Operations during PLL Clock Mode

- If the PLL clock mode is selected, the microcontroller attempt to be working with the self-oscillating circuit even when there is no external oscillator or external clock input is stopped. Performance of this operation, however, cannot be guaranteed.

Sequence of Turning on Power of A/D Converter and Applying Analog Input

- Be sure to turn on digital power (Vcc) before applying signals to the A/D converter and applying analog input signals (AN0 to AN7 pins).
- Be sure to turn off the power of A/D converter and analog input before turning off the digital power source.
- Be sure not to apply AVR exceeding AVcc when turning on and off. (No problems occur if analog and digital power is turned on and off simultaneously.)

Handling Pins When A/D Converter is Not Used

- If the A/D converter is not used, connect the pins under the following conditions: "AVcc=AVR=Vcc," and "AVss=Vss"

Note on Turning on Power

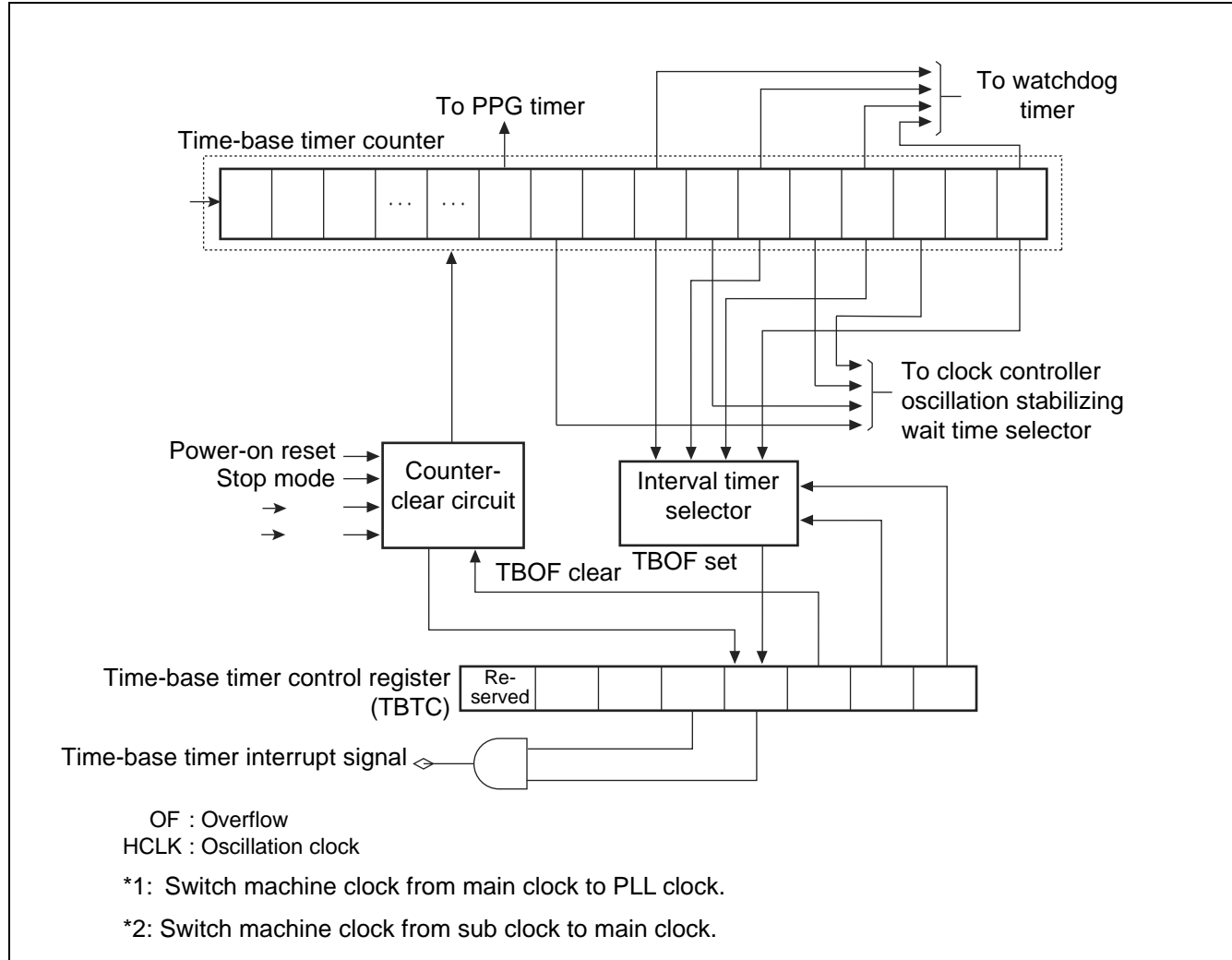
- For preventing malfunctions on built-in step-down circuit, maintain a minimum of 50 μ s of voltage rising time (between 0.2 V and 2.7V) when turning on the power.

Stabilization of Supply Voltage

- A sudden change in the supply voltage may cause the device to malfunction even within the specified Vcc supply voltage operating range. Therefore, the Vcc supply voltage should be stabilized.
For reference, the supply voltage should be controlled so that Vcc ripple variations (peak-to-peak values) at commercial frequencies (50 Hz / 60 Hz) fall below 10% of the standard Vcc supply voltage and the coefficient of fluctuation does not exceed 0.1 V/ms at instantaneous power switching.

Address	Register Abbreviation	Register	Read/Write	Resource	Initial Value
000083 _H	(Reserved area) *				
000084 _H	TCANR	Send cancel register	W	CAN controller	00000000 _B
000085 _H	(Reserved area) *				
000086 _H	TCR	Send completion register	R/W	CAN controller	00000000 _B
000087 _H	(Reserved area) *				
000088 _H	RCR	Receive completion register	R/W	CAN controller	00000000 _B
000089 _H	(Reserved area) *				
00008A _H	RRTRR	Receive RTR register	R/W	CAN controller	00000000 _B
00008B _H	(Reserved area) *				
00008C _H	ROVRR	Receive overrun register	R/W	CAN controller	00000000 _B
00008D _H	(Reserved area) *				
00008E _H	RIER	Receive completion interrupt permission register	R/W	CAN controller	00000000 _B
00008F _H to 00009D _H	(Reserved area) *				
00009E _H	PACSR	Address detection control register	R/W	Address matching detection function	00000000 _B
00009F _H	DIRR	Delay interrupt request generation/release register	R/W	Delay interrupt generation module	XXXXXXX0 _B
0000A0 _H	LPMCR	Lower power consumption mode control register	W,R/W	Lower power consumption mode	00011000 _B
0000A1 _H	CKSCR	Clock selection register	R,R/W	Clock	11111100 _B
0000A2 _H to 0000A7 _H	(Reserved area) *				
0000A8 _H	WDTC	Watchdog timer control register	R,W	Watchdog timer	XXXXX111 _B
0000A9 _H	TBTC	Time-base timer control register	R/W,W	Time-base timer	1XX00100 _B
0000AA _H	WTC	Watch timer control register	R,R/W	Watch timer	1X001000 _B
0000AB _H to 0000AD _H	(Reserved area) *				
0000AE _H	FMCS	Flash memory control status register	R,W,R/W	512k-bit Flash memory	000X0000 _B
0000AF _H	(Reserved area) *				

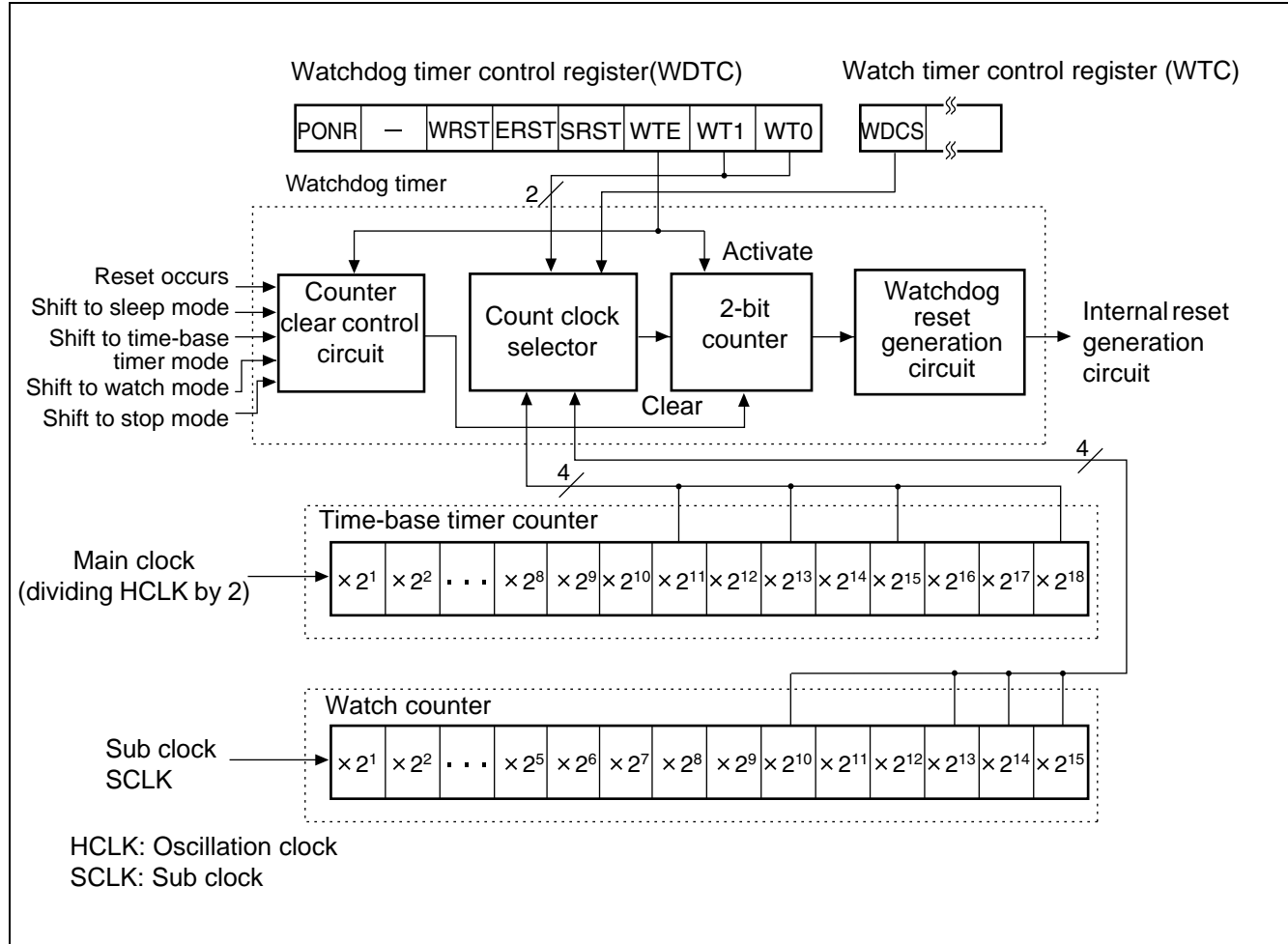
Time-base Timer Block Diagram



Actual interrupt request number of time-base timer is as follows:

Interrupt request number: #16 (10H)

Watchdog Timer Block Diagram



12.4 16-bit Input/Output Timer

The 16-bit input/output timer is a compound module composed of 16-bit free-run timer, (1 unit) and input capture (2 units, 4 input pins). The timer, using the 16-bit free-run timer as a basis, enables measurement of clock cycle of an input signal and its pulse width.

Configuration of 16-bit Input/Output Timer

The 16-bit input/output timer is composed of the following modules:

- 16-bit free-run timer (1 unit)
- Input capture (2 units, 2 input pins per unit)

Functions of 16-bit Input/Output Timer

Functions of 16-bit Free-run Timer

The 16-bit free-run timer is composed of 16-bit up counter, timer counter control status register, and prescaler. The 16-bit up counter increments in synchronization with dividing ratio of machine clock.

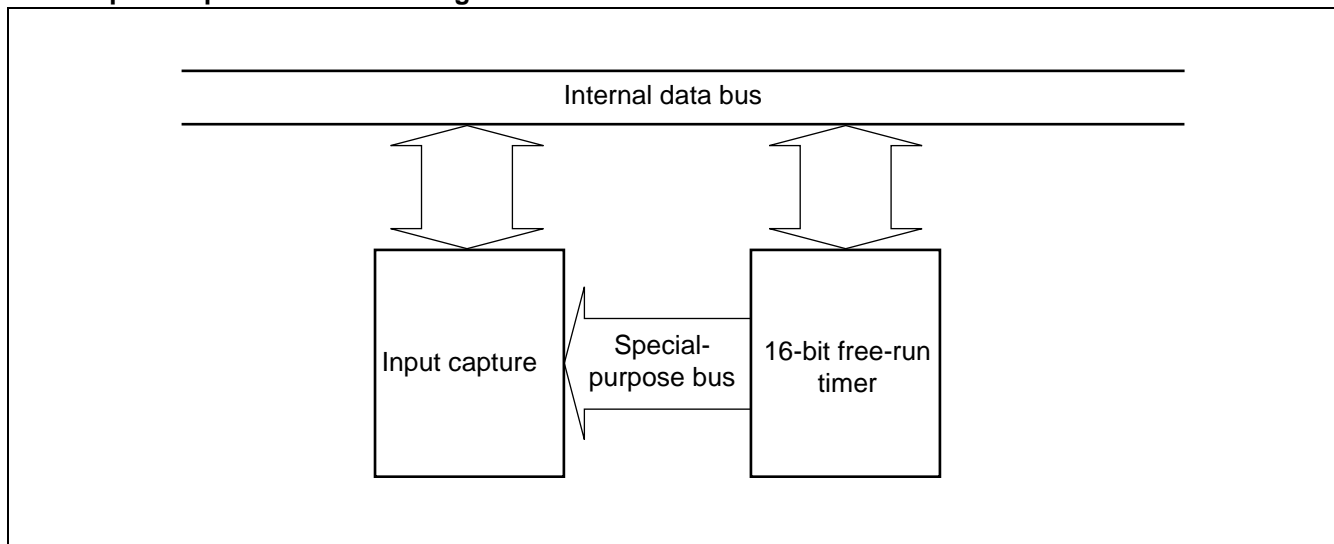
- Count clock is set among four types of machine clock dividing rates.
- Generation of interrupt is allowed by counter value overflow.
- Activation of expanded intelligent I/O service (EI²OS) is allowed by interrupt generation.
- Counter value of 16-bit free-run timer is cleared to "0000_H" by either resetting or software-clearing with timer count clear bit (TCCS: CLR).
- Counter value of 16-bit free-run timer is output to input capture, which is available as base time for capture operation.

Functions of Input Capture

The input capture, upon detecting an edge of a signal input to the input pin from external device, stores a counter value of 16-bit free-run timer at the time of detection into the input capture data register. The function includes the input capture data registers corresponding to four input pins, input capture control status register, and edge detection circuit.

- Rising edge, falling edge, and both edges are selectable for detection.
- Generating interrupt on CPU is allowed by detecting an edge of input signal.
- Expanded intelligent I/O service (EI²OS) is activated by interrupt generation.
- The four input capture input pins and input capture data registers allows monitoring of a maximum of four events.

16-bit Input/Output Timer Block Diagram



12.5 16-bit Reload Timer

The 16-bit reload timer has the following functions:

- Count clock is selectable among 3 internal clocks and external event clock.
- Activation trigger is selectable between software trigger and external trigger.
- Generation of CPU interrupt is allowed upon occurrence of underflow on 16-bit timer register. Available as an interval timer using the interrupt function.
- When underflow of 16-bit timer register (TMR) occurs, one of two reload modes is selectable between one-shot mode that halts counting operation of TMR, and reload mode that reloads 16-bit reload register value to TMR, continuing TMR counting operation.
- The 16-bit reload timer is ready for expanded intelligent I/O service (EI²OS).
- MB90385 series device has 2 channels of built-in 16-bit reload timer.

Operation Mode of 16-bit Reload Timer

Count Clock	Activation Trigger	Operation upon Underflow
Internal clock mode	Software trigger, external trigger	One-shot mode, reload mode
Event count mode	Software trigger	One-shot mode, reload mode

Internal Clock Mode

- The 16-bit reload timer is set to internal clock mode, by setting count clock selection bit (TMCSR: CSL1, CSL0) to "00_b", "01_b", "10_b".
- In the internal clock mode, the counter decrements in synchronization with the internal clock.
- Three types of count clock cycles are selectable by count clock selection bit (TMCSR: CSL1, CSL0) in timer control status register.
- Edge detection of software trigger or external trigger is specified as an activation trigger.

12.6 Watch Timer Outline

The watch timer is a 15-bit free-run counter that increments in synchronization with sub clock.

- Interval time is selectable among 7 choices, and generation of interrupt request is allowed for each interval.
- Provides operation clock to the subclock oscillation stabilizing wait timer and watchdog timer.
- Always uses subclock as a count clock regardless of settings of clock selection register (CKSCR).

Interval Timer Function

- In the watch timer, a bit corresponding to the interval time overflows (carry-over) when an interval time, which is specified by interval time selection bit, is reached. Then overflow flag bit is set (WTC: WTOF=1).
- If an interrupt by overflow is permitted (WTC: WTIE=1), an interrupt request is generated upon setting an overflow flag bit.
- Interval time of watch timer is selectable among the following seven choices:

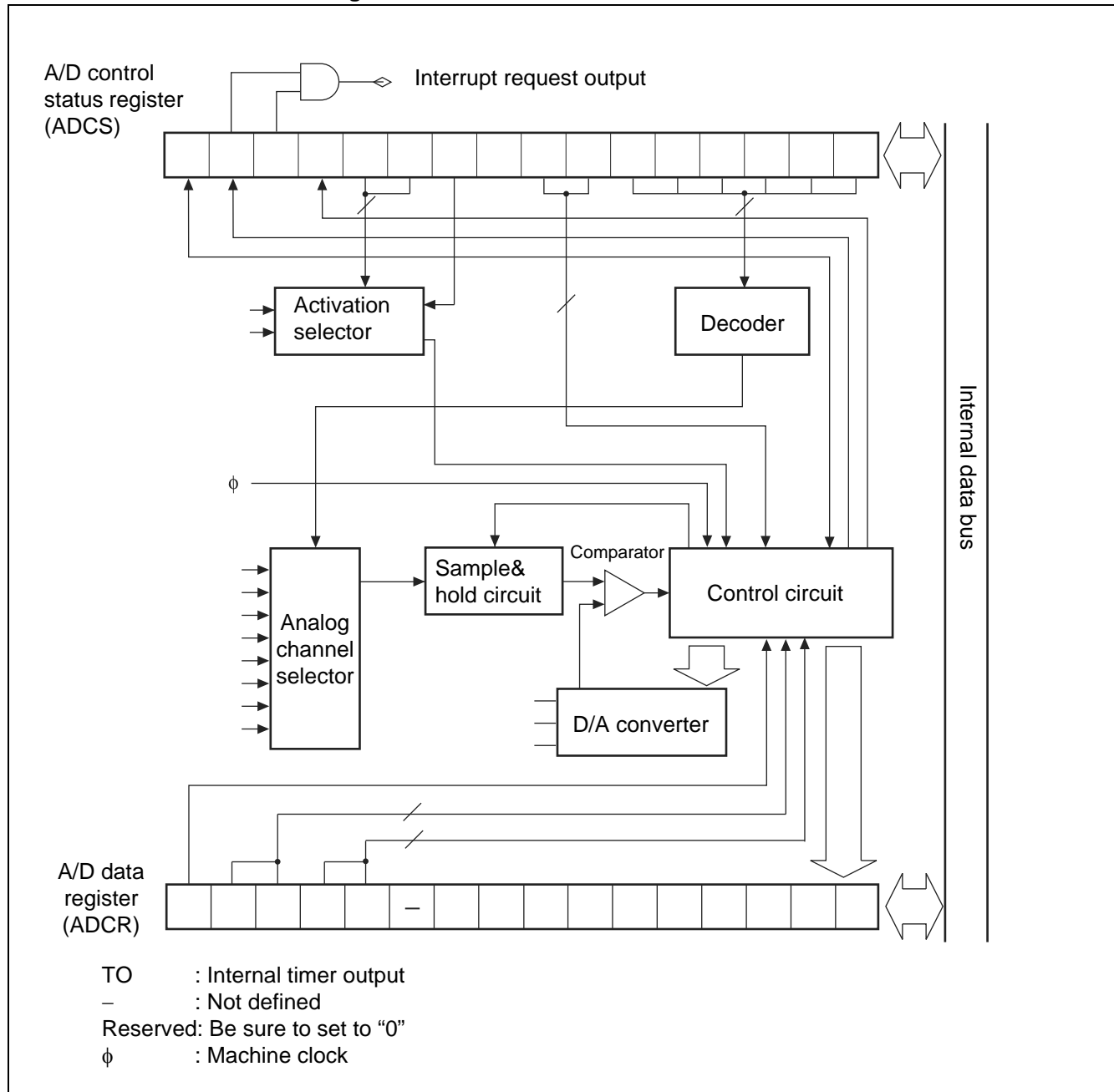
Interval Time of Watch Timer

Sub Clock Cycle	Interval Time
1/SCLK (122 μ s)	2^8 /SCLK (31.25 ms)
	2^9 /SCLK (62.5 ms)
	2^{10} /SCLK (125 ms)
	2^{11} /SCLK (250 ms)
	2^{12} /SCLK (500 ms)
	2^{13} /SCLK (1.0 s)
	2^{14} /SCLK (2.0 s)

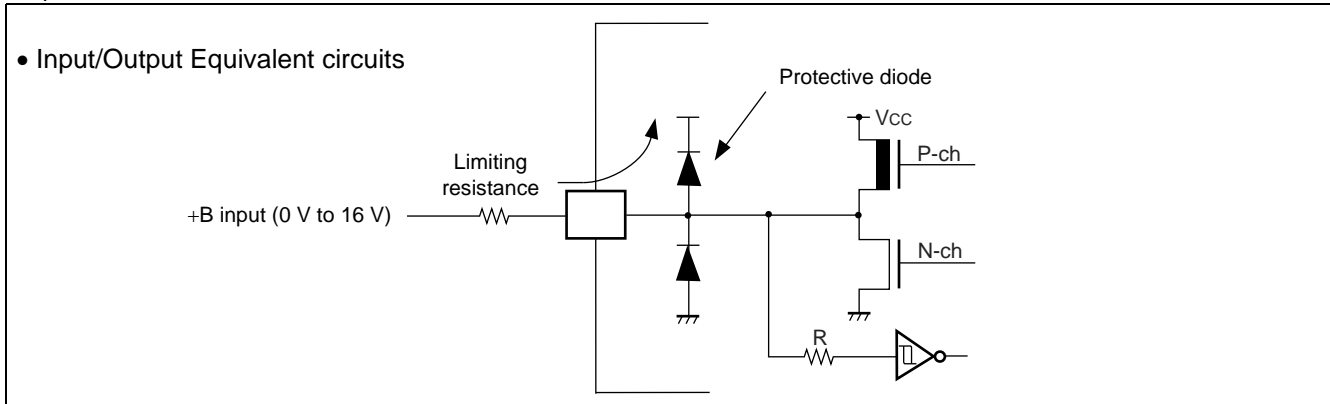
SCLK: Sub clock frequency

Values in parentheses “()” are calculation when operating with 8.192 kHz clock.

8/10-bit A/D Converter Block Diagram



- Use within recommended operating conditions.
- Use at DC voltage (current).
- The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on reset.
- Care must be taken not to leave the +B input pin open.
- Note that analog system input/output pins other than the A/D input pins (LCD drive pins, comparator input pins, etc.) cannot accept +B signal input.
- Sample recommended circuits:



WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

13.4 AC Characteristics

13.4.1 Clock Timing

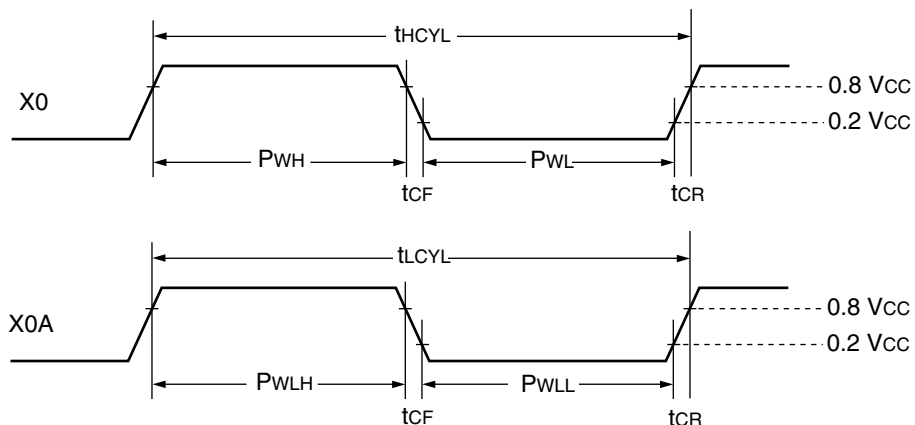
($V_{CC} = 5.0 \text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0 \text{ V}$, $T_A = -40 \text{ }^\circ\text{C}$ to $+105 \text{ }^\circ\text{C}$)

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_c	X0, X1	3	—	8	MHz	When crystal or ceramic resonator is used*2
			3	—	16	MHz	External clock input*1, *2
			4	—	16	MHz	PLL Multiply by 1 *2
			4	—	8	MHz	PLL Multiply by 2 *2
			4	—	5.33	MHz	PLL Multiply by 3 *2
			4	—	4	MHz	PLL Multiply by 4 *2
Clock cycle time	f_{CL}	X0A, X1A	—	32.768	—	kHz	
	t_{HCYL}	X0, X1	125	—	333	ns	
	t_{LCYL}	X0A, X1A	—	30.5	—	μs	
Input clock pulse width	P_{WH}, P_{WL}	X0	10	—	—	ns	Set duty factor at 30% to 70% as a guideline.
	P_{WLH}, P_{WLL}	X0A	—	15.2	—	μs	
Input clock rise time and fall time	t_{CR}, t_{CF}	X0	—	—	5	ns	When external clock is used
Internal operation clock frequency	f_{CP}	—	1.5	—	16	MHz	When main clock is used
	f_{LCP}	—	—	8.192	—	kHz	When sub clock is used
Internal operation clock cycle time	t_{CP}	—	62.5	—	666	ns	When main clock is used
	t_{LCP}	—	—	122.1	—	μs	When sub clock is used

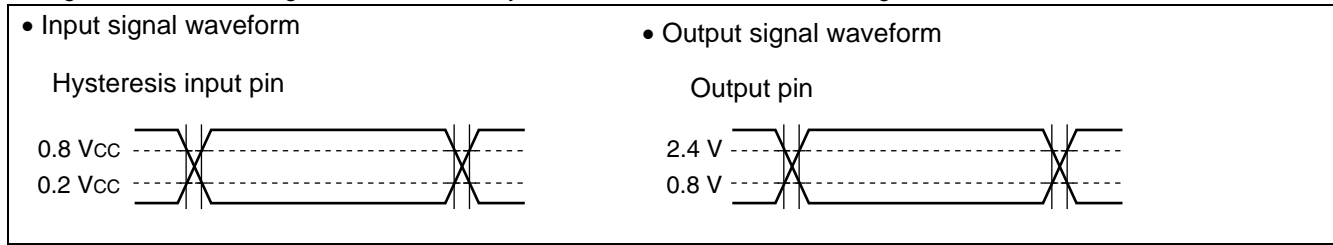
*1: Internal operation clock frequency should not exceed 16 MHz.

*2: When selecting the PLL clock, the range of clock frequency is limited. Use this product within range as mentioned in “Relation among external clock frequency and internal clock frequency”.

• Clock timing



Rating values of alternating current is defined by the measurement reference voltage values shown below:



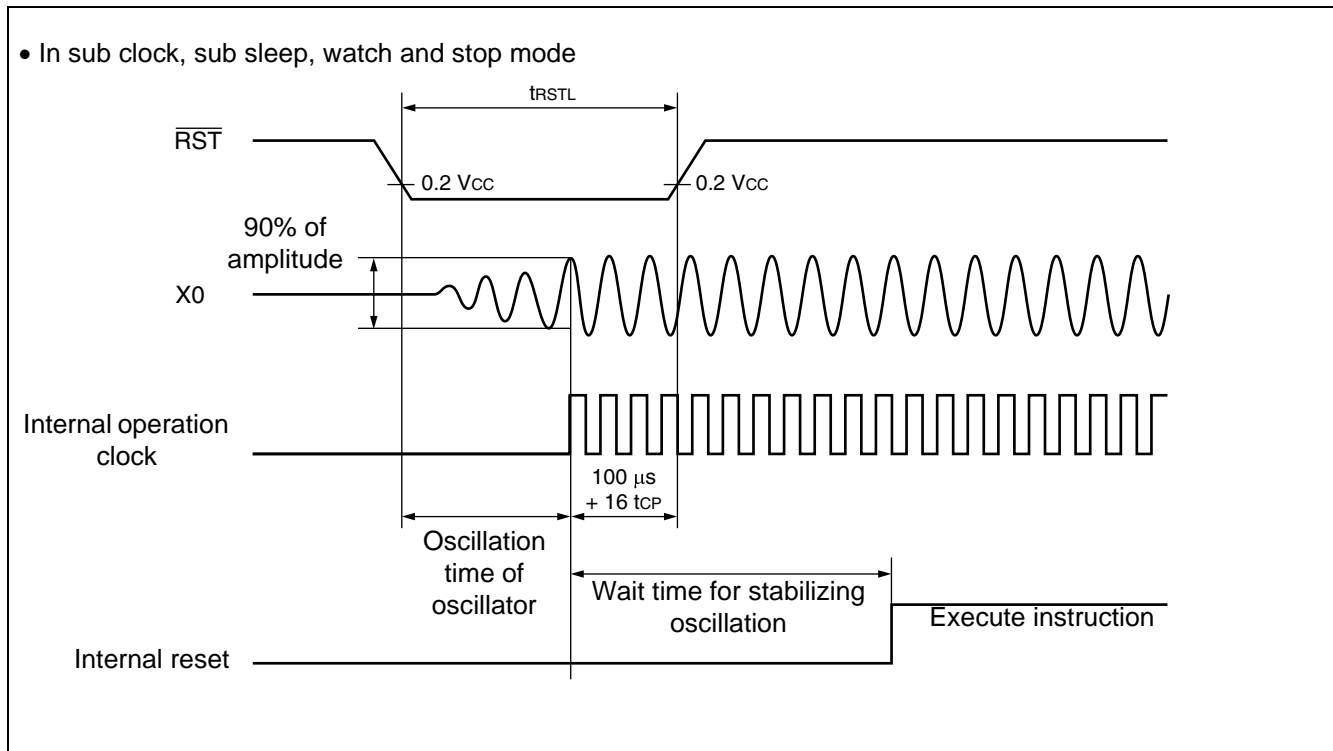
13.4.2 Reset Input Timing

Parameter	Symbol	Pin Name	Value		Unit	Remarks
			Min	Max		
Reset input time	trSTL	RST	16 tCP*3	—	ns	Normal operation
			Oscillation time of oscillator*1 + 100 μs + 16 tCP*3	—	—	In sub clock*2, sub sleep*2, watch*2 and stop mode
			100	—	μs	In timebase timer

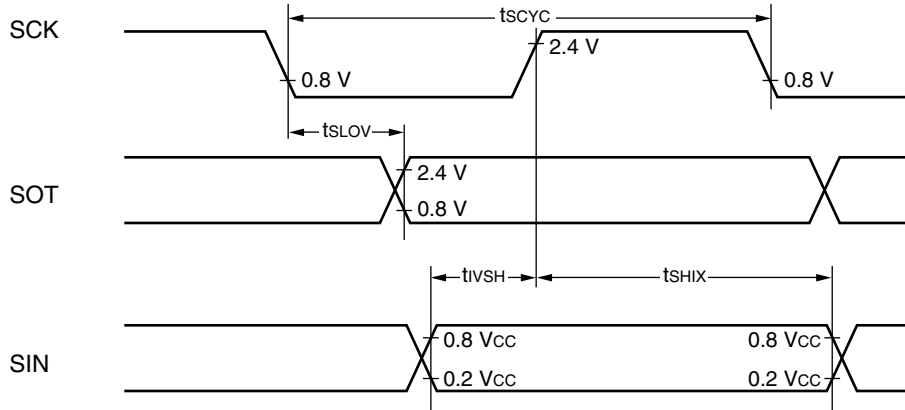
*1: Oscillation time of oscillator is time that the amplitude reached the 90%. In the crystal oscillator, the oscillation time is between several ms to tens of ms. In ceramic oscillator, the oscillation time is between hundreds of μs to several ms. In the external clock, the oscillation time is 0 ms.

*2: Except for MB90F387S and MB90387S.

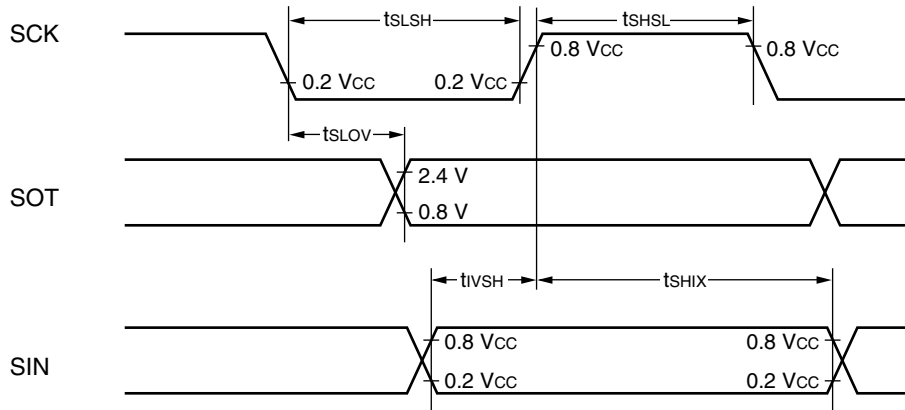
*3: Refer to "(1) Clock timing" ratings for tCP (internal operation clock cycle time).



• Internal shift clock mode



• External shift clock mode



13.4.5 Timer Input Timing

($V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$, $V_{SS} = 0.0 \text{ V}$, $T_A = -40 \text{ }^{\circ}\text{C to } +105 \text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH}	TIN0, TIN1	—	$4 t_{CP}^*$	—	ns	
	t_{TIWL}	IN0 to IN3					

*: Refer to Clock Timing ratings for t_{CP} (internal operation clock cycle time).

13.5 A/D Converter

($V_{CC} = AV_{CC} = 4.0 \text{ V to } 5.5 \text{ V}$, $V_{SS} = AV_{SS} = 0.0 \text{ V}$, $3.0 \text{ V} \leq AVR - AV_{SS}$, $T_A = -40 \text{ }^\circ\text{C to } +105 \text{ }^\circ\text{C}$)

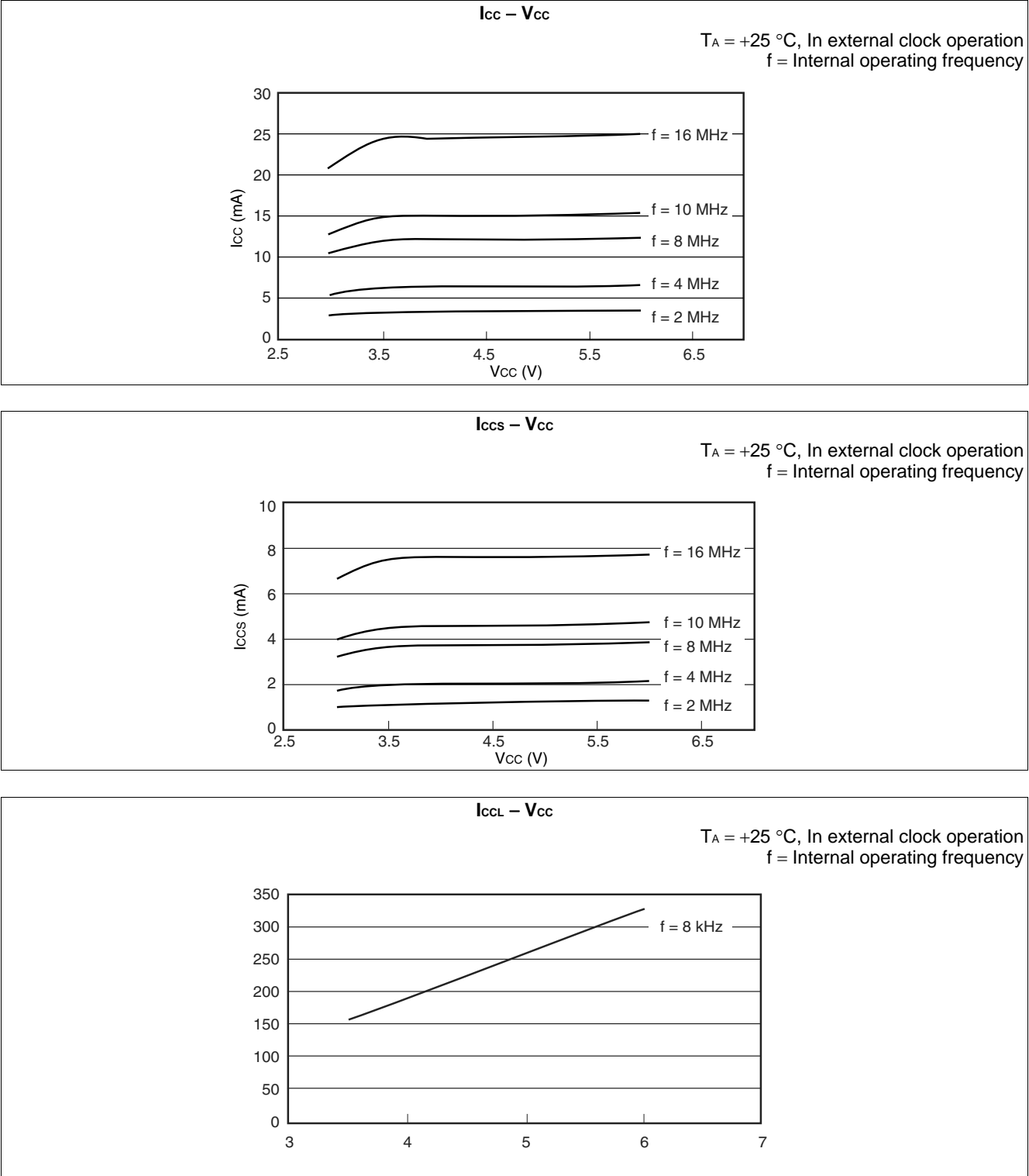
Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Total error	—	—	—	—	± 3.0	LSB	
Nonlinear error	—	—	—	—	± 2.5	LSB	
Differential linear error	—	—	—	—	± 1.9	LSB	
Zero transition voltage	V_{OT}	AN0 to AN7	$AV_{SS} - 1.5 \text{ LSB}$	$AV_{SS} + 0.5 \text{ LSB}$	$AV_{SS} + 2.5 \text{ LSB}$	V	1 LSB = $(AVR - AV_{SS}) / 1024$
Full-scale transition voltage	V_{FST}	AN0 to AN7	$AVR - 3.5 \text{ LSB}$	$AVR - 1.5 \text{ LSB}$	$AVR + 0.5 \text{ LSB}$	V	
Compare time	—	—	66 t_{CP}^{*1}	—	—	ns	With 16 MHz machine clock $5.5 \text{ V} \geq AV_{CC} \geq 4.5 \text{ V}$
			88 t_{CP}^{*1}	—	—	ns	With 16 MHz machine clock $4.5 \text{ V} > AV_{CC} \geq 4.0 \text{ V}$
Sampling time	—	—	32 t_{CP}^{*1}	—	—	ns	With 16 MHz machine clock $5.5 \text{ V} \geq AV_{CC} \geq 4.5 \text{ V}$
			128 t_{CP}^{*1}	—	—	ns	With 16 MHz machine clock $4.5 \text{ V} > AV_{CC} \geq 4.0 \text{ V}$
Analog port input current	I_{AIN}	AN0 to AN7	—	—	10	μA	
Analog input voltage	V_{AIN}	AN0 to AN7	AV_{SS}	—	AVR	V	
Reference voltage	—	AVR	$AV_{SS} + 2.7$	—	AV_{CC}	V	
Power supply current	I_A	AV_{CC}	—	3.5	7.5	mA	
	I_{AH}	AV_{CC}	—	—	5	μA	*2
Reference voltage supplying current	I_R	AVR	—	165	250	μA	
	I_{RH}	AVR	—	—	5	μA	*2
Variation among channels	—	AN0 to AN7	—	—	4	LSB	

*1: Refer to Clock Timing on AC Characteristics.

*2: If A/D converter is not operating, a current when CPU is stopped is applicable ($V_{CC}=AV_{CC}=AVR=5.0 \text{ V}$).

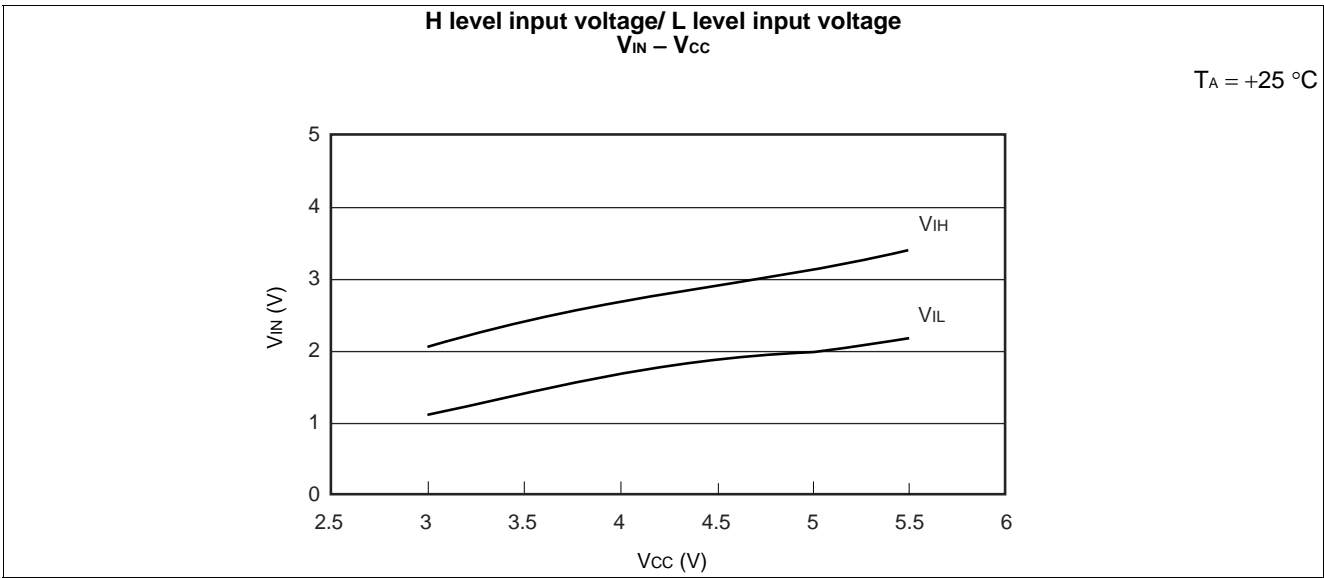
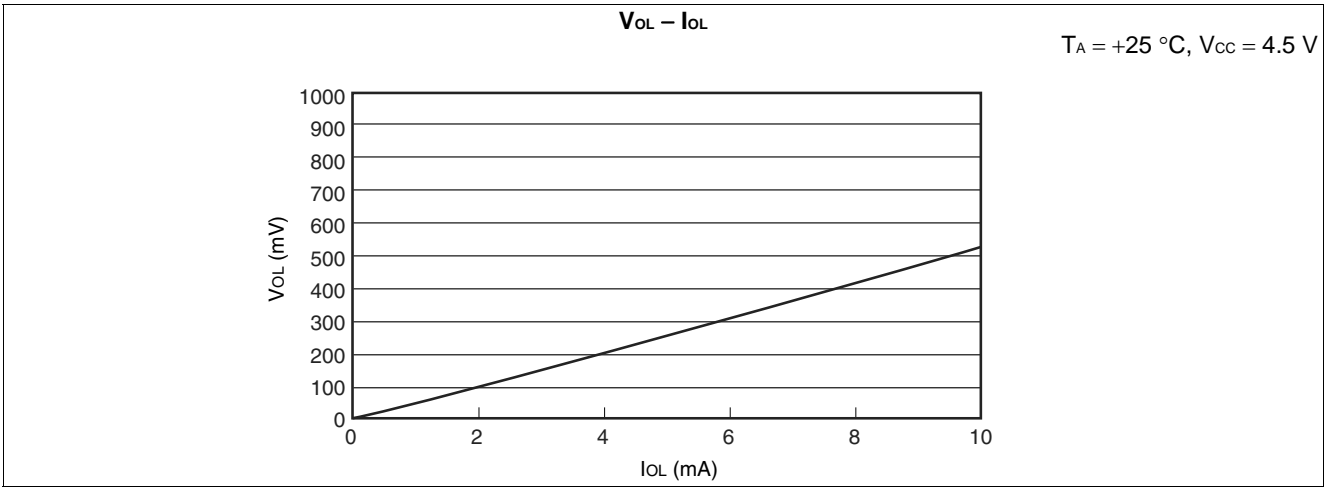
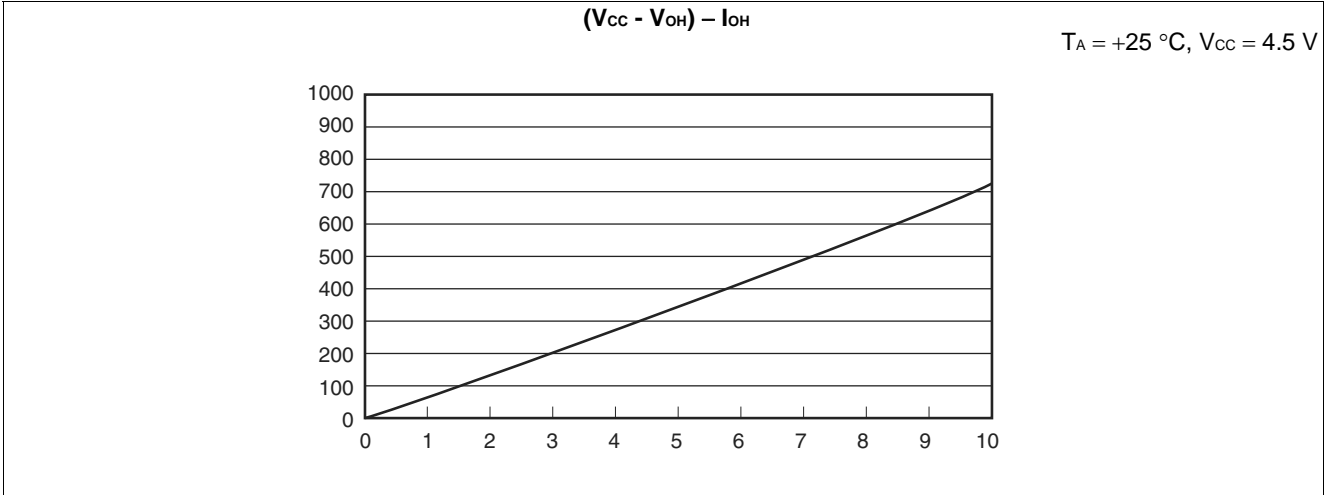
14. Example Characteristics

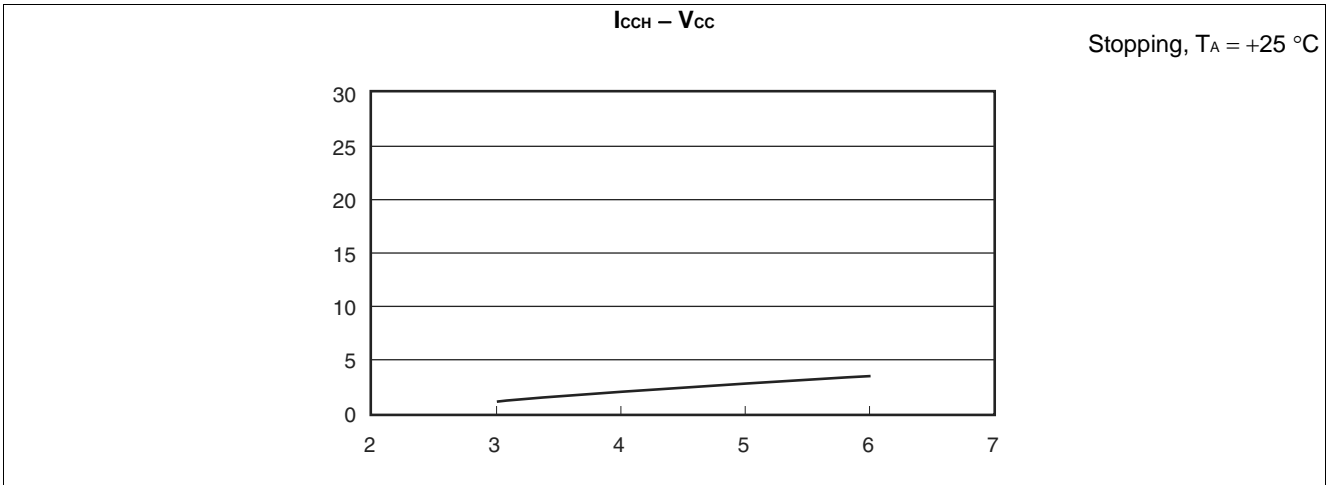
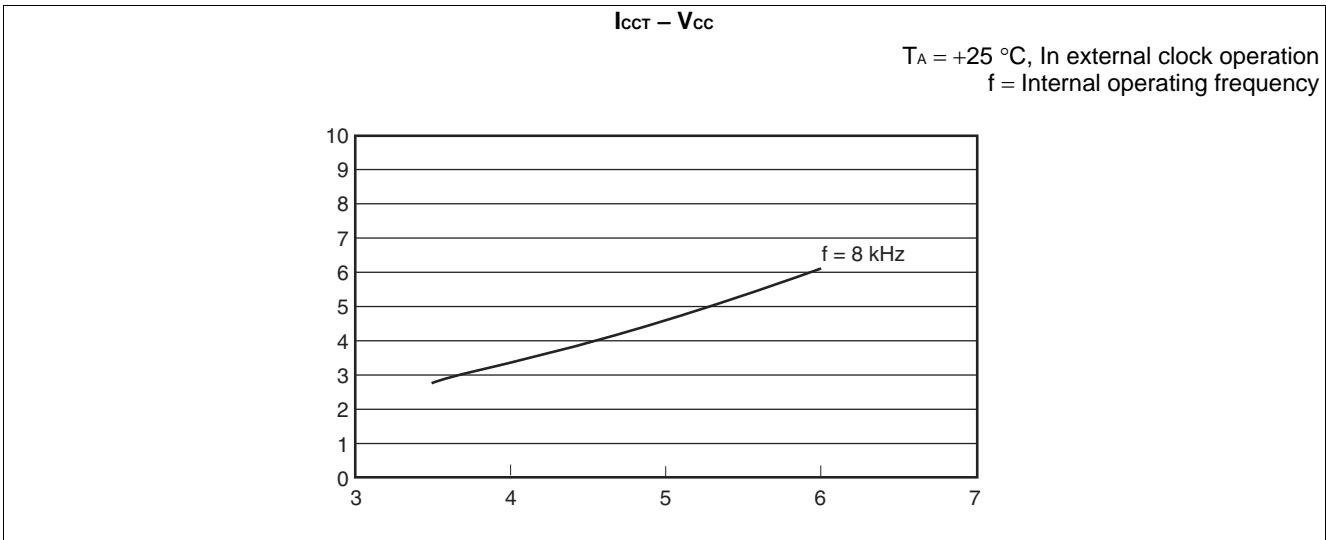
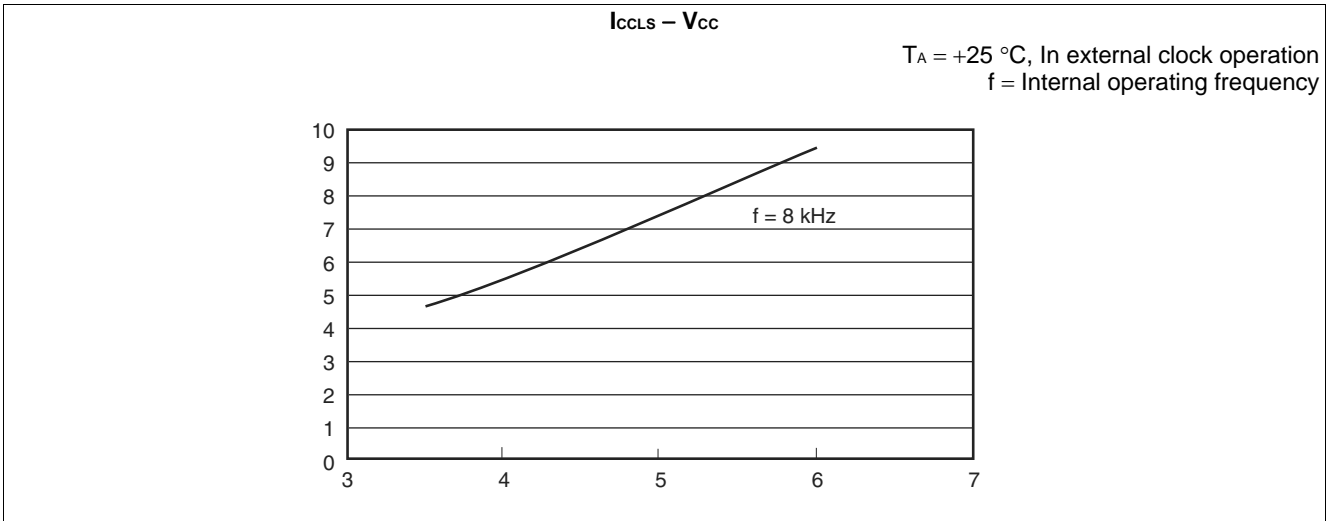
MB90F387



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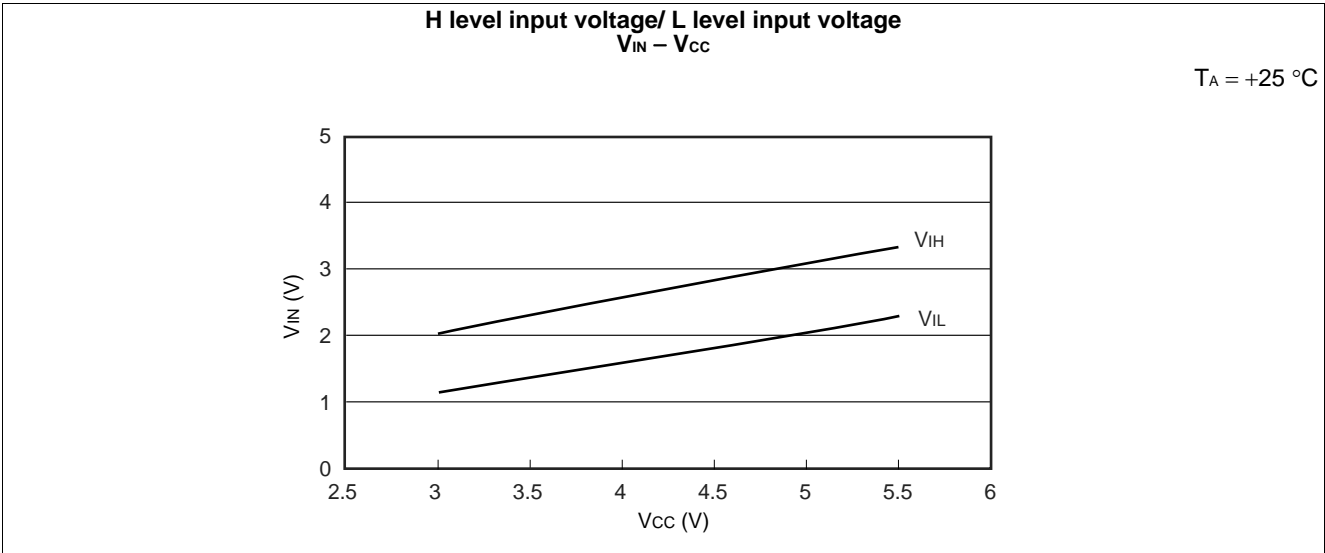
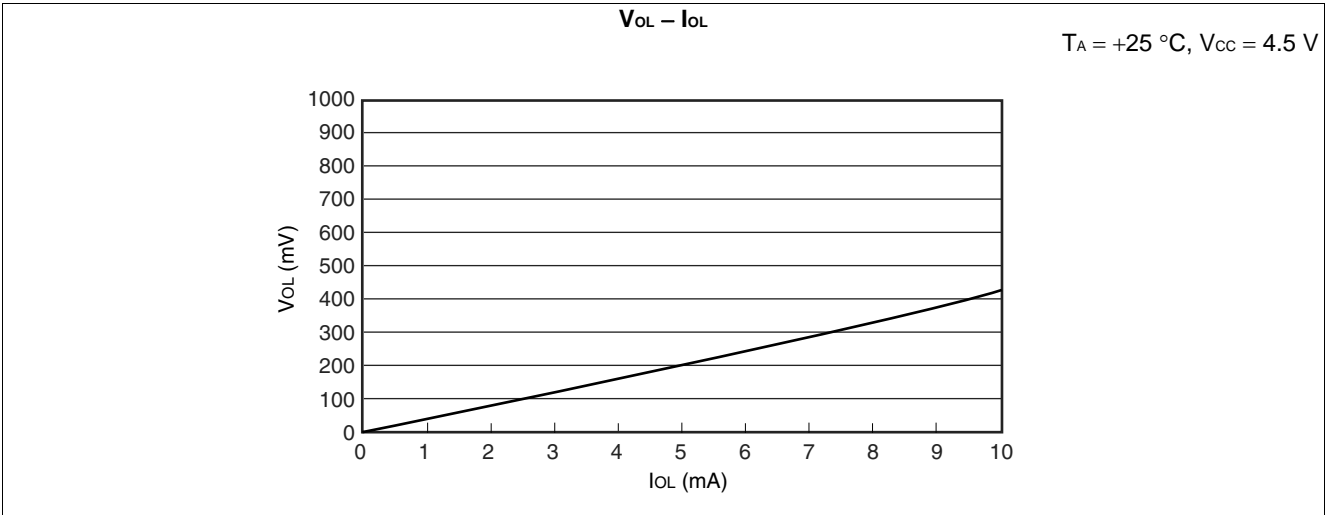
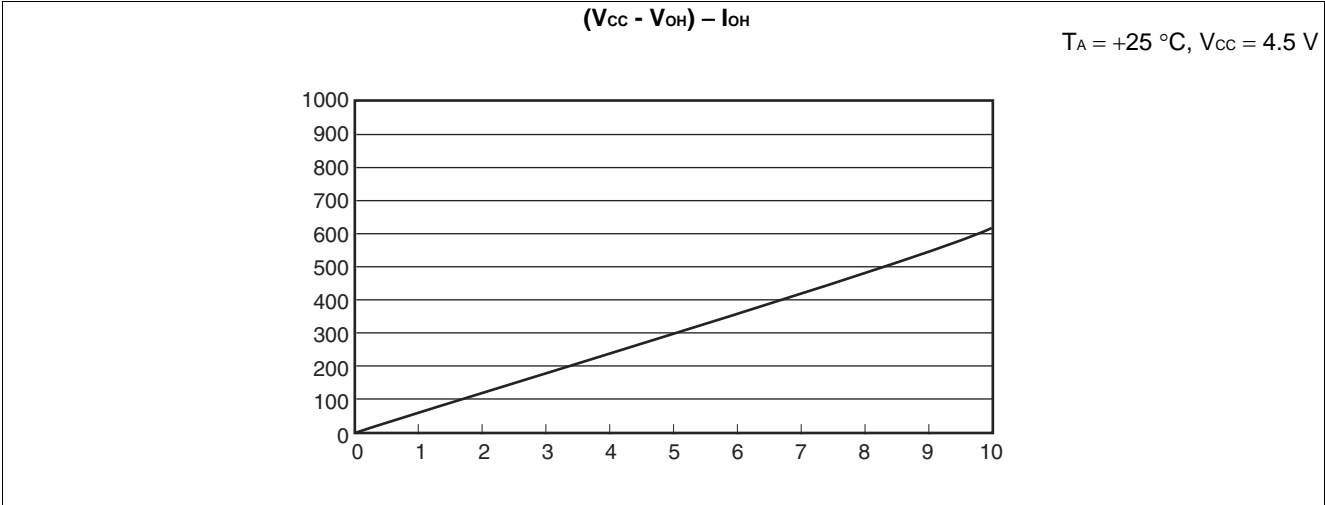
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17. Major Changes

Spanion Publication Number: DS07-13717-5E

Page	Section	Change Results
4	■ PRODUCT LINEUP	Changed the number of channel of 8/16 bit PPG timer. or one 16-bit channel → or two 16-bit channels
13	■ BLOCK DIAGRAM	Changed the direction of arrow of TIN0, TIN1 signals of 16-bit reload timer. right arrow (output) → left arrow (input)
67	■ ELECTRIC CHARACTERISTICS 4. AC Characteristics (4) UART timing	Changed the value of Serial clock. Serial clock "H" pulse width: $4t_{CP} \rightarrow 2t_{CP}$ Serial clock "L" pulse width: $4t_{CP} \rightarrow 2t_{CP}$

NOTE: Please see "Document History" about later revised information.