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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

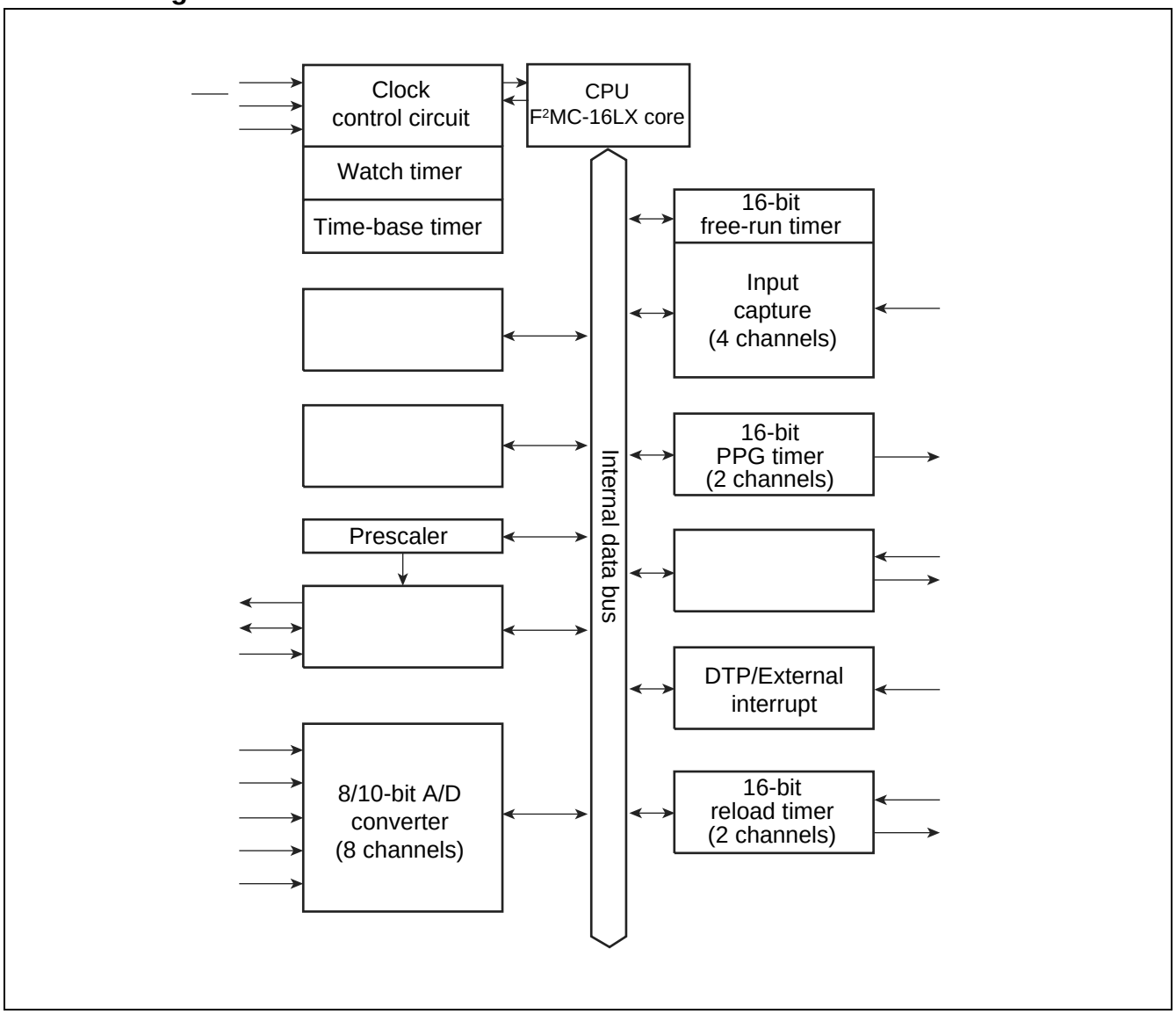
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, SCI, UART/USART
Peripherals	POR, WDT
Number of I/O	36
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90f387spmt-gs

Pin No.	Pin Name	Circuit Type	Function
39	P42	D	General-purpose input/output port.
	SOT1		Serial data input pin for UART. Valid only when serial data input/output setting on UART is “enabled.”
40	P43	D	General-purpose input/output port.
	TX		Transmission output pin for CAN. Valid only when output setting is “enabled.”
41	P44	D	General-purpose input/output port.
	RX		Transmission output pin for CAN. Valid only when output setting is “enabled.”
42 to 45	P30 to P33	D	General-purpose input/output ports.
46	X0A*	A	Pin for low-rate oscillation.
	P35*		General-purpose input/output port.
47	X1A*	A	Pin for low-rate oscillation.
	P36*		General-purpose input/output port.
48	AVss	–	Vss power source input pin for A/D converter.

*: MB90387, MB90F387: X1A, X0A
MB90387S, MB90F387S: P36, P35

8. Block Diagram



9. Memory Map

MB90385 series allows specifying a memory access mode “single chip mode.”

9.1 Memory Allocation of MB90385

MB90385 series model has 24-bit wide internal address bus and up to 24-bit bus of external address bus.
A maximum of 16-Mbyte memory space of external access memory is accessible.

10. I/O Map

Address	Register Abbreviation	Register	Read/ Write	Resource	Initial Value
000000H	(Reserved area) *				
000001H	PDR1	Port 1 data register	R/W	Port 1	XXXXXXXXB
000002H	PDR2	Port 2 data register	R/W	Port 2	XXXXXXXXB
000003H	PDR3	Port 3 data register	R/W	Port 3	XXXXXXXXB
000004H	PDR4	Port 4 data register	R/W	Port 4	XXXXXXXXB
000005H	PDR5	Port 5 data register	R/W	Port 5	XXXXXXXXB
000006H to 000010H	(Reserved area) *				
000011H	DDR1	Port 1 direction data register	R/W	Port 1	00000000B
000012H	DDR2	Port 2 direction data register	R/W	Port 2	00000000B
000013H	DDR3	Port 3 direction data register	R/W	Port 3	000X0000B
000014H	DDR4	Port 4 direction data register	R/W	Port 4	XXX00000B
000015H	DDR5	Port 5 direction data register	R/W	Port 5	00000000B
000016H to 00001AH	(Reserved area) *				
00001BH	ADER	Analog input permission register	R/W	8/10-bit A/D converter	11111111B
00001CH to 000025H	(Reserved area) *				
000026H	SMR1	Serial mode register 1	R/W	UART1	00000000B
000027H	SCR1	Serial control register 1	R/W, W		00000100B
000028H	SIDR1/ SODR1	Serial input data register 1/ Serial output data register 1	R, W		XXXXXXXXB
000029H	SSR1	Serial status data register 1	R, R/W		00001000B
00002AH	(Reserved area) *				
00002BH	CDCR1	Communication prescaler control register 1	R/W	UART1	0XXX0000B
00002CH to 00002FH	(Reserved area) *				
000030H	ENIR	DTP/External interrupt permission register	R/W	DTP/External interrupt	00000000B
000031H	EIRR	DTP/External interrupt permission register	R/W		XXXXXXXXB
000032H	ELVR	Detection level setting register	R/W		00000000B
000033H			R/W		00000000B
000034H	ADCS	A/D control status register	R/W	8/10-bit A/D converter	00000000B
000035H			R/W, W		00000000B
000036H	ADCR	A/D data register	W, R		XXXXXXXXB
000037H			R		00101XXXB

Address	Register Abbreviation	Register	Read/ Write	Resource	Initial Value
000038H to 00003FH	(Reserved area) *				
000040H	PPGC0	PPG0 operation mode control register	R/W, W	8/16-bit PPG timer 0/1	0X000XX1B
000041H	PPGC1	PPG1 operation mode control register	R/W, W		0X000001B
000042H	PPG01	PPG0/1 count clock selection register	R/W		000000XXB
000043H	(Reserved area) *				
000044H	PPGC2	PPG2 operation mode control register	R/W, W	8/16-bit PPG timer 2/3	0X000XX1B
000045H	PPGC3	PPG3 operation mode control register	R/W, W		0X000001B
000046H	PPG23	PPG2/3 count clock selection register	R/W		000000XXB
000047H to 00004FH	(Reserved area) *				
000050H	IPCP0	Input capture data register 0	R	16-bit input/output timer	XXXXXXXXB
000051H					XXXXXXXXB
000052H	IPCP1	Input capture data register 1	R		XXXXXXXXB
000053H					XXXXXXXXB
000054H	ICS01	Input capture control status register	R/W		00000000B
000055H	ICS23				00000000B
000056H	TCDT	Timer counter data register	R/W		00000000B
000057H					00000000B
000058H	TCCS	Timer counter control status register	R/W		00000000B
000059H	(Reserved area) *				
00005AH	IPCP2	Input capture data register 2	R	16-bit input/output timer	XXXXXXXXB
00005BH					XXXXXXXXB
00005CH	IPCP3	Input capture data register 3	R		XXXXXXXXB
00005DH					XXXXXXXXB
00005EH to 000065H	(Reserved area) *				
000066H	TMCSR0	Timer control status register	R/W	16-bit reload timer 0	00000000B
000067H			R/W		XXXX0000B
000068H	TMCSR1		R/W	16-bit reload timer 1	00000000B
000069H			R/W		XXXX0000B
00006AH to 00006EH	(Reserved area) *				
00006FH	ROMM	ROM mirroring function selection register	W	ROM mirroring function selection module	XXXXXXX1B
000070H to 00007FH	(Reserved area) *				
000080H	BVALR	Message buffer enabling register	R/W	CAN controller	00000000B
000081H	(Reserved area) *				
000082H	TREQR	Send request register	R/W	CAN controller	00000000B

Address	Register Abbreviation	Register	Read/ Write	Resource	Initial Value
0000B0H	ICR00	Interrupt control register 00	R/W	Interrupt controller	00000111B
0000B1H	ICR01	Interrupt control register 01			00000111B
0000B2H	ICR02	Interrupt control register 02			00000111B
0000B3H	ICR03	Interrupt control register 03			00000111B
0000B4H	ICR04	Interrupt control register 04			00000111B
0000B5H	ICR05	Interrupt control register 05			00000111B
0000B6H	ICR06	Interrupt control register 06			00000111B
0000B7H	ICR07	Interrupt control register 07			00000111B
0000B8H	ICR08	Interrupt control register 08			00000111B
0000B9H	ICR09	Interrupt control register 09			00000111B
0000BAH	ICR10	Interrupt control register 10			00000111B
0000BBH	ICR11	Interrupt control register 11			00000111B
0000BCH	ICR12	Interrupt control register 12			00000111B
0000BDH	ICR13	Interrupt control register 13			00000111B
0000BEH	ICR14	Interrupt control register 14			00000111B
0000BFH	ICR15	Interrupt control register 15			00000111B
0000C0H to 0000FFH	(Reserved area) *				
001FF0H	PADR0	Detection address setting register 0 (low-order)	R/W	Address matching detection function	XXXXXXXXB
001FF1H		Detection address setting register 0 (middle-order)			XXXXXXXXB
001FF2H		Detection address setting register 0 (high-order)			XXXXXXXXB
001FF3H	PADR1	Detection address setting register 1 (low-order)	R/W		XXXXXXXXB
001FF4H		Detection address setting register 1 (middle-order)			XXXXXXXXB
001FF5H		Detection address setting register 1 (high-order)			XXXXXXXXB
003900H	TMR0/ TMRLR0	16-bit timer register 0/16-bit reload register	R,W	16-bit reload timer 0	XXXXXXXXB
003901H					XXXXXXXXB
003902H	TMR1/ TMRLR1	16-bit timer register 1/16-bit reload register	R,W	16-bit reload timer 1	XXXXXXXXB
003903H					XXXXXXXXB
003904H to 00390FH	(Reserved area) *				

Address	Register Abbreviation	Register	Read/ Write	Resource	Initial Value
003D0D$_H$	(Reserved area) *				
003D0E$_H$	TIER	Send completion interrupt permission register	R/W	CAN controller	00000000$_B$
003D0F$_H$	(Reserved area) *				
003D10$_H$, 003D11$_H$	AMSR	Acceptance mask selection register	R/W	CAN controller	XXXXXXXX$_B$, XXXXXXXX$_B$
003D12$_H$, 003D13$_H$	(Reserved area) *				
003D14$_H$ to 003D17$_H$	AMR0	Acceptance mask register 0	R/W	CAN controller	XXXXXXXX$_B$ to XXXXXXXX$_B$
003D18$_H$ to 003D1B$_H$	AMR1	Acceptance mask register 1	R/W		XXXXXXXX$_B$ to XXXXXXXX$_B$
003D1C$_H$ to 003DFF$_H$	(Reserved area) *				
003E00$_H$ to 003EFF$_H$	(Reserved area) *				
003FF0$_H$ to 003FFF$_H$	(Reserved area) *				

Initial values:

0: Initial value of this bit is “0.”

1: Initial value of this bit is “1.”

X: Initial value of this bit is undefined.

*: “Reserved area” should not be written anything. Result of reading from “Reserved area” is undefined.

12.4 16-bit Input/Output Timer

The 16-bit input/output timer is a compound module composed of 16-bit free-run timer, (1 unit) and input capture (2 units, 4 input pins). The timer, using the 16-bit free-run timer as a basis, enables measurement of clock cycle of an input signal and its pulse width.

Configuration of 16-bit Input/Output Timer

The 16-bit input/output timer is composed of the following modules:

- 16-bit free-run timer (1 unit)
- Input capture (2 units, 2 input pins per unit)

Functions of 16-bit Input/Output Timer

Functions of 16-bit Free-run Timer

The 16-bit free-run timer is composed of 16-bit up counter, timer counter control status register, and prescaler. The 16-bit up counter increments in synchronization with dividing ratio of machine clock.

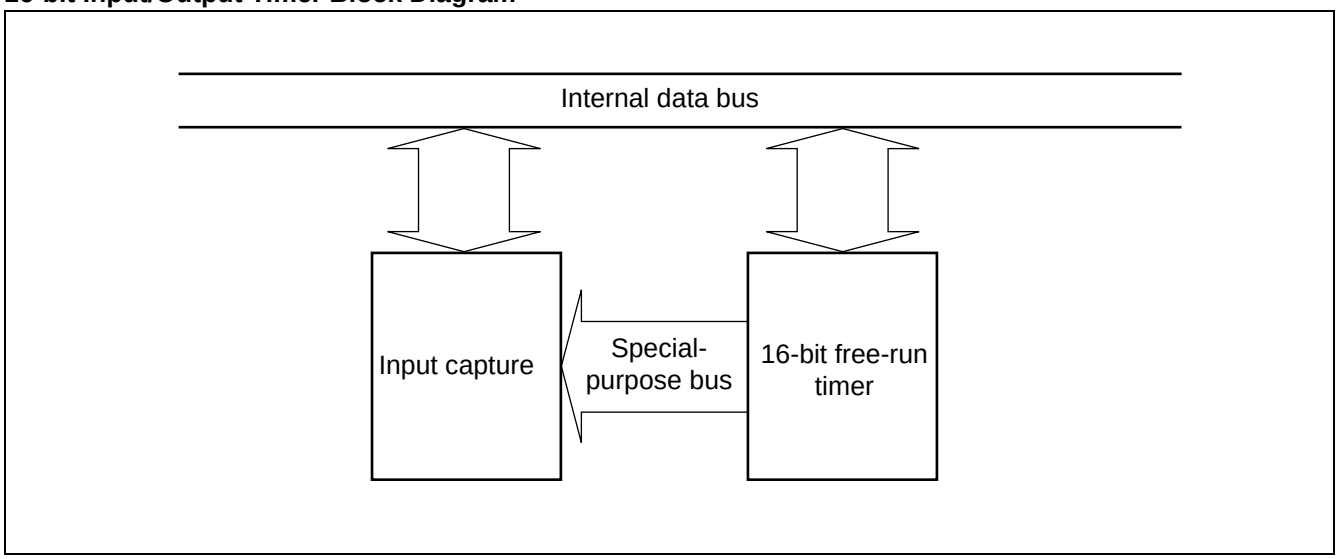
- Count clock is set among four types of machine clock dividing rates.
- Generation of interrupt is allowed by counter value overflow.
- Activation of expanded intelligent I/O service (EI^{2}OS) is allowed by interrupt generation.
- Counter value of 16-bit free-run timer is cleared to "0000$_H$" by either resetting or software-clearing with timer count clear bit (TCCS: CLR).
- Counter value of 16-bit free-run timer is output to input capture, which is available as base time for capture operation.

Functions of Input Capture

The input capture, upon detecting an edge of a signal input to the input pin from external device, stores a counter value of 16-bit free-run timer at the time of detection into the input capture data register. The function includes the input capture data registers corresponding to four input pins, input capture control status register, and edge detection circuit.

- Rising edge, falling edge, and both edges are selectable for detection.
- Generating interrupt on CPU is allowed by detecting an edge of input signal.
- Expanded intelligent I/O service (EI^{2}OS) is activated by interrupt generation.
- The four input capture input pins and input capture data registers allows monitoring of a maximum of four events.

16-bit Input/Output Timer Block Diagram



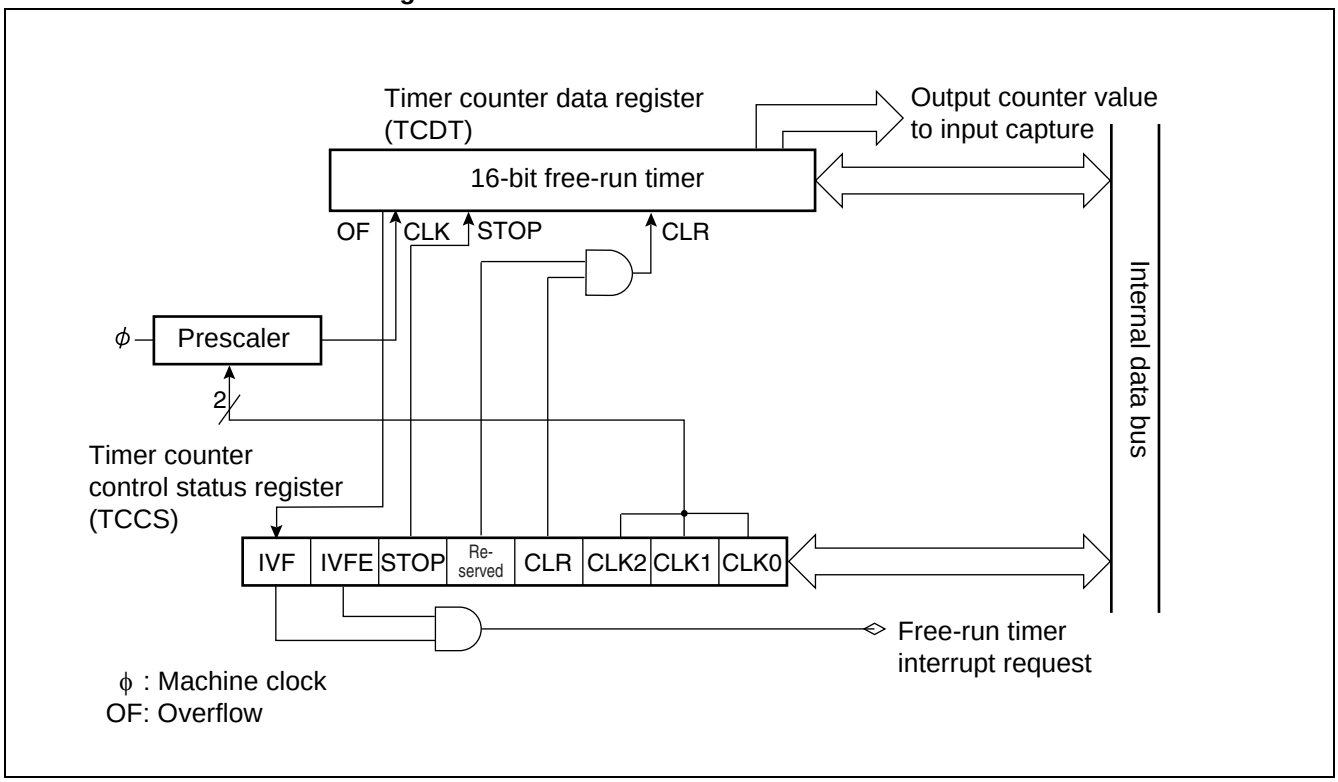
16-bit Free-run Timer

Counter value of 16-bit free-run timer is used as reference time (base time) of input capture.

Input Capture

Input capture detects rising edge, falling edge or both edges and retains a counter value of 16-bit free-run timer. Detection of edge on input signal is allowed to generate interrupt.

16-bit Free-run Timer Block Diagram



Detailed Pin Assignment on Block Diagram

The 16-bit input/output timer includes a 16-bit free-run timer. Interrupt request number of the 16-bit free-run timer is as follows:
Interrupt request number: 19 (13_H)

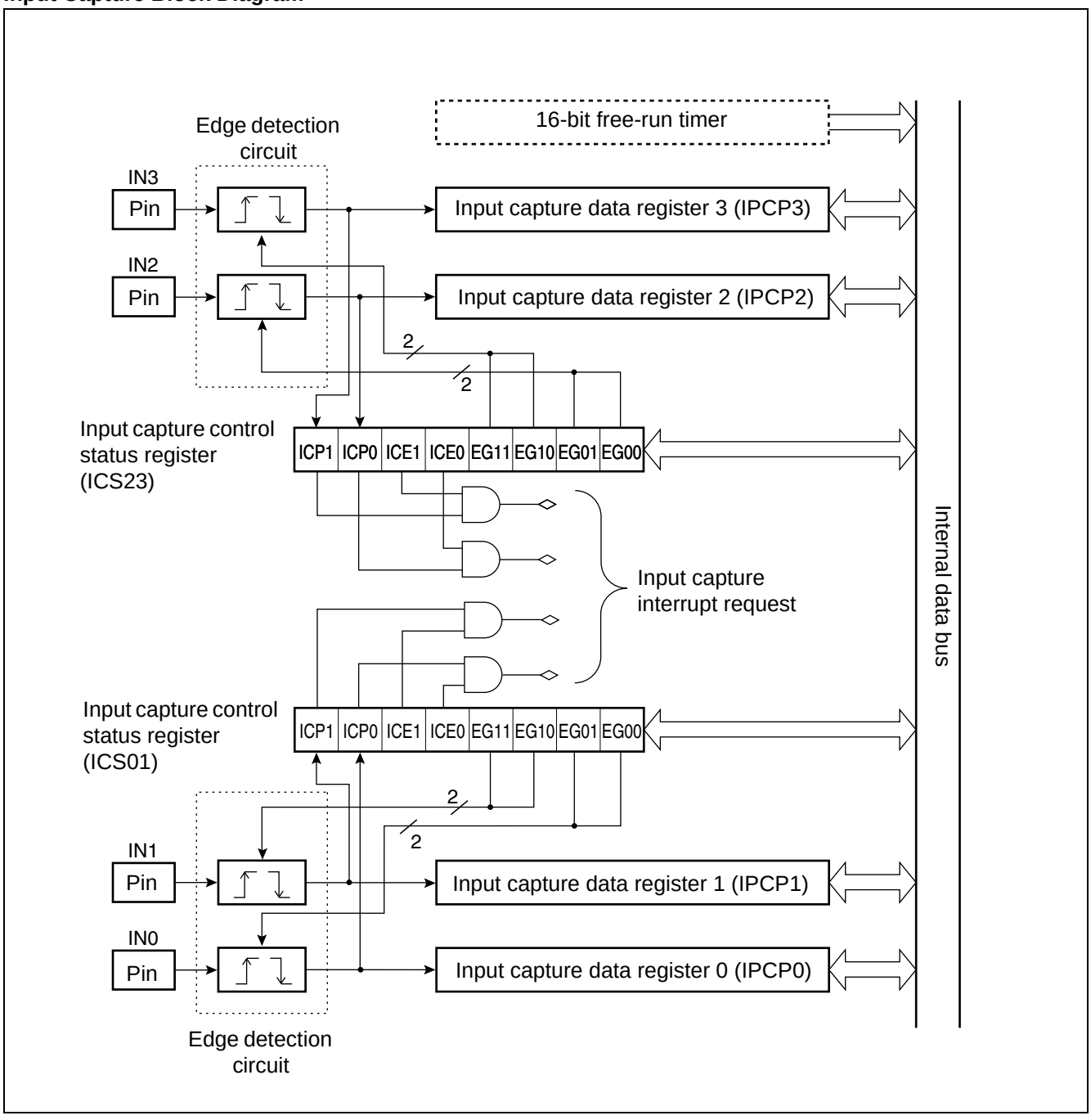
Prescaler

The prescaler divides a machine clock and provides a counter clock to the 16-bit up counter. Dividing ratio of the machine clock is specified by timer counter control status register (TCCS) among four values.

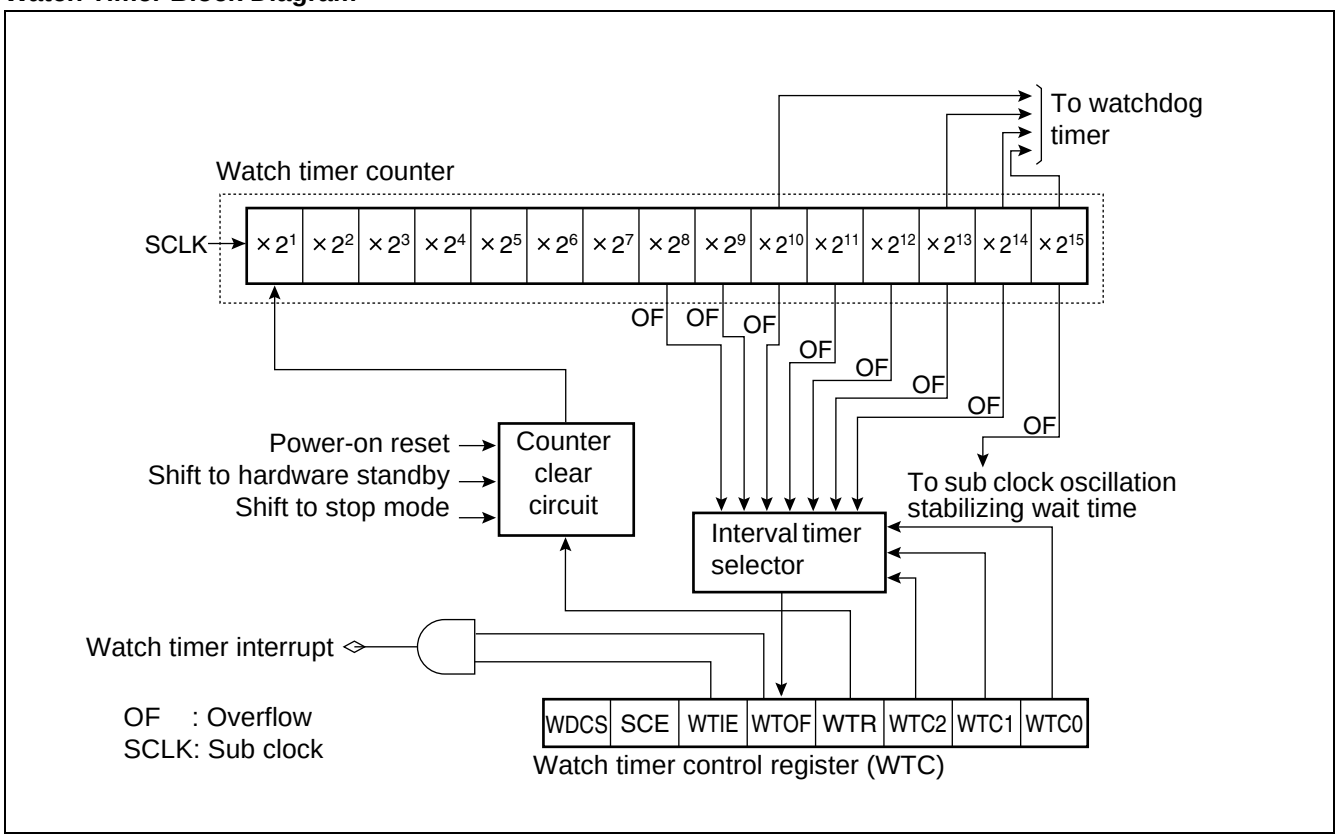
Timer Counter Data Register (TCDT)

The timer counter data register is a 16-bit up counter. A current counter value of the 16-bit free-run timer is read. Writing a value during halt of the counter allows setting an arbitrary counter value.

Input Capture Block Diagram



Watch Timer Block Diagram



Actual interrupt request number of watch timer is as follows:
Interrupt request number: #28 ($1C_H$)

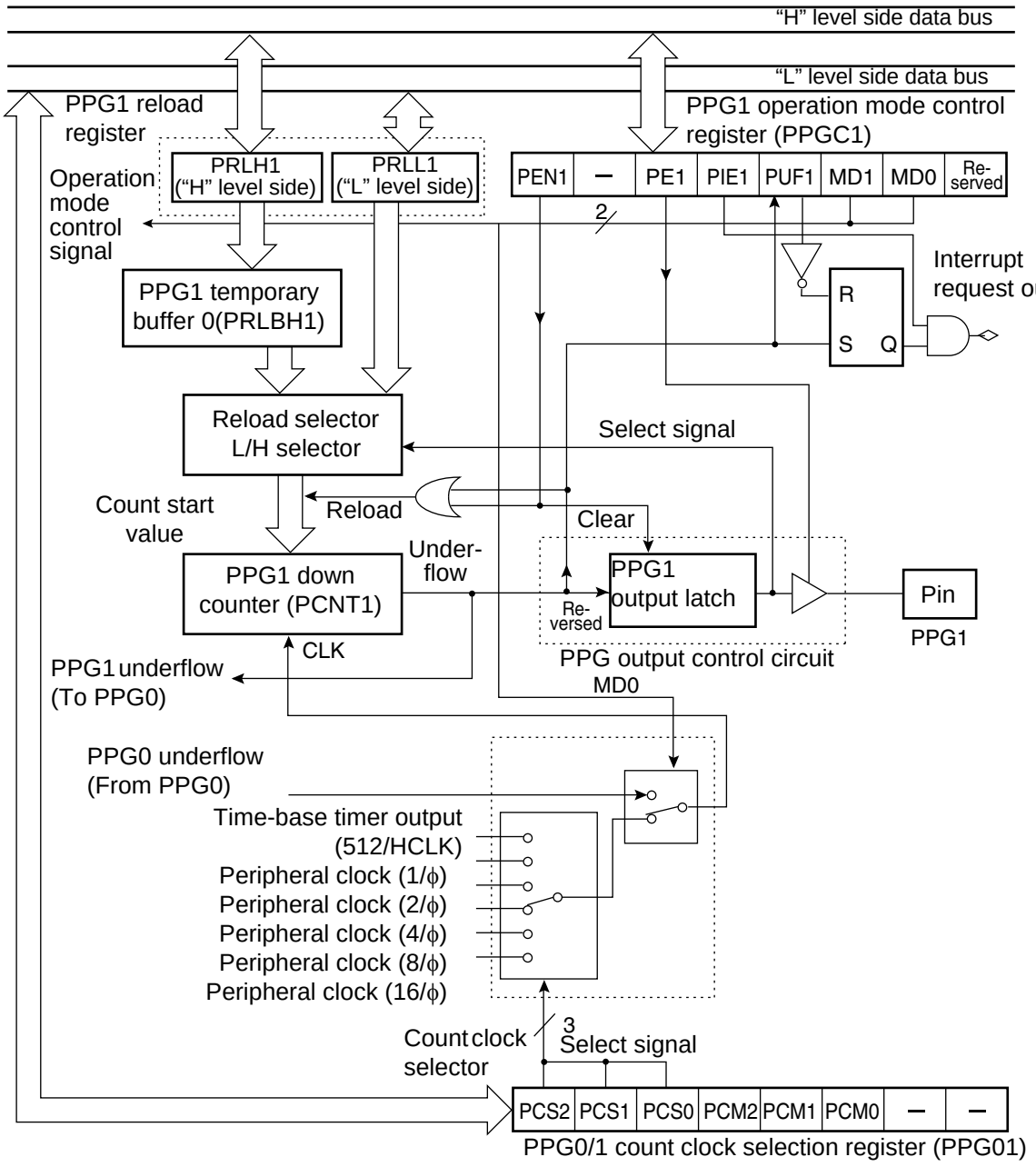
Watch Timer Counter

A 15-bit up counter that uses sub clock (SCLK) as a count clock.

Counter Clear Circuit

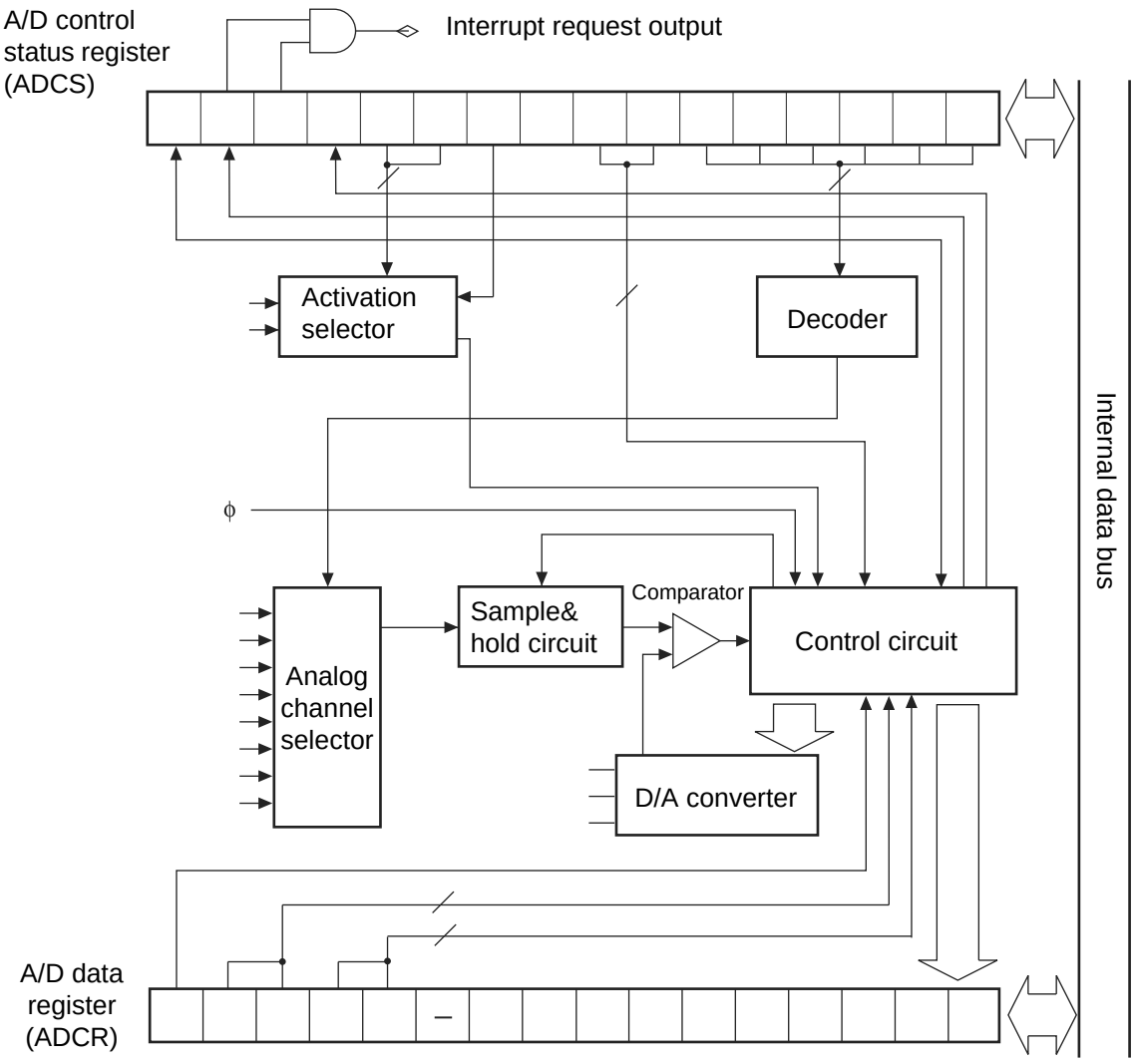
A circuit that clears the watch timer counter.

8/16-bit PPG Timer 1 Block Diagram



– : Undefined
Reserved: Reserved bit
HCLK : Oscillation clock frequency
ϕ : Machine clock frequency
* : Interrupt output of 8/16-bit PPG timer 1 is incorporated into one by the OR circuit against interrupt output of 8/16-bit PPG timer 0.

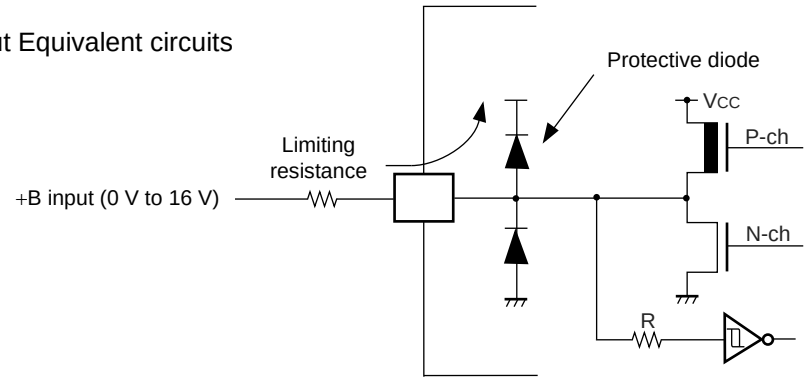
8/10-bit A/D Converter Block Diagram



TO : Internal timer output
– : Not defined
Reserved: Be sure to set to “0”
ϕ : Machine clock

- Use within recommended operating conditions.
- Use at DC voltage (current).
- The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on reset.
- Care must be taken not to leave the +B input pin open.
- Note that analog system input/output pins other than the A/D input pins (LCD drive pins, comparator input pins, etc.) cannot accept +B signal input.
- Sample recommended circuits:

• Input/Output Equivalent circuits



WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

13.2 Recommended Operating Conditions

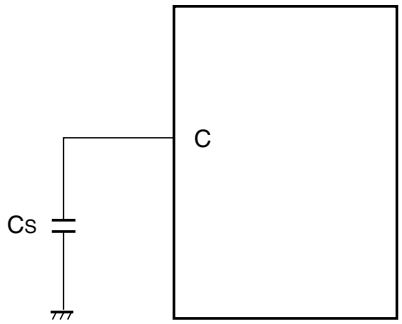
(V_{SS} = AV_{SS} = 0.0V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	V_{CC}	3.5	5.0	5.5	V	Under normal operation
		3.0	–	5.5	V	Retain status of stop operation
	AV_{CC}	4.0	–	5.5	V	*2
Smoothing capacitor	C_S	0.1	–	1.0	μF	*1
Operating temperature	T_A	−40	–	+105	°C	

*1: Use a ceramic capacitor, or a capacitor of similar frequency characteristics. On the Vcc pin, use a bypass capacitor that has a larger capacity than that of Cs.
Refer to the following figure for connection of smoothing capacitor Cs.

*2: AVcc is a voltage at which accuracy is guaranteed. AVcc should not exceed Vcc.

- C pin connection diagram



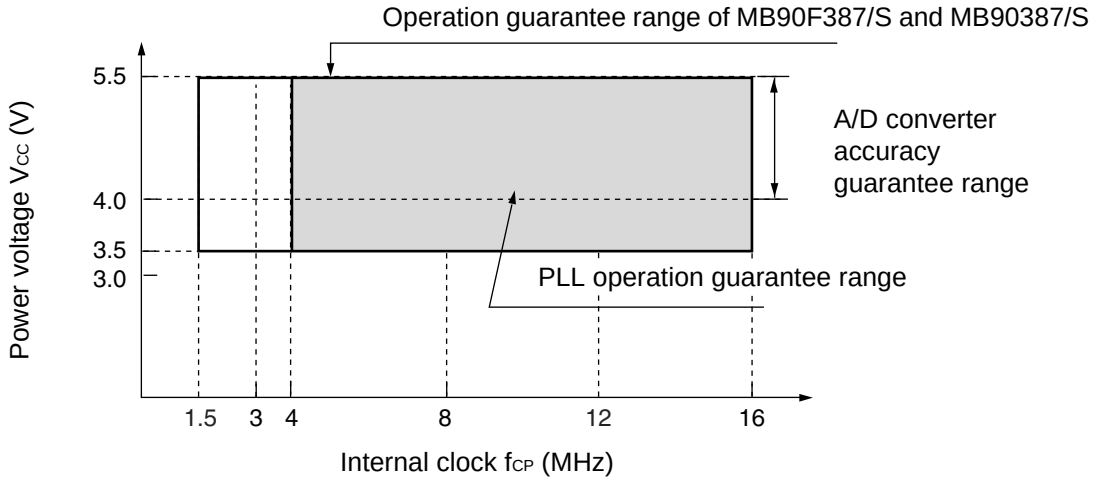
WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

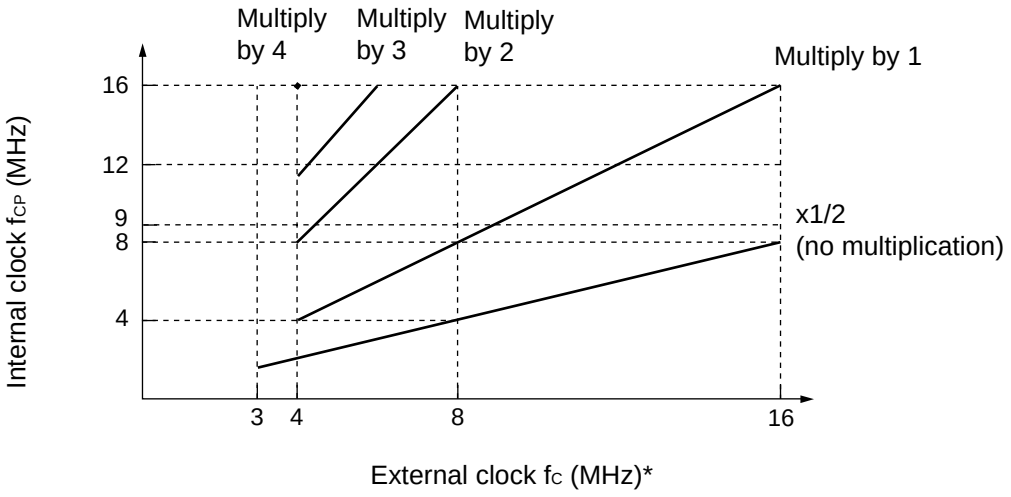
No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

• PLL operation guarantee range

Relation between internal operation clock frequency and power supply voltage



Relation among external clock frequency and internal clock frequency

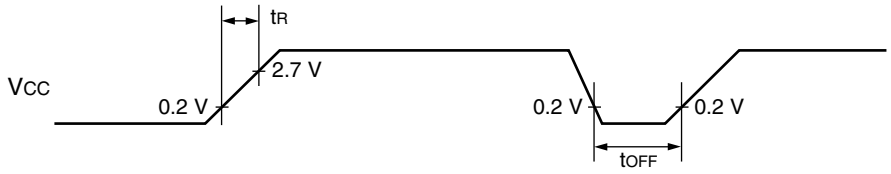


*: fc is 8 MHz at maximum when crystal or ceramic resonator circuit is used.

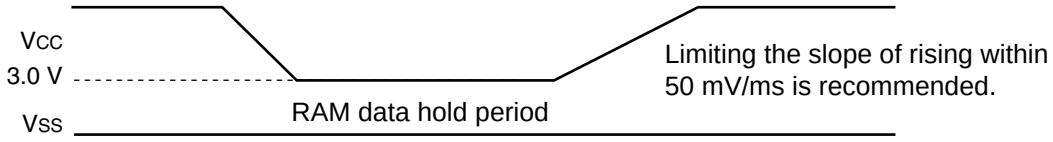
13.4.3 Power-on Reset

(V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Power supply rise time	t_R	V_{CC}	–	0.05	30	ms	
Power supply shutdown time	t_{OFF}	V_{CC}		1	–	ms	Waiting time until power-on

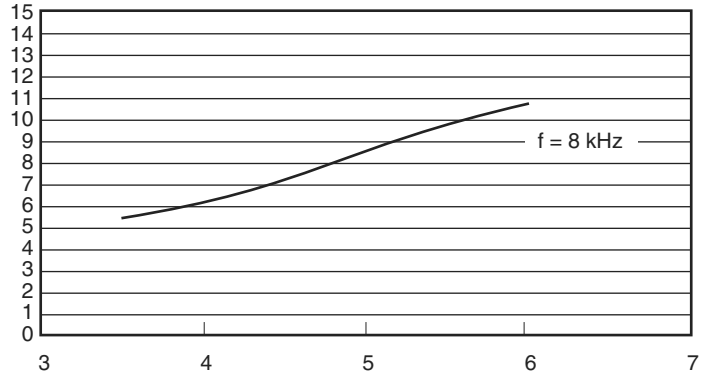


Sudden change of power supply voltage may activate the power-on reset function. When changing power supply voltages during operation, raise the power smoothly by suppressing variation of voltages as shown below. When raising the power, do not use PLL clock. However, if voltage drop is 1V/s or less, use of PLL clock is allowed during operation.



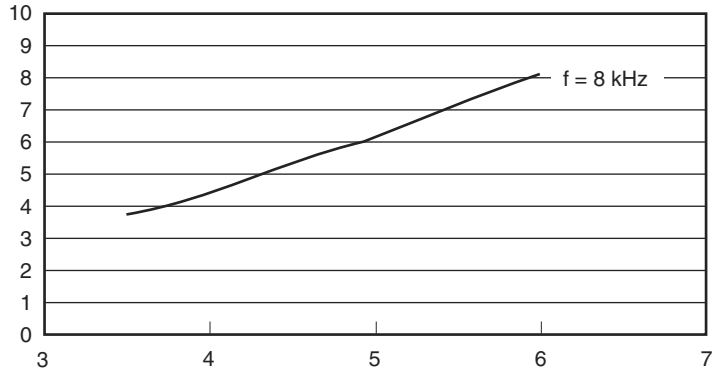
I_{CCLS} – V_{CC}

T_A = +25 °C, In external clock operation
f = Internal operating frequency



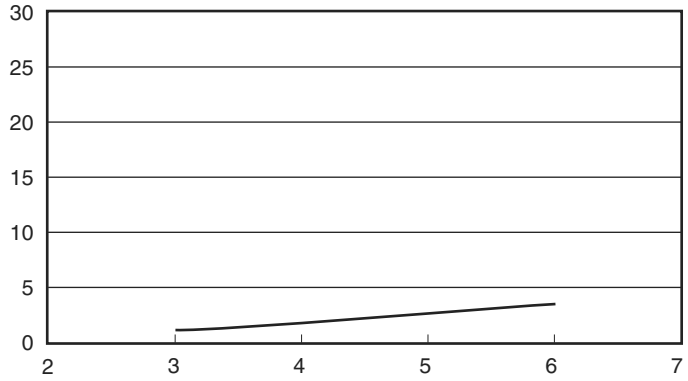
I_{CCT} – V_{CC}

T_A = +25 °C, In external clock operation
f = Internal operating frequency



I_{CCH} – V_{CC}

Stopping, T_A = +25 °C



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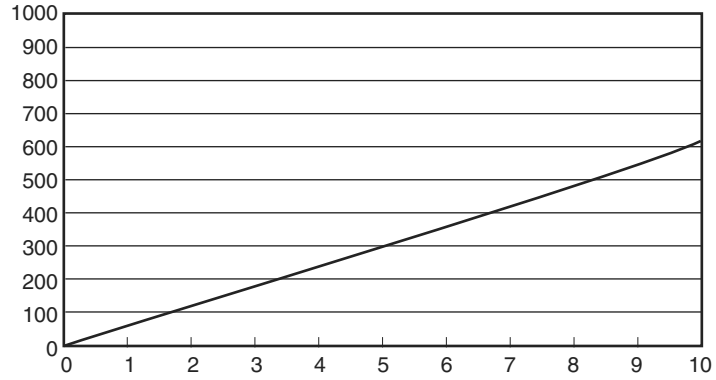
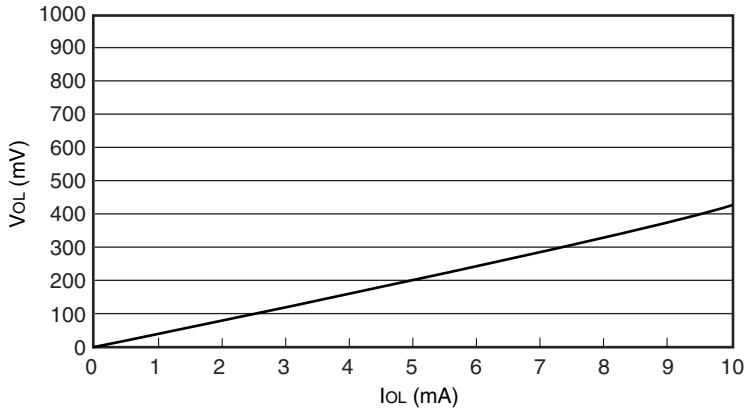
(V_{CC} - V_{OH}) – I_{OH}

T_A = +25 °C, V_{CC} = 4.5 V



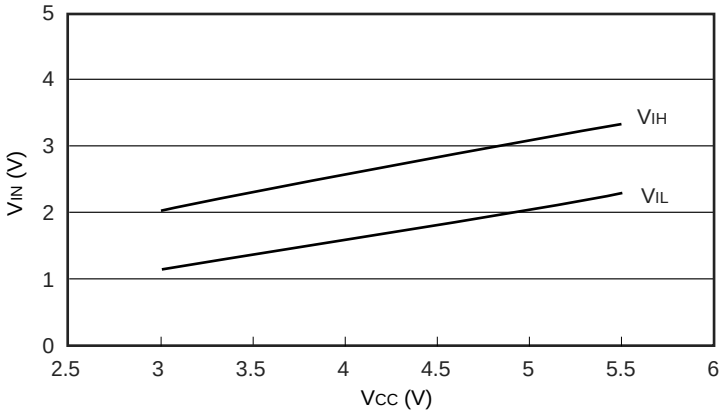
V_{OL} – I_{OL}

T_A = +25 °C, V_{CC} = 4.5 V



H level input voltage/ L level input voltage
V_{IN} – V_{CC}

T_A = +25 °C



17. Major Changes

Spansion Publication Number: DS07-13717-5E

Page	Section	Change Results
4	■ PRODUCT LINEUP	Changed the number of channel of 8/16 bit PPG timer. or one 16-bit channel → or two 16-bit channels
13	■ BLOCK DIAGRAM	Changed the direction of arrow of TIN0, TIN1 signals of 16-bit reload timer. right arrow (output) → left arrow (input)
67	■ ELECTRIC CHARACTERISTICS 4. AC Characteristics (4) UART timing	Changed the value of Serial clock. Serial clock “H” pulse width: $4t_{CP} \rightarrow 2t_{CP}$ Serial clock “L” pulse width: $4t_{CP} \rightarrow 2t_{CP}$

NOTE: Please see "Document History" about later revised information.

Document History

Document Title: MB90387/387S/F387/F387S, MB90V495G, 16-bit Microcontrollers F²MC-16LX MB90385 Series Document Number:002-07765				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	—	AKIH	12/19/2008	Migrated to Cypress and assigned document number 002-07765. No change to document contents or format.
*A	6059071	SSAS	02/05/2018	Updated to Cypress template Package: FPT-48P-M26 --> LQA048