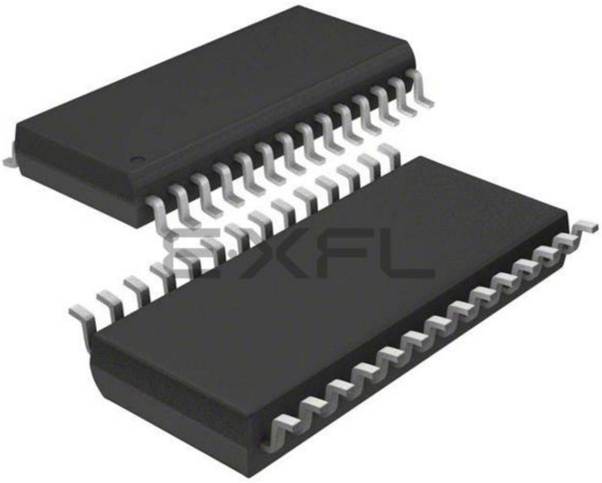
Infineon Technologies - CY8C29466-24PVXA Datasheet



Details	
Product Status	Obsolete
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	24
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.25V
Data Converters	A/D 12x14b; D/A 4x9b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c29466-24pvxa

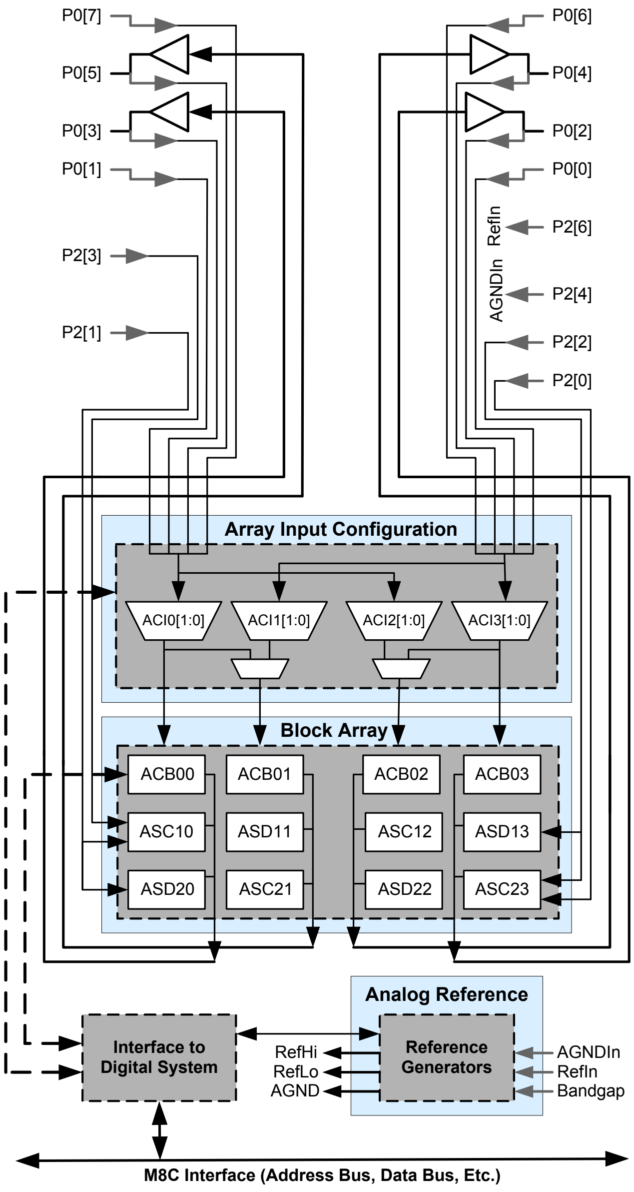
The Analog System

The analog system is composed of 12 configurable blocks, each comprised of an opamp circuit allowing the creation of complex analog signal flows. Analog peripherals are very flexible and can be customized to support specific application requirements. Some of the common PSoC analog functions for this device (most available as user modules) are as follows:

- ADCs (up to four, with 6- to 14-bit resolution, selectable as incremental, delta-sigma, or successive approximation register (SAR))
- Filters (two- and four-pole band pass, low pass, and notch)
- Amplifiers (up to four, with selectable gain up to 48x)
- Instrumentation amplifiers (up to two, with selectable gain up to 93x)
- Comparators (up to four, with 16 selectable thresholds)
- DACs (up to four, with 6- to 9-bit resolution)
- Multiplying DACs (up to four, with 6- to 9-bit resolution)
- High current output drivers (four with 30-mA drive)
- 1.3-V reference (as a system resource)
- DTMF Dialer
- Modulators
- Correlators
- Peak Detectors
- Many other topologies possible

Analog blocks are provided in columns of three, which includes one continuous time (CT) and two switched capacitor (SC) blocks, as shown in Figure 2.

Figure 2. Analog System Block Diagram



Additional System Resources

System resources, some of which have been previously listed, provide additional capability useful for complete systems. Additional resources include a multiplier, decimator, LVD, and power-on reset (POR). Brief statements describing the merits of each system resource are given below:

- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks can be routed to both the digital and analog systems. Additional clocks can be generated using digital PSoC blocks as clock dividers.
- Two multiply accumulates (MACs) provide fast 8-bit multiplier with 32-bit accumulate to assist in both general math as well as digital filters.
- The decimator provides a custom hardware filter for digital signal processing applications including the creation of delta-sigma ADCs.
- The I^2C module provides 0 to 400 kHz communication over two wires. Slave, master, and multimaster modes are all supported.
- LVD interrupts can signal the application of falling voltage levels, while the advanced POR circuit eliminates the need for a system supervisor.
- An internal 1.3-V voltage reference provides an absolute reference for the analog system, including ADCs and DACs.

PSoC Device Characteristics

Depending on your PSoC device characteristics, the digital and analog systems can have a varying number of digital and analog blocks. The following table lists the resources available for specific PSoC device groups. The PSoC device covered by this data sheet is highlighted in Table 1.

Table 1. PSoC Device Characteristics

PSoC Part Number	Digital I/O	Digital Rows	Digital Blocks	Analog Inputs	Analog Outputs	Analog Columns	Analog Blocks	SRAM Size	Flash Size
CY8C29x66[2]	up to 64	4	16	up to 12	4	4	12	2 K	32 K
CY8C28xxx	up to 44	up to 3	up to 12	up to 44	up to 4	up to 6	up to 12 + 4[3]	1 K	16 K
CY8C27x43	up to 44	2	8	up to 12	4	4	12	256	16 K
CY8C24x94[2]	up to 56	1	4	up to 48	2	2	6	1 K	16 K
CY8C24x23A[2]	up to 24	1	4	up to 12	2	2	6	256	4 K
CY8C23x33	up to 26	1	4	up to 12	2	2	4	256	8 K
CY8C22x45[2]	up to 38	2	8	up to 38	0	4	6[3]	1 K	16 K
CY8C21x45[2]	up to 24	1	4	up to 24	0	4	6[3]	512	8 K
CY8C21x34[2]	up to 28	1	4	up to 28	0	2	4[3]	512	8 K
CY8C21x23	up to 16	1	4	up to 8	0	2	4[3]	256	4 K
CY8C20x34[2]	up to 28	0	0	up to 28	0	0	3[3,4]	512	8 K
CY8C20xx6	up to 36	0	0	up to 36	0	0	3[3,4]	up to 2 K	up to 32 K

Notes

[2] Automotive qualified devices available in this group.

[3] Limited analog functionality.

[4] Two analog blocks and one CapSense® block.

Getting Started

For in depth information, along with detailed programming details, see the *PSoC® Technical Reference Manual*.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device datasheets on the web.

Application Notes

Cypress application notes are an excellent introduction to the wide variety of possible PSoC designs.

Development Kits

PSoC Development Kits are available online from and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

Training

Free PSoC technical training (on demand, webinars, and workshops), which is available online via www.cypress.com, covers a wide variety of topics and skill levels to assist you in your designs.

CYPros Consultants

Certified PSoC consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC consultant go to the CYPros Consultants web site.

Solutions Library

Visit our growing library of solution focused designs. Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

Technical Support

Technical support – including a searchable Knowledge Base articles and technical forums – is also available online. If you cannot find an answer to your question, call our Technical Support hotline at 1-800-541-4736.

Designing with PSoC Designer

The development process for the PSoC® device differs from that of a traditional fixed function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called PSoC Blocks, have the ability to implement a wide variety of user-selectable functions. The PSoC development process is summarized in four steps:

1. Select User Modules.
2. Configure user modules.
3. Organize and connect.
4. Generate, verify, and debug.

Select User Modules

PSoC Designer provides a library of prebuilt, pretested hardware peripheral components called “user modules.” User modules make selecting and implementing peripheral devices, both analog and digital, simple.

Configure User Modules

Each user module that you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a pulse width modulator (PWM) User Module configures one or more digital PSoC blocks, one for each 8 bits of resolution. The user module parameters permit you to establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These user module datasheets explain the internal operation of the user module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information you may need to successfully implement your design.

Organize and Connect

You build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. You perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, you perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides application programming interfaces (APIs) with high-level functions to control and respond to hardware events at run time and interrupt service routines that you can adapt as needed.

A complete code development environment allows you to develop and customize your applications in either C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer’s debugger (access by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint and watch-variable features, the debug interface provides a large trace buffer and allows you to define complex breakpoint events that include monitoring address and data bus values, memory locations and external signals.

Table 6. Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW	DBB20FN	40	RW	ASC10CR0	80	RW	RDI2RI	C0	RW
PRT0DM1	01	RW	DBB20IN	41	RW	ASC10CR1	81	RW	RDI2SYN	C1	RW
PRT0IC0	02	RW	DBB20OU	42	RW	ASC10CR2	82	RW	RDI2IS	C2	RW
PRT0IC1	03	RW		43		ASC10CR3	83	RW	RDI2LT0	C3	RW
PRT1DM0	04	RW	DBB21FN	44	RW	ASD11CR0	84	RW	RDI2LT1	C4	RW
PRT1DM1	05	RW	DBB21IN	45	RW	ASD11CR1	85	RW	RDI2RO0	C5	RW
PRT1IC0	06	RW	DBB21OU	46	RW	ASD11CR2	86	RW	RDI2RO1	C6	RW
PRT1IC1	07	RW		47		ASD11CR3	87	RW		C7	
PRT2DM0	08	RW	DCB22FN	48	RW	ASC12CR0	88	RW	RDI3RI	C8	RW
PRT2DM1	09	RW	DCB22IN	49	RW	ASC12CR1	89	RW	RDI3SYN	C9	RW
PRT2IC0	0A	RW	DCB22OU	4A	RW	ASC12CR2	8A	RW	RDI3IS	CA	RW
PRT2IC1	0B	RW		4B		ASC12CR3	8B	RW	RDI3LT0	CB	RW
PRT3DM0	0C	RW	DCB23FN	4C	RW	ASD13CR0	8C	RW	RDI3LT1	CC	RW
PRT3DM1	0D	RW	DCB23IN	4D	RW	ASD13CR1	8D	RW	RDI3RO0	CD	RW
PRT3IC0	0E	RW	DCB23OU	4E	RW	ASD13CR2	8E	RW	RDI3RO1	CE	RW
PRT3IC1	0F	RW		4F		ASD13CR3	8F	RW		CF	
PRT4DM0	10	RW	DBB30FN	50	RW	ASD20CR0	90	RW	GDI_O_IN	D0	RW
PRT4DM1	11	RW	DBB30IN	51	RW	ASD20CR1	91	RW	GDI_E_IN	D1	RW
PRT4IC0	12	RW	DBB30OU	52	RW	ASD20CR2	92	RW	GDI_O_OU	D2	RW
PRT4IC1	13	RW		53		ASD20CR3	93	RW	GDI_E_OU	D3	RW
PRT5DM0	14	RW	DBB31FN	54	RW	ASC21CR0	94	RW		D4	
PRT5DM1	15	RW	DBB31IN	55	RW	ASC21CR1	95	RW		D5	
PRT5IC0	16	RW	DBB31OU	56	RW	ASC21CR2	96	RW		D6	
PRT5IC1	17	RW		57		ASC21CR3	97	RW		D7	
	18		DCB32FN	58	RW	ASD22CR0	98	RW		D8	
	19		DCB32IN	59	RW	ASD22CR1	99	RW		D9	
	1A		DCB32OU	5A	RW	ASD22CR2	9A	RW		DA	
	1B			5B		ASD22CR3	9B	RW		DB	
	1C		DCB33FN	5C	RW	ASC23CR0	9C	RW		DC	
	1D		DCB33IN	5D	RW	ASC23CR1	9D	RW	OSC_GO_EN	DD	RW
	1E		DCB33OU	5E	RW	ASC23CR2	9E	RW	OSC_CR4	DE	RW
	1F			5F		ASC23CR3	9F	RW	OSC_CR3	DF	RW
DBB00FN	20	RW	CLK_CR0	60	RW		A0		OSC_CR0	E0	RW
DBB00IN	21	RW	CLK_CR1	61	RW		A1		OSC_CR1	E1	RW
DBB00OU	22	RW	ABF_CR0	62	RW		A2		OSC_CR2	E2	RW
	23		AMD_CR0	63	RW		A3		VLT_CR	E3	RW
DBB01FN	24	RW		64			A4		VLT_CMP	E4	R
DBB01IN	25	RW		65			A5			E5	
DBB01OU	26	RW	AMD_CR1	66	RW		A6			E6	
	27		ALT_CR0	67	RW		A7			E7	
DCB02FN	28	RW	ALT_CR1	68	RW		A8		IMO_TR	E8	W
DCB02IN	29	RW	CLK_CR2	69	RW		A9		ILO_TR	E9	W
DCB02OU	2A	RW		6A			AA		BDG_TR	EA	RW
	2B			6B			AB		ECO_TR	EB	W
DCB03FN	2C	RW	TMP_DR0	6C	RW		AC			EC	
DCB03IN	2D	RW	TMP_DR1	6D	RW		AD			ED	
DCB03OU	2E	RW	TMP_DR2	6E	RW		AE			EE	
	2F		TMP_DR3	6F	RW		AF			EF	
DBB10FN	30	RW	ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
DBB10IN	31	RW	ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
DBB10OU	32	RW	ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
DBB11FN	34	RW	ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
DBB11IN	35	RW	ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
DBB11OU	36	RW	ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
	37		ACB01CR2	77	RW		B7		CPU_F	F7	RL
DCB12FN	38	RW	ACB02CR3	78	RW	RDI1RI	B8	RW		F8	
DCB12IN	39	RW	ACB02CR0	79	RW	RDI1SYN	B9	RW		F9	
DCB12OU	3A	RW	ACB02CR1	7A	RW	RDI1IS	BA	RW	FLS_PR1	FA	RW
	3B		ACB02CR2	7B	RW	RDI1LT0	BB	RW		FB	
DCB13FN	3C	RW	ACB03CR3	7C	RW	RDI1LT1	BC	RW		FC	
DCB13IN	3D	RW	ACB03CR0	7D	RW	RDI1RO0	BD	RW		FD	
DCB13OU	3E	RW	ACB03CR1	7E	RW	RDI1RO1	BE	RW	CPU_SCR1	FE	#
	3F		ACB03CR2	7F	RW		BF		CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed.

Access is bit specific.

Table 10. DC GPIO Specifications (continued)

Symbol	Description	Min	Typ	Max	Units	Notes
V_H	Input hysteresis	–	60	–	mV	
I_{IL}	Input leakage (absolute value)	–	1	–	nA	Gross tested to 1 μA.
C_{IN}	Capacitive load on pins as input	–	3.5	10	pF	Package and pin dependent. T_A = 25 °C.
C_{OUT}	Capacitive load on pins as output	–	3.5	10	pF	Package and pin dependent. T_A = 25 °C.

DC Operational Amplifier Specifications

Table 11 and Table 12 on page 18 list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

The operational amplifier is a component of both the analog CT PSoC blocks and the analog SC PSoC blocks. The guaranteed specifications are measured in the analog CT PSoC block. Typical parameters apply to 5 V at 25 °C and are for design guidance only.

Power = high and Opamp bias = high settings are not allowed together for 3.3 V V_{DD} operation.

Table 11. 5-V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input offset voltage (absolute value)	–	1.6	10	mV	
TCV_{OSOA}	Average input offset voltage drift	–	4.0	23.0	μV/°C	
I_{EBOA}	Input leakage current (Port 0 analog pins)	–	200	–	pA	Gross tested to 1 μA.
C_{INOA}	Input capacitance (Port 0 analog pins)	–	4.5	9.5	pF	Package and pin dependent. T_A = 25 °C.
V_{CMOA}	Common-mode voltage range All cases, except highest Power = high, Opamp bias = high	 0.0 0.5	 – –	 V_{DD} V_{DD} – 0.5	 V V	
$CMRR_{OA}$	Common-mode rejection ratio	60	–	–	dB	This specification is measured through the analog output buffer and therefore includes the limitations imposed by the characteristics of the analog output buffer.
G_{OLOA}	Open loop gain	80	–	–	dB	
$V_{OHIGHOA}$	High output voltage swing (internal signals)	V_{DD} – 0.01	–	–	V	
V_{OLOWOA}	Low output voltage swing (internal signals)	–	–	0.01	V	
I_{SOA}	Supply current (including associated AGND buffer) Power = low, Opamp bias = low Power = low, Opamp bias = high Power = medium, Opamp bias = low Power = medium, Opamp bias = high Power = high, Opamp bias = low Power = high, Opamp bias = high	 – – – – – –	 150 300 600 1200 2400 4600	 200 400 800 1600 3200 6400	 μA μA μA μA μA μA	
$PSRR_{OA}$	Supply voltage rejection ratio	67	80	–	dB	$V_{SS} \le V_{IN} \le (V_{DD} - 2.25)$ or $(V_{DD} - 1.25\text{ V}) \le V_{IN} \le V_{DD}$.

DC Analog Reference Specifications

Table 16 and Table 17 on page 25 list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

The guaranteed specifications for RefHI and RefLO are measured through the analog continuous time PSoC blocks. The power levels for RefHI and RefLO refer to the analog reference control register. AGND is measured at P2[4] in AGND bypass mode. Each analog continuous time PSoC block adds a maximum of 10 mV additional offset error to guaranteed AGND specifications from the local AGND buffer. Reference control power can be set to medium or high unless otherwise noted.

Note Avoid using P2[4] for digital signaling when using an analog resource that depends on the analog reference. Some coupling of the digital signal may appear on the AGND.

Table 16. 5-V DC Analog Reference Specifications

Reference ARF_CR[5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Unit
0b000	RefPower = High Opamp bias = High	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2 + 1.228$	$V_{DD}/2 + 1.290$	$V_{DD}/2 + 1.352$	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2 – 0.078$	$V_{DD}/2 – 0.007$	$V_{DD}/2 + 0.063$	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2 – 1.336$	$V_{DD}/2 – 1.295$	$V_{DD}/2 – 1.250$	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2 + 1.224$	$V_{DD}/2 + 1.293$	$V_{DD}/2 + 1.356$	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2 – 0.056$	$V_{DD}/2 – 0.005$	$V_{DD}/2 + 0.043$	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2 – 1.338$	$V_{DD}/2 – 1.298$	$V_{DD}/2 – 1.255$	V
	RefPower = Med Opamp bias = High	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2 + 1.226$	$V_{DD}/2 + 1.293$	$V_{DD}/2 + 1.356$	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2 – 0.057$	$V_{DD}/2 – 0.006$	$V_{DD}/2 + 0.044$	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2 – 1.337$	$V_{DD}/2 – 1.298$	$V_{DD}/2 – 1.256$	V
	RefPower = Med Opamp bias = Low	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2 + 1.226$	$V_{DD}/2 + 1.294$	$V_{DD}/2 + 1.359$	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2 – 0.047$	$V_{DD}/2 – 0.004$	$V_{DD}/2 + 0.035$	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2 – 1.338$	$V_{DD}/2 – 1.299$	$V_{DD}/2 – 1.258$	V

DC Programming Specifications

Table 20 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 20. DC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{DDP}	V_{DD} for programming and erase	4.5	5.0	5.5	V	This specification applies to the functional requirements of external programmer tools.
V_{DDLV}	Low V_{DD} for verify	3.0	3.1	3.2	V	This specification applies to the functional requirements of external programmer tools.
V_{DDHV}	High V_{DD} for verify	5.1	5.2	5.3	V	This specification applies to the functional requirements of external programmer tools.
$V_{DDIWRITE}$	Supply voltage for flash write operation	3.0	–	5.25	V	This specification applies to this device when it is executing internal flash writes.
I_{DDP}	Supply current during programming or verify	–	10	30	mA	
V_{ILP}	Input low voltage during programming or verify	–	–	0.8	V	
V_{IHP}	Input high voltage during programming or verify	2.1	–	–	V	
I_{ILP}	Input current when applying V_{ILP} to P1[0] or P1[1] during programming or verify	–	–	0.2	mA	Driving internal pull-down resistor.
I_{IHP}	Input current when applying V_{IHP} to P1[0] or P1[1] during programming or verify	–	–	1.5	mA	Driving internal pull-down resistor.
V_{OLV}	Output low voltage during programming or verify	–	–	0.75	V	
V_{OHV}	Output high voltage during programming or verify	V_{DD} – 1.0	–	V_{DD}	V	
$Flash_{ENPB}$	Flash endurance (per block)[9, 10]	1,000	–	–	–	Erase/write cycles per block.
$Flash_{ENT}$	Flash endurance (total)[10, 11]	512,000	–	–	–	Erase/write cycles.
$Flash_{DR}$	Flash data retention	15	–	–	Years	

Notes

[9] The erase/write cycle limit per block ($Flash_{ENPB}$) is only guaranteed if the device operates within one voltage range. Voltage ranges are 3.0 V to 3.6 V and 4.75 V to 5.25 V.

[10] For the full temperature range, the user must employ a temperature sensor user module (FlashTemp) or other temperature sensor, and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 for more information.

[11] The maximum total number of allowed erase/write cycles is the minimum $Flash_{ENPB}$ value multiplied by the number of flash blocks in the device.

AC Electrical Characteristics

AC Chip-Level Specifications

Table 21 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40°C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 21. AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{IMO24}	IMO frequency for 24 MHz	22.8[12]	24	25.2[12]	MHz	Trimmed for 5 V or 3.3 V operation using factory trim values. See Figure 5 on page 14. SLIMO mode = 0.
F_{IMO6}	IMO frequency for 6 MHz	5.5[12]	6	6.5[12]	MHz	Trimmed for 5 V or 3.3 V operation using factory trim values. See Figure 5 on page 14. SLIMO mode = 1.
F_{CPU1}	CPU frequency (5 V nominal)	0.089[12]	–	25.2[12]	MHz	4.75 V ≤ V_{DD} ≤ 5.25 V. SLIMO mode = 0.
F_{CPU2}	CPU frequency (3.3 V nominal)	0.089[12]	–	12.6[12]	MHz	3.0 V ≤ V_{DD} ≤ 3.6 V. SLIMO mode = 0.
F_{BLK5}	Digital PSoC block frequency (5 V V_{DD} nominal)	0	–	50.4[12,13]	MHz	Refer to AC Digital Block Specifications on page 35.
F_{BLK33}	Digital PSoC block frequency (3.3 V V_{DD} nominal)	0	–	25.2[12,13]	MHz	Refer to AC Digital Block Specifications on page 35.
F_{32K1}	ILO frequency	15	32	64	kHz	This specification applies when the ILO has been trimmed.
F_{32KU}	ILO untrimmed frequency	5	–	100	kHz	After a reset and before the M8C processor starts to execute, the ILO is not trimmed.
F_{32K2}	ECO frequency	–	32.768	–	kHz	Accuracy is capacitor and crystal dependent. 50% duty cycle.
F_{PLL}	PLL frequency	–	23.986	–	MHz	A multiple (x732) of crystal frequency.
$t_{PLLSLEW}$	PLL lock time	0.5	–	10	ms	Refer to Figure 7 on page 31.
$t_{PLLSLEWLOW}$	PLL lock time for low gain setting	0.5	–	50	ms	Refer to Figure 8 on page 31.
t_{OS}	ECO startup to 1%	–	250	500	ms	Refer to Figure 9 on page 31.
t_{OSACC}	ECO startup to 100 ppm	–	300	600	ms	The ECO frequency is within 100 ppm of its final value by the end of the t_{OSACC} period. Correct operation assumes a properly loaded 1-μW maximum drive level, 32.768-kHz crystal.
t_{XRST}	External reset pulse width	10	–	–	μs	
DC24M	24 MHz duty cycle	40	50	60	%	
DC_{ILO}	ILO duty cycle	20	50	80	%	
Step24M	24 MHz trim step size	–	50	–	kHz	
Fout48M	48 MHz output frequency	45.6 [12]	48.0	50.4 [12]	MHz	
F_{MAX}	Maximum frequency of signal on row input or row output.	–	–	12.6[12]	MHz	
$SR_{POWERUP}$	Power supply slew rate	–	–	250	V/ms	V_{DD} slew rate during power up.
$t_{POWERUP}$	Time between end of POR state and CPU code execution	–	16	100	ms	Power up from 0 V.

Notes

[12] Accuracy derived from IMO with appropriate trim for V_{DD} range.

[13] See the individual user module data sheets for information on maximum frequencies for user modules.

Table 21. AC Chip-Level Specifications (continued)

Symbol	Description	Min	Typ	Max	Units	Notes
t_{JIT_IMO}[14]	24 MHz IMO cycle-to-cycle jitter (RMS)	–	200	700	ps	
	24 MHz IMO long term N cycle-to-cycle jitter (RMS)	–	300	900	ps	N = 32
	24 MHz IMO period jitter (RMS)	–	100	400	ps	
t_{JIT_PLL}[14]	PLL cycle-to-cycle jitter (RMS)	–	200	800	ps	
	PLL long term N cycle-to-cycle jitter (RMS)	–	300	1200	ps	N = 32
	PLL period jitter (RMS)	–	100	700	ps	

Figure 7. PLL Lock Timing Diagram

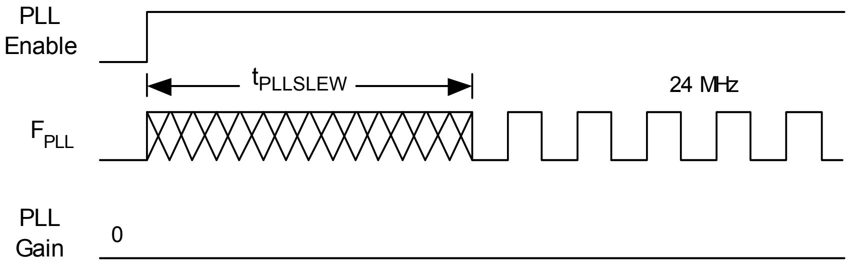


Figure 8. PLL Lock for Low Gain Setting Timing Diagram

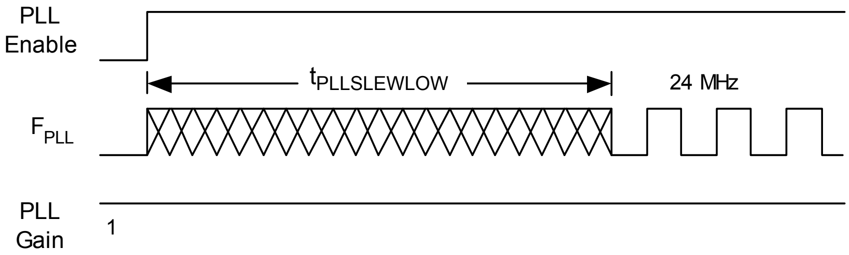
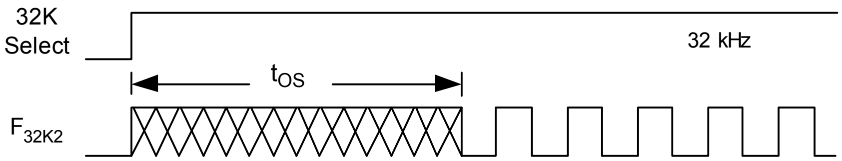


Figure 9. External Crystal Oscillator Startup Timing Diagram



Note

[14] Refer to Cypress Jitter Specifications application note, Understanding Datasheet Jitter Specifications for Cypress Timing Products – AN5054 for more information.

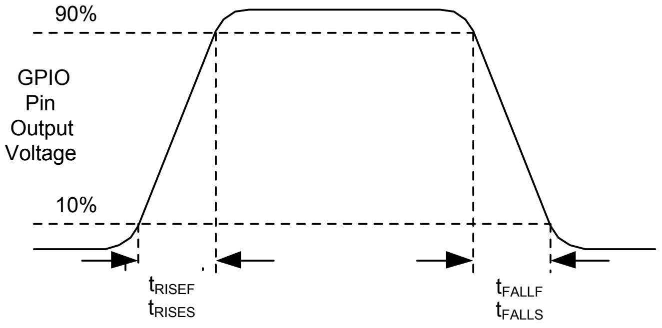
AC GPIO Specifications

Table 22 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 22. AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO operating frequency	0	–	12.6[15]	MHz	Normal strong mode
t_{RISEF}	Rise time, normal strong mode, Cload = 50 pF	3	–	18	ns	V_{DD} = 4.75 to 5.25 V, 10% - 90%
t_{FALLF}	Fall time, normal strong mode, Cload = 50 pF	2	–	18	ns	V_{DD} = 4.75 to 5.25 V, 10% - 90%
t_{RISES}	Rise time, slow strong mode, Cload = 50 pF	10	27	–	ns	V_{DD} = 3 to 5.25 V, 10% - 90%
t_{FALLS}	Fall time, slow strong mode, Cload = 50 pF	10	22	–	ns	V_{DD} = 3 to 5.25 V, 10% - 90%

Figure 10. GPIO Timing Diagram

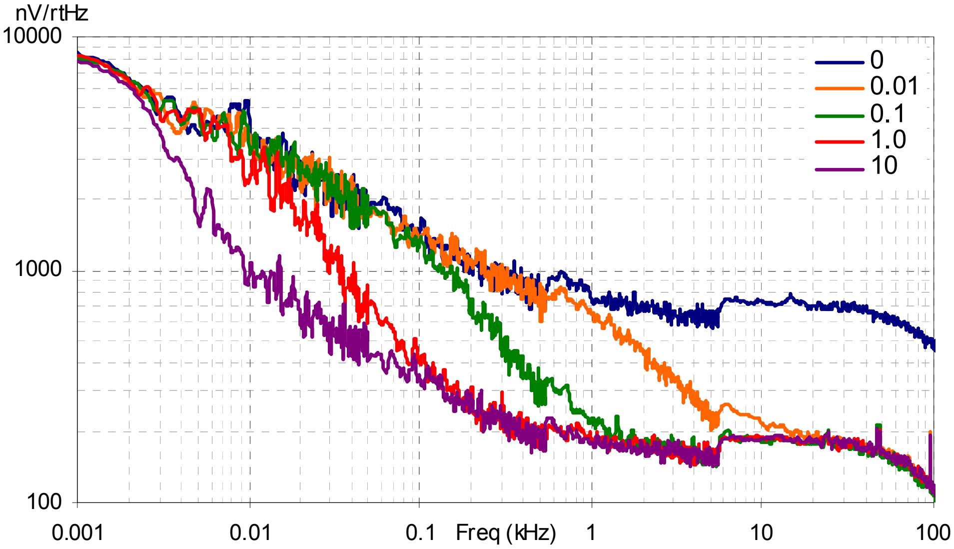


Note

15. Accuracy derived from IMO with appropriate trim for V_{DD} range.

When bypassed by a capacitor on P2[4], the noise of the analog ground signal distributed to each block is reduced by a factor of up to 5 (14 dB). This is at frequencies above the corner frequency defined by the on-chip 8.1 kΩ resistance and the external capacitor.

Figure 11. Typical AGND Noise with P2[4] Bypass



At low frequencies, the opamp noise is proportional to 1/f, power independent, and determined by device geometry. At high frequencies, increased power level reduces the noise spectrum level.

Figure 12. Typical Opamp Noise

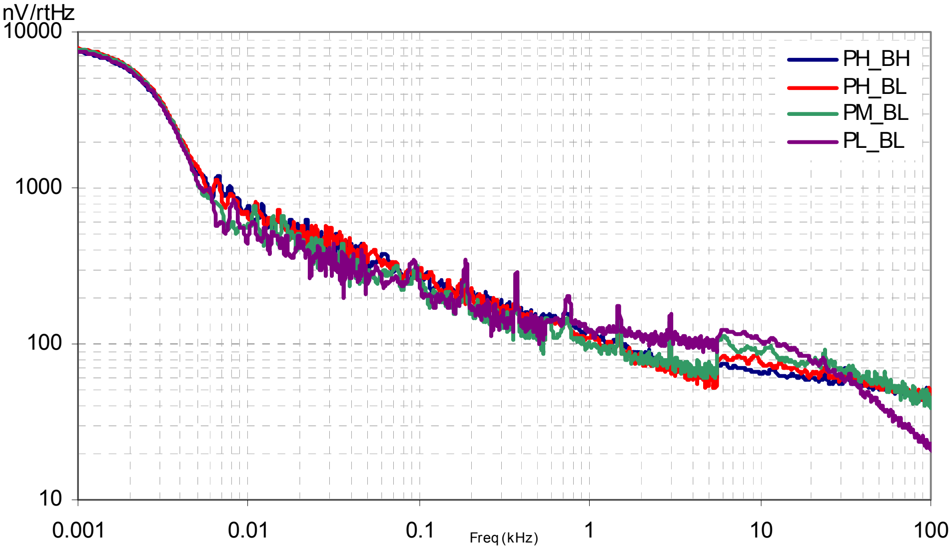
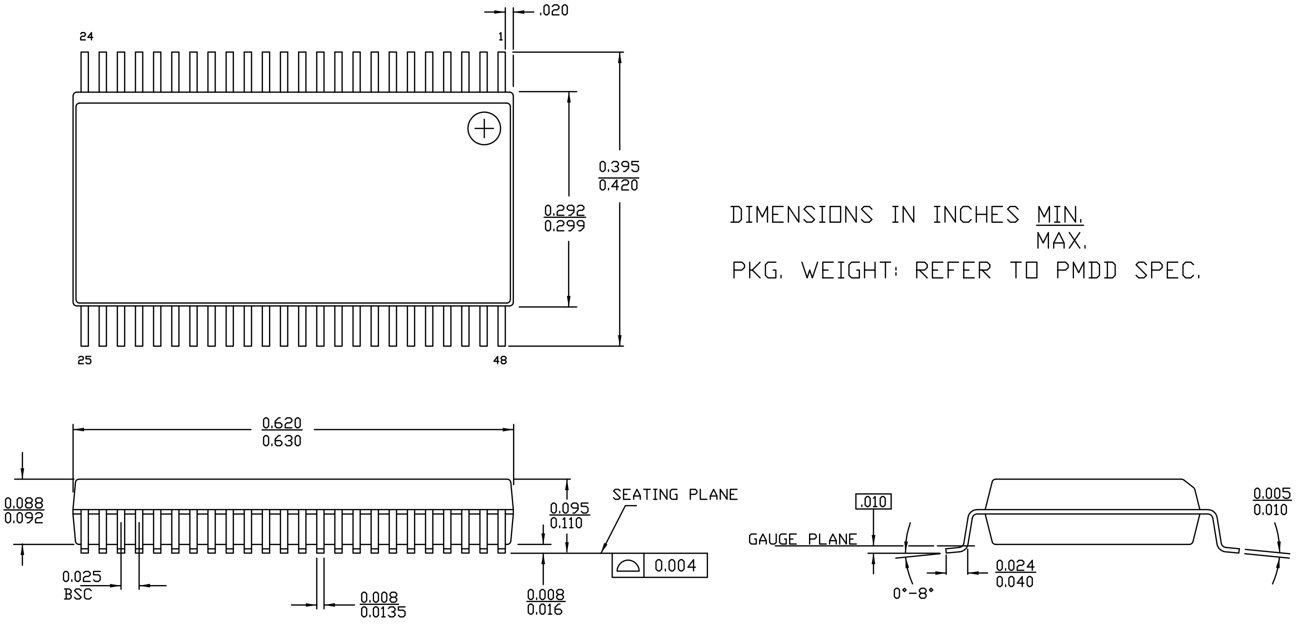


Figure 15. 48-Pin (300-Mil) SSOP



51-85061 *F

Thermal Impedances

Table 33. Thermal Impedances per Package

Package	Typical θ_{JA} [22]
28-pin SSOP	94 °C/W
48-pin SSOP	69 °C/W

Capacitance on Crystal Pins

Table 34. Typical Package Capacitance on Crystal Pins

Package	Package Capacitance
28-pin SSOP	2.8 pF
48-pin SSOP	3.3 pF

Solder Reflow Specifications

Table 35 shows the solder reflow temperature limits that must not be exceeded.

Table 35. Solder Reflow Specifications

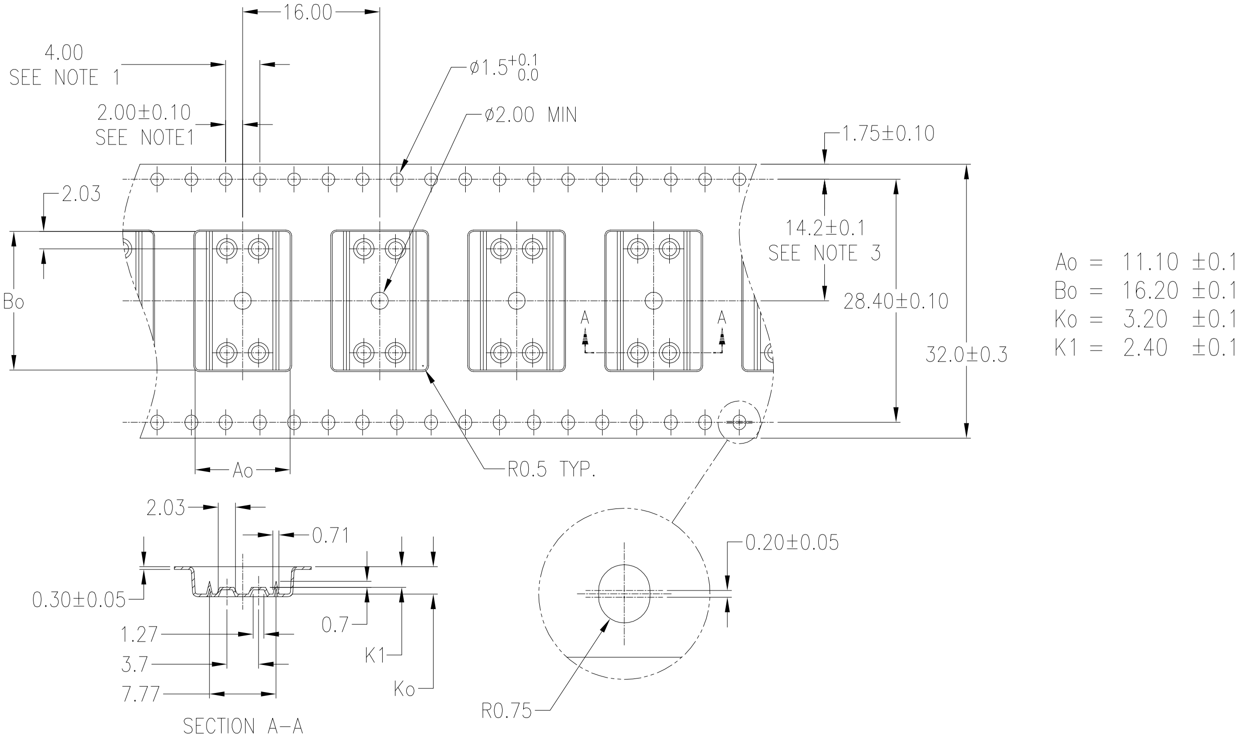
Package	Maximum Peak Temperature (T_C)	Maximum Time above T_C – 5 °C
28-pin SSOP	260 °C	30 seconds
48-pin SSOP	260 °C	30 seconds

Note

[22] $T_J = T_A + \text{Power} \times \theta_{JA}$.

Figure 17. 48-Pin SSOP Carrier Tape Drawing

NOTES:
1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.2
2. CAMBER IN COMPLIANCE WITH EIA 481
3. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE
POSITION OF POCKET, NOT POCKET HOLE



51-51104 *E

Table 36. Tape and Reel Specifications

Package	Cover Tape Width (mm)	Hub Size (inches)	Minimum Leading Empty Pockets	Minimum Trailing Empty Pockets	Standard Full Reel Quantity
28-Pin SSOP	13.3	7	42	25	1000
48-Pin SSOP	25.5	4	32	19	1000

Device Programmers

All device programmers can be purchased from the Cypress Online Store. The online store also has the most up to date information on kit contents, descriptions, and availability.

CY3210-MiniProg1

The CY3210-MiniProg1 kit allows a user to program PSoC devices through the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC via a provided USB 2.0 cable. The kit includes:

- MiniProg programming unit
- MiniEval socket programming and evaluation board
- 28-pin CY8C29466-24PXI PDIP PSoC device sample
- PSoC Designer software CD
- Getting Started guide
- USB 2.0 cable

CY3207ISSP In-System Serial Programmer (ISSP)

The CY3207ISSP is a production programmer. It includes protection circuitry and an industrial case that is more robust than the MiniProg in a production-programming environment.

Note: CY3207ISSP needs special software and is not compatible with PSoC Programmer. This software is free and can be downloaded from http://www.cypress.com. The kit includes:

- CY3207 programmer unit
- PSoC ISSP software CD
- 110 ~ 240-V power supply, Euro-Plug adapter
- USB 2.0 cable

Accessories (Emulation and Programming)

Table 37. Emulation and Programming Accessories

Part Number	Pin Package	Pod Kit[23]	Foot Kit[24]	Adapter[25]
CY8C29466-24PVXA	28-pin SSOP	CY3250-29XXX	CY3250-28SSOP-FK	AS-28-28-02SS-6ENP-GANG
CY8C29666-24PVXA	48-pin SSOP	CY3250-29XXX	CY3250-48SSOP-FK	AS-48-48-01SS-6-GANG

Notes

[23] Pod kit contains an emulation pod, a flex-cable (connects the pod to the ICE), two feet, and device samples.

[24] Foot kit includes surface mount feet that can be soldered to the target PCB.

[25] Programming adapter converts non-DIP package to DIP footprint. Specific details and ordering information for each of the adapters are available at http://www.emulation.com.

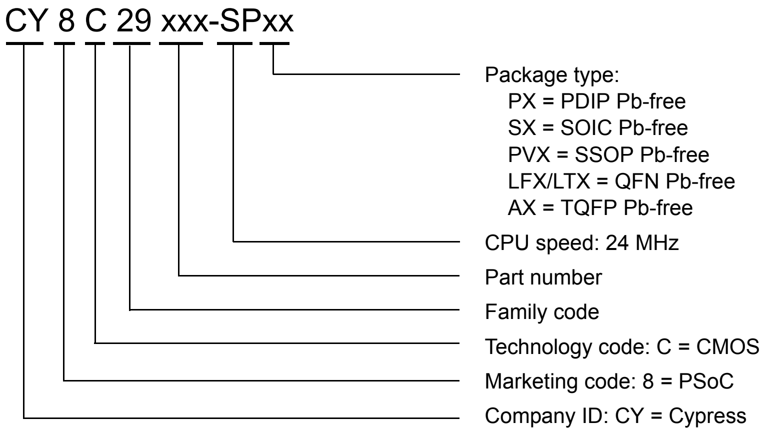
Ordering Information

The following table lists the automotive CY8C29x66 PSoC devices' key package features and ordering codes.

Table 38. CY8C29x66 Automotive PSoC Device Key Features and Ordering Information

Package	Ordering Code	Flash (KB)	RAM (KB)	Temperature Range	Digital PSoC Blocks	Analog PSoC Blocks	Digital I/O Pins	Analog Inputs	Analog Outputs	XRES Pin
28-pin (210-Mil) SSOP	CY8C29466-24PVXA	32	2	–40 °C to +85 °C	16	12	24	12[26]	4	Yes
28-pin (210-Mil) SSOP (tape and reel)	CY8C29466-24PVXAT	32	2	–40 °C to +85 °C	16	12	24	12[26]	4	Yes
48-pin (300-Mil) SSOP	CY8C29666-24PVXA	32	2	–40 °C to +85 °C	16	12	44	12[26]	4	Yes
48-pin (300-Mil) SSOP (tape and reel)	CY8C29666-24PVXAT	32	2	–40 °C to +85 °C	16	12	44	12[26]	4	Yes

Ordering Code Definitions



CY 8 C 29 xxx-SPxx

Package type:
PX = PDIP Pb-free
SX = SOIC Pb-free
PVX = SSOP Pb-free
LFX/LTX = QFN Pb-free
AX = TQFP Pb-free

CPU speed: 24 MHz

Part number

Family code

Technology code: C = CMOS

Marketing code: 8 = PSoC

Company ID: CY = Cypress

Thermal Rating:
A = Automotive -40 °C to +85 °C
C = Commercial
E = Automotive Extended -40 °C to +125 °C
I = Industrial

Note

[26] There are eight standard analog inputs on the GPIO. The other four analog inputs connect from the GPIO directly to specific switched-capacitor block inputs. See the *PSoC Technical Reference Manual* for more details

Glossary (continued)

bias	1. A systematic deviation of a value from a reference value. 2. The amount by which the average of a set of values departs from a reference value. 3. The electrical, mechanical, magnetic, or other force (field) applied to a device to establish a reference level to operate the device.
block	1. A functional unit that performs a single function, such as an oscillator. 2. A functional unit that may be configured to perform one of several functions, such as a digital PSoC block or an analog PSoC block.
buffer	1. A storage area for data that is used to compensate for a speed difference, when transferring data from one device to another. Usually refers to an area reserved for I/O operations, into which data is read, or from which data is written. 2. A portion of memory set aside to store data, often before it is sent to an external device or as it is received from an external device. 3. An amplifier used to lower the output impedance of a system.
bus	1. A named connection of nets. Bundling nets together in a bus makes it easier to route nets with similar routing patterns. 2. A set of signals performing a common function and carrying similar data. Typically represented using vector notation; for example, address[7:0]. 3. One or more conductors that serve as a common connection for a group of related devices.
clock	The device that generates a periodic signal with a fixed frequency and duty cycle. A clock is sometimes used to synchronize different logic blocks.
comparator	An electronic circuit that produces an output voltage or current whenever two input levels simultaneously satisfy predetermined amplitude requirements.
compiler	A program that translates a high level language, such as C, into machine language.
configuration space	In PSoC devices, the register space accessed when the XIO bit, in the CPU_F register, is set to ‘1’.
crystal oscillator	An oscillator in which the frequency is controlled by a piezoelectric crystal. Typically a piezoelectric crystal is less sensitive to ambient temperature than other circuit components.
cyclic redundancy check (CRC)	A calculation used to detect errors in data communications, typically performed using a linear feedback shift register. Similar calculations may be used for a variety of other purposes such as data compression.
data bus	A bi-directional set of signals used by a computer to convey information from a memory location to the central processing unit and vice versa. More generally, a set of signals used to convey data between digital functions.
debugger	A hardware and software system that allows you to analyze the operation of the system under development. A debugger usually allows the developer to step through the firmware one step at a time, set break points, and analyze memory.
dead band	A period of time when neither of two or more signals are in their active state or in transition.
digital blocks	The 8-bit logic blocks that can act as a counter, timer, serial receiver, serial transmitter, CRC generator, pseudo-random number generator, or SPI.
digital-to-analog converter (DAC)	A device that changes a digital signal to an analog signal of corresponding magnitude. The analog-to-digital converter (ADC) performs the reverse operation.

Glossary (continued)

microcontroller	An integrated circuit chip that is designed primarily for control systems and products. In addition to a CPU, a microcontroller typically includes memory, timing circuits, and I/O circuitry. The reason for this is to permit the realization of a controller with a minimal quantity of chips, thus achieving maximal possible miniaturization. This in turn, reduces the volume and the cost of the controller. The microcontroller is normally not used for general-purpose computation as is a microprocessor.
mixed-signal	The reference to a circuit containing both analog and digital techniques and components.
modulator	A device that imposes a signal on a carrier.
noise	1. A disturbance that affects a signal and that may distort the information carried by the signal. 2. The random variations of one or more characteristics of any entity such as voltage, current, or data.
oscillator	A circuit that may be crystal controlled and is used to generate a clock frequency.
parity	A technique for testing transmitted data. Typically, a binary digit is added to the data to make the sum of all the digits of the binary data either always even (even parity) or always odd (odd parity).
phase-locked loop (PLL)	An electronic circuit that controls an *oscillator* so that it maintains a constant phase angle relative to a reference signal.
pinouts	The pin number assignment: the relation between the logical inputs and outputs of the PSoC device and their physical counterparts in the printed circuit board (PCB) package. Pinouts involve pin numbers as a link between schematic and PCB design (both being computer generated files) and may also involve pin names.
port	A group of pins, usually eight.
power-on reset (POR)	A circuit that forces the PSoC device to reset when the voltage is below a pre-set level. This is one type of hardware reset.
PSoC®	Cypress Semiconductor's PSoC® is a registered trademark and Programmable System-on-Chip™ is a trademark of Cypress.
PSoC Designer™	The software for Cypress' Programmable System-on-Chip technology.
pulse width modulator (PWM)	An output in the form of duty cycle which varies as a function of the applied value.
RAM	An acronym for random access memory. A data-storage device from which data can be read out and new data can be written in.
register	A storage device with a specific capacity, such as a bit or byte.
reset	A means of bringing a system back to a known state. See hardware reset and software reset.
ROM	An acronym for read only memory. A data-storage device from which data can be read out, but new data cannot be written in.
serial	1. Pertaining to a process in which all events occur one after the other. 2. Pertaining to the sequential or consecutive occurrence of two or more related activities in a single device or channel.
settling time	The time it takes for an output signal or value to stabilize after the input has changed from one value to another.

Document History Page

Document Title: CY8C29466, CY8C29666 Automotive PSoC® Programmable System-on-Chip™
Document Number: 001-12899

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	772096	HMT	See ECN	New silicon, new document (Revision **).
*A	2697720	VIVG/ PYRS	04/24/09	Updated template Content edits
*B	2769233	BTK	09/25/09	Updated Features section. Updated text of PSoC Functional Overview section. Updated Getting Started section. Made corrections and minor text edits to Pinouts section. Changed the name of some sections for added clarity. Improved formatting of the register tables. Added clarifying comments to some electrical specifications. Changed T_{RAMP} specification per MASJ input. Fixed all AC specifications to conform to a ±5% IMO accuracy. Made other miscellaneous minor text edits. Deleted some non-applicable or redundant information. Added a footnote to clarify that 8 of the 12 analog inputs are regular and the other 4 are direct SC block connections. Updated the Development Tool Selection section. Improved the bookmark structure. Edited F_{IMO6}, T_{ERASEB}, T_{WRITE}, T_{RSCLK}, T_{FSCLK}, V_{IHP}, V_{PPORxR}, and 5 V RefLo specifications according to MASJ input. Removed ‘TM’ from Programmable System-on-Chip in the title.
*C	2822792	BTK/ AESA	12/07/2009	Added T_{PRGH}, T_{PRGC}, I_{OL}, I_{OH}, F_{32KU}, DC_{ILO}, and $T_{POWERUP}$ electrical specifications. Updated the footnotes for the DC Programming Specifications table. Added maximum values and updated typical values for T_{ERASEB} and T_{WRITE} electrical specifications. Replaced T_{RAMP} electrical specification with $SR_{POWERUP}$ electrical specification. Added “Contents” on page 2.
*D	2888007	NJF	03/30/2010	Updated Cypress website links. Added $T_{BAKETEMP}$ and $T_{BAKETIME}$ parameters in Absolute Maximum Ratings Updated Packaging Information. Updated Ordering Code Definitions. Removed Third Party Tools and Build a PSoC Emulator into your Board. Updated Development Kits and Evaluation Tools. Updated links in Sales, Solutions, and Legal Information.
*E	2987146	BTK	07/19/2010	Updated Pinouts section to add 48-pin package. Updated Packaging Information section to add 48-pin package. Updated Development Tool Selection section to add 48-pin package development tool information. Updated Ordering Information section to add new 48-pin package product. Moved Acronyms section to the end of the document. Added part number CY8C29666 to the title.
*F	3111512	BTK/NJF	07/25/2011	Updated I^2C timing diagram to improve clarity. Updated wording, formatting, and notes of the AC Digital Block Specifications table to improve clarity. Added V_{DDP}, V_{DDLV}, and V_{DDHV} electrical specifications to give more information for programming the device. Updated solder reflow temperature specifications to give more clarity. Updated the jitter specifications. Updated PSoC Device Characteristics table. Updated the F_{32KU} electrical specification. Updated note for R_{PD} electrical specification. Updated note for the T_{STG} electrical specification to add more clarity. Added Tape and Reel Information section. Added C_L electrical specification. Updated Analog Reference specifications. Updated V_{OSOA}, TCV_{OSOA}, V_{OSOB}, and TCV_{OSOB} electrical specifications.
*G	3543452	KAUL	03/06/2012	Updated Tape and Reel Information under Packaging Information.

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