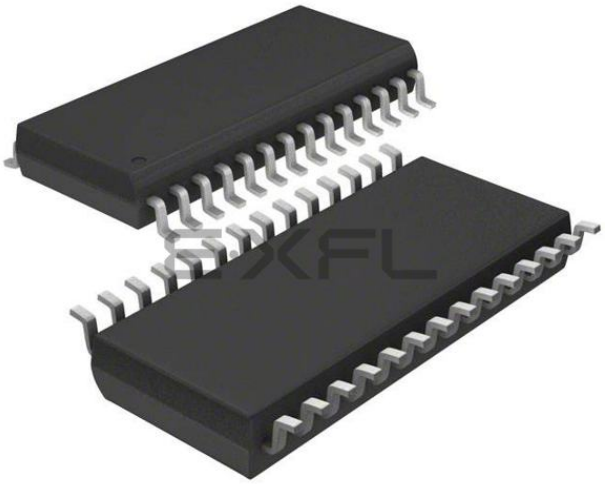

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	24
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.25V
Data Converters	A/D 12x14b; D/A 4x9b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c29466-24pvxat

The Analog System

The analog system is composed of 12 configurable blocks, each comprised of an opamp circuit allowing the creation of complex analog signal flows. Analog peripherals are very flexible and can be customized to support specific application requirements. Some of the common PSoC analog functions for this device (most available as user modules) are as follows:

- ADCs (up to four, with 6- to 14-bit resolution, selectable as incremental, delta-sigma, or successive approximation register (SAR))
- Filters (two- and four-pole band pass, low pass, and notch)
- Amplifiers (up to four, with selectable gain up to 48x)
- Instrumentation amplifiers (up to two, with selectable gain up to 93x)
- Comparators (up to four, with 16 selectable thresholds)
- DACs (up to four, with 6- to 9-bit resolution)
- Multiplying DACs (up to four, with 6- to 9-bit resolution)
- High current output drivers (four with 30-mA drive)
- 1.3-V reference (as a system resource)
- DTMF Dialer
- Modulators
- Correlators
- Peak Detectors
- Many other topologies possible

Analog blocks are provided in columns of three, which includes one continuous time (CT) and two switched capacitor (SC) blocks, as shown in Figure 2.

Figure 2. Analog System Block Diagram

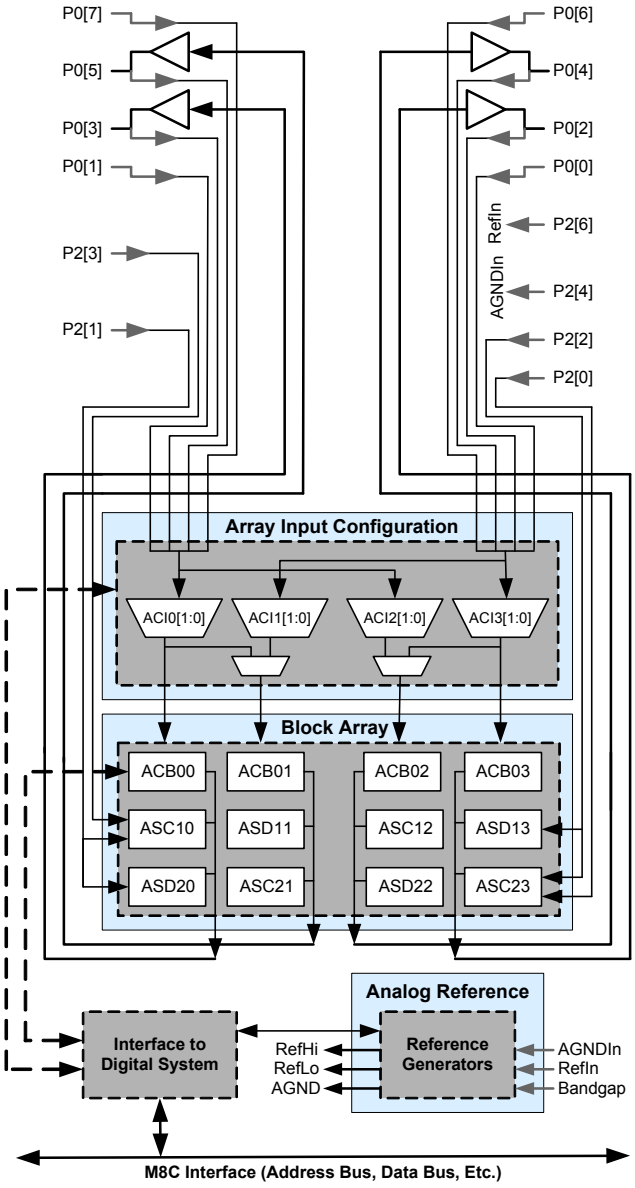


Table 6. Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW	DBB20FN	40	RW	ASC10CR0	80	RW	RDI2RI	C0	RW
PRT0DM1	01	RW	DBB20IN	41	RW	ASC10CR1	81	RW	RDI2SYN	C1	RW
PRT0IC0	02	RW	DBB20OU	42	RW	ASC10CR2	82	RW	RDI2IS	C2	RW
PRT0IC1	03	RW		43		ASC10CR3	83	RW	RDI2LT0	C3	RW
PRT1DM0	04	RW	DBB21FN	44	RW	ASD11CR0	84	RW	RDI2LT1	C4	RW
PRT1DM1	05	RW	DBB21IN	45	RW	ASD11CR1	85	RW	RDI2RO0	C5	RW
PRT1IC0	06	RW	DBB21OU	46	RW	ASD11CR2	86	RW	RDI2RO1	C6	RW
PRT1IC1	07	RW		47		ASD11CR3	87	RW		C7	
PRT2DM0	08	RW	DCB22FN	48	RW	ASC12CR0	88	RW	RDI3RI	C8	RW
PRT2DM1	09	RW	DCB22IN	49	RW	ASC12CR1	89	RW	RDI3SYN	C9	RW
PRT2IC0	0A	RW	DCB22OU	4A	RW	ASC12CR2	8A	RW	RDI3IS	CA	RW
PRT2IC1	0B	RW		4B		ASC12CR3	8B	RW	RDI3LT0	CB	RW
PRT3DM0	0C	RW	DCB23FN	4C	RW	ASD13CR0	8C	RW	RDI3LT1	CC	RW
PRT3DM1	0D	RW	DCB23IN	4D	RW	ASD13CR1	8D	RW	RDI3RO0	CD	RW
PRT3IC0	0E	RW	DCB23OU	4E	RW	ASD13CR2	8E	RW	RDI3RO1	CE	RW
PRT3IC1	0F	RW		4F		ASD13CR3	8F	RW		CF	
PRT4DM0	10	RW	DBB30FN	50	RW	ASD20CR0	90	RW	GDI_O_IN	D0	RW
PRT4DM1	11	RW	DBB30IN	51	RW	ASD20CR1	91	RW	GDI_E_IN	D1	RW
PRT4IC0	12	RW	DBB30OU	52	RW	ASD20CR2	92	RW	GDI_O_OU	D2	RW
PRT4IC1	13	RW		53		ASD20CR3	93	RW	GDI_E_OU	D3	RW
PRT5DM0	14	RW	DBB31FN	54	RW	ASC21CR0	94	RW		D4	
PRT5DM1	15	RW	DBB31IN	55	RW	ASC21CR1	95	RW		D5	
PRT5IC0	16	RW	DBB31OU	56	RW	ASC21CR2	96	RW		D6	
PRT5IC1	17	RW		57		ASC21CR3	97	RW		D7	
	18		DCB32FN	58	RW	ASD22CR0	98	RW		D8	
	19		DCB32IN	59	RW	ASD22CR1	99	RW		D9	
	1A		DCB32OU	5A	RW	ASD22CR2	9A	RW		DA	
	1B			5B		ASD22CR3	9B	RW		DB	
	1C		DCB33FN	5C	RW	ASC23CR0	9C	RW		DC	
	1D		DCB33IN	5D	RW	ASC23CR1	9D	RW	OSC_GO_EN	DD	RW
	1E		DCB33OU	5E	RW	ASC23CR2	9E	RW	OSC_CR4	DE	RW
	1F			5F		ASC23CR3	9F	RW	OSC_CR3	DF	RW
DBB00FN	20	RW	CLK_CR0	60	RW		A0		OSC_CR0	E0	RW
DBB00IN	21	RW	CLK_CR1	61	RW		A1		OSC_CR1	E1	RW
DBB00OU	22	RW	ABF_CR0	62	RW		A2		OSC_CR2	E2	RW
	23		AMD_CR0	63	RW		A3		VLT_CR	E3	RW
DBB01FN	24	RW		64			A4		VLT_CMP	E4	R
DBB01IN	25	RW		65			A5			E5	
DBB01OU	26	RW	AMD_CR1	66	RW		A6			E6	
	27		ALT_CR0	67	RW		A7			E7	
DCB02FN	28	RW	ALT_CR1	68	RW		A8		IMO_TR	E8	W
DCB02IN	29	RW	CLK_CR2	69	RW		A9		ILO_TR	E9	W
DCB02OU	2A	RW		6A			AA		BDG_TR	EA	RW
	2B			6B			AB		ECO_TR	EB	W
DCB03FN	2C	RW	TMP_DR0	6C	RW		AC			EC	
DCB03IN	2D	RW	TMP_DR1	6D	RW		AD			ED	
DCB03OU	2E	RW	TMP_DR2	6E	RW		AE			EE	
	2F		TMP_DR3	6F	RW		AF			EF	
DBB10FN	30	RW	ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
DBB10IN	31	RW	ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
DBB10OU	32	RW	ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
DBB11FN	34	RW	ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
DBB11IN	35	RW	ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
DBB11OU	36	RW	ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
	37		ACB01CR2	77	RW		B7		CPU_F	F7	RL
DCB12FN	38	RW	ACB02CR3	78	RW	RDI1RI	B8	RW		F8	
DCB12IN	39	RW	ACB02CR0	79	RW	RDI1SYN	B9	RW		F9	
DCB12OU	3A	RW	ACB02CR1	7A	RW	RDI1IS	BA	RW	FLS_PR1	FA	RW
	3B		ACB02CR2	7B	RW	RDI1LT0	BB	RW		FB	
DCB13FN	3C	RW	ACB03CR3	7C	RW	RDI1LT1	BC	RW		FC	
DCB13IN	3D	RW	ACB03CR0	7D	RW	RDI1RO0	BD	RW		FD	
DCB13OU	3E	RW	ACB03CR1	7E	RW	RDI1RO1	BE	RW	CPU_SCR1	FE	#
	3F		ACB03CR2	7F	RW		BF		CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed. # Access is bit specific.

Table 10. DC GPIO Specifications (continued)

Symbol	Description	Min	Typ	Max	Units	Notes
V_H	Input hysteresis	–	60	–	mV	
I_{IL}	Input leakage (absolute value)	–	1	–	nA	Gross tested to 1 µA.
C_{IN}	Capacitive load on pins as input	–	3.5	10	pF	Package and pin dependent. T_A = 25 °C.
C_{OUT}	Capacitive load on pins as output	–	3.5	10	pF	Package and pin dependent. T_A = 25 °C.

DC Operational Amplifier Specifications

Table 11 and Table 12 on page 18 list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

The operational amplifier is a component of both the analog CT PSoC blocks and the analog SC PSoC blocks. The guaranteed specifications are measured in the analog CT PSoC block. Typical parameters apply to 5 V at 25 °C and are for design guidance only.

Power = high and Opamp bias = high settings are not allowed together for 3.3 V V_{DD} operation.

Table 11. 5-V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input offset voltage (absolute value)	–	1.6	10	mV	
TCV_{OSOA}	Average input offset voltage drift	–	4.0	23.0	µV/°C	
I_{EBOA}	Input leakage current (Port 0 analog pins)	–	200	–	pA	Gross tested to 1 µA.
C_{INOA}	Input capacitance (Port 0 analog pins)	–	4.5	9.5	pF	Package and pin dependent. T_A = 25 °C.
V_{CMOA}	Common-mode voltage range All cases, except highest Power = high, Opamp bias = high	 0.0 0.5	 – –	 V_{DD} V_{DD} – 0.5	 V V	
$CMRR_{OA}$	Common-mode rejection ratio	60	–	–	dB	This specification is measured through the analog output buffer and therefore includes the limitations imposed by the characteristics of the analog output buffer.
G_{OLOA}	Open loop gain	80	–	–	dB	
$V_{OHIGHOA}$	High output voltage swing (internal signals)	V_{DD} – 0.01	–	–	V	
V_{OLOWOA}	Low output voltage swing (internal signals)	–	–	0.01	V	
I_{SOA}	Supply current (including associated AGND buffer) Power = low, Opamp bias = low Power = low, Opamp bias = high Power = medium, Opamp bias = low Power = medium, Opamp bias = high Power = high, Opamp bias = low Power = high, Opamp bias = high	 – – – – – –	 150 300 600 1200 2400 4600	 200 400 800 1600 3200 6400	 µA µA µA µA µA µA	
$PSRR_{OA}$	Supply voltage rejection ratio	67	80	–	dB	$V_{SS} \le V_{IN} \le (V_{DD} – 2.25)$ or $(V_{DD} – 1.25\ V) \le V_{IN} \le V_{DD}$.

Table 15. 3.3-V DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOB}	Input offset voltage (absolute value) Power = low Power = high	 – –	 3.2 6.0	 20.0 25.0	 mV mV	High power setting is not recommended.
TCV_{OSOB}	Average input offset voltage drift Power = low Power = high	 – –	 8.0 12.0	 32.0 41.0	 µV/°C µV/°C	
V_{CMOB}	Common-mode input voltage range	0.5	–	V_{DD} – 1.0	V	
R_{OUTOB}	Output resistance Power = low Power = high	 – –	 – –	 10 10	 Ω Ω	
$V_{OHIGHOB}$	High output voltage swing (load = 1 kΩ to $V_{DD}/2$) Power = low Power = high	 0.5 × V_{DD} + 1.0 0.5 × V_{DD} + 1.0	 – –	 – –	 V V	
V_{OLOWOB}	Low output voltage swing (load = 1 kΩ to $V_{DD}/2$) Power = low Power = high	 – –	 – –	 0.5 × V_{DD} – 1.0 0.5 × V_{DD} – 1.0	 V V	
I_{SOB}	Supply current including bias cell (no load) Power = low Power = high	 – –	 0.8 2.0	 1 5	 mA mA	
$PSRR_{OB}$	Power supply rejection ratio	60	64	–	dB	
C_L	Load capacitance	–	–	200	pF	This specification applies to the external circuit driven by the analog output buffer.

Table 16. 5-V DC Analog Reference Specifications(continued)

Reference ARF_CR[5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Unit
0b001	RefPower = High Opamp bias = High	V_{REFHI}	Ref High	P2[4] + P2[6] ($P2[4] = V_{DD}/2$, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.085	P2[4] + P2[6] – 0.016	P2[4] + P2[6] + 0.044	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – P2[6] ($P2[4] = V_{DD}/2$, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.022	P2[4] – P2[6] + 0.010	P2[4] – P2[6] + 0.055	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref High	P2[4] + P2[6] ($P2[4] = V_{DD}/2$, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.077	P2[4] + P2[6] – 0.010	P2[4] + P2[6] + 0.051	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – P2[6] ($P2[4] = V_{DD}/2$, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.022	P2[4] – P2[6] + 0.005	P2[4] – P2[6] + 0.039	V
	RefPower = Med Opamp bias = High	V_{REFHI}	Ref High	P2[4] + P2[6] ($P2[4] = V_{DD}/2$, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.070	P2[4] + P2[6] – 0.010	P2[4] + P2[6] + 0.050	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – P2[6] ($P2[4] = V_{DD}/2$, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.022	P2[4] – P2[6] + 0.005	P2[4] – P2[6] + 0.039	V
	RefPower = Med Opamp bias = Low	V_{REFHI}	Ref High	P2[4] + P2[6] ($P2[4] = V_{DD}/2$, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.070	P2[4] + P2[6] – 0.007	P2[4] + P2[6] + 0.054	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – P2[6] ($P2[4] = V_{DD}/2$, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.022	P2[4] – P2[6] + 0.002	P2[4] – P2[6] + 0.032	V
0b010	RefPower = High Opamp bias = High	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.037	V_{DD} – 0.009	V_{DD}	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.061	$V_{DD}/2$ – 0.006	$V_{DD}/2$ + 0.047	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.007	V_{SS} + 0.028	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.039	V_{DD} – 0.006	V_{DD}	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.049	$V_{DD}/2$ – 0.005	$V_{DD}/2$ + 0.036	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.005	V_{SS} + 0.019	V
	RefPower = Med Opamp bias = High	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.037	V_{DD} – 0.007	V_{DD}	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.054	$V_{DD}/2$ – 0.005	$V_{DD}/2$ + 0.041	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.006	V_{SS} + 0.024	V
	RefPower = Med Opamp bias = Low	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.042	V_{DD} – 0.005	V_{DD}	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.046	$V_{DD}/2$ – 0.004	$V_{DD}/2$ + 0.034	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.004	V_{SS} + 0.017	V

Table 17. 3.3-V DC Analog Reference Specifications (continued)

Reference ARF_CR[5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Unit
0b110	RefPower = High Opamp bias = High	V_{REFHI}	Ref High	2 × BandGap	2.507	2.598	2.698	V
		V_{AGND}	AGND	BandGap	1.203	1.307	1.424	V
		V_{REFLO}	Ref Low	Vss	Vss	Vss + 0.012	Vss + 0.067	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref High	2 × BandGap	2.516	2.598	2.683	V
		V_{AGND}	AGND	BandGap	1.241	1.303	1.376	V
		V_{REFLO}	Ref Low	Vss	Vss	Vss + 0.007	Vss + 0.040	V
	RefPower = Med Opamp bias = High	V_{REFHI}	Ref High	2 × BandGap	2.510	2.599	2.693	V
		V_{AGND}	AGND	BandGap	1.240	1.305	1.374	V
		V_{REFLO}	Ref Low	Vss	Vss	Vss + 0.008	Vss + 0.048	V
	RefPower = Med Opamp bias = Low	V_{REFHI}	Ref High	2 × BandGap	2.515	2.598	2.683	V
		V_{AGND}	AGND	BandGap	1.258	1.302	1.355	V
		V_{REFLO}	Ref Low	Vss	Vss	Vss + 0.005	Vss + 0.03	V
0b111	All power settings. Not allowed for 3.3 V.	–	–	–	–	–	–	–

DC Analog PSoC Block Specifications

Table 18 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 18. DC Analog PSoC Block Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{CT}	Resistor unit value (continuous time)	–	12.2	–	kΩ	
C_{SC}	Capacitor unit value (switch cap)	–	80	–	fF	

DC POR and LVD Specifications

Table 19 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 19. DC POR and LVD Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
	V_{DD} value for PPOR trip (negative ramp)					
V_{PPOR0}	PORLEV[1:0] = 00b	–	2.82	–	V	
V_{PPOR1}	PORLEV[1:0] = 01b	–	4.39	–	V	
V_{PPOR2}	PORLEV[1:0] = 10b	–	4.55	–	V	
	PPOR hysteresis					
V_{PH0}	PORLEV[1:0] = 00b	–	92	–	mV	
V_{PH1}	PORLEV[1:0] = 01b	–	0	–	mV	
V_{PH2}	PORLEV[1:0] = 10b	–	0	–	mV	
	V_{DD} value for LVD trip					
V_{LVD0}	VM[2:0] = 000b	2.86	2.92	2.98[7]	V	
V_{LVD1}	VM[2:0] = 001b	2.96	3.02	3.08	V	
V_{LVD2}	VM[2:0] = 010b	3.07	3.13	3.20	V	
V_{LVD3}	VM[2:0] = 011b	3.92	4.00	4.08	V	
V_{LVD4}	VM[2:0] = 100b	4.39	4.48	4.57	V	
V_{LVD5}	VM[2:0] = 101b	4.55	4.64	4.74[8]	V	
V_{LVD6}	VM[2:0] = 110b	4.63	4.73	4.82	V	
V_{LVD7}	VM[2:0] = 111b	4.72	4.81	4.91	V	

Notes
7. Always greater than 50 mV above PPOR (PORLEV = 00) for falling supply.
8. Always greater than 50 mV above PPOR (PORLEV = 10) for falling supply.

DC Programming Specifications

Table 20 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 20. DC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{DDP}	V_{DD} for programming and erase	4.5	5.0	5.5	V	This specification applies to the functional requirements of external programmer tools.
V_{DDLV}	Low V_{DD} for verify	3.0	3.1	3.2	V	This specification applies to the functional requirements of external programmer tools.
V_{DDHV}	High V_{DD} for verify	5.1	5.2	5.3	V	This specification applies to the functional requirements of external programmer tools.
$V_{DDIWRITE}$	Supply voltage for flash write operation	3.0	–	5.25	V	This specification applies to this device when it is executing internal flash writes.
I_{DDP}	Supply current during programming or verify	–	10	30	mA	
V_{ILP}	Input low voltage during programming or verify	–	–	0.8	V	
V_{IHP}	Input high voltage during programming or verify	2.1	–	–	V	
I_{ILP}	Input current when applying V_{ILP} to P1[0] or P1[1] during programming or verify	–	–	0.2	mA	Driving internal pull-down resistor.
I_{IHP}	Input current when applying V_{IHP} to P1[0] or P1[1] during programming or verify	–	–	1.5	mA	Driving internal pull-down resistor.
V_{OLV}	Output low voltage during programming or verify	–	–	0.75	V	
V_{OHV}	Output high voltage during programming or verify	V_{DD} – 1.0	–	V_{DD}	V	
$Flash_{ENPB}$	Flash endurance (per block)[9, 10]	1,000	–	–	–	Erase/write cycles per block.
$Flash_{ENT}$	Flash endurance (total)[10, 11]	512,000	–	–	–	Erase/write cycles.
$Flash_{DR}$	Flash data retention	15	–	–	Years	

Notes
9. The erase/write cycle limit per block ($Flash_{ENPB}$) is only guaranteed if the device operates within one voltage range. Voltage ranges are 3.0 V to 3.6 V and 4.75 V to 5.25 V.
10. For the full temperature range, the user must employ a temperature sensor user module (FlashTemp) or other temperature sensor, and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 for more information.
11. The maximum total number of allowed erase/write cycles is the minimum $Flash_{ENPB}$ value multiplied by the number of flash blocks in the device.

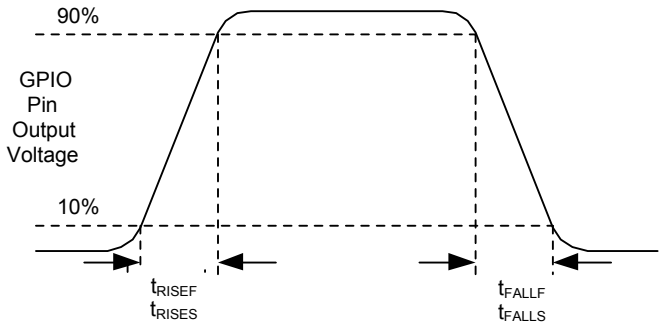
AC GPIO Specifications

Table 22 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 22. AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO operating frequency	0	–	12.6[15]	MHz	Normal strong mode
t_{RISEF}	Rise time, normal strong mode, Cload = 50 pF	3	–	18	ns	V_{DD} = 4.75 to 5.25 V, 10% - 90%
t_{FALLF}	Fall time, normal strong mode, Cload = 50 pF	2	–	18	ns	V_{DD} = 4.75 to 5.25 V, 10% - 90%
t_{RISES}	Rise time, slow strong mode, Cload = 50 pF	10	27	–	ns	V_{DD} = 3 to 5.25 V, 10% - 90%
t_{FALLS}	Fall time, slow strong mode, Cload = 50 pF	10	22	–	ns	V_{DD} = 3 to 5.25 V, 10% - 90%

Figure 10. GPIO Timing Diagram



Note
15. Accuracy derived from IMO with appropriate trim for V_{DD} range.

AC Operational Amplifier Specifications

Table 23 and Table 24 list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Settling times, slew rates, and gain bandwidth are based on the analog CT PSoC block.

Power = high and Opamp bias = high is not supported at 3.3 V.

Table 23. 5-V AC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{ROA}	Rising settling time to 0.1% for a 1-V step (10 pF load, unity gain) Power = low, Opamp bias = low Power = medium, Opamp bias = high Power = high, Opamp bias = high	 – – –	 – – –	 3.9 0.72 0.62	 µs µs µs	
t_{SOA}	Falling settling time to 0.1% for a 1-V step (10 pF load, unity gain) Power = low, Opamp bias = low Power = medium, Opamp bias = high Power = high, Opamp bias = high	 – – –	 – – –	 5.9 0.92 0.72	 µs µs µs	
SR_{ROA}	Rising slew rate (20% to 80%) of a 1-V step (10 pF load, unity gain) Power = low, Opamp bias = low Power = medium, Opamp bias = high Power = high, Opamp bias = high	 0.15 1.7 6.5	 – – –	 – – –	 V/µs V/µs V/µs	
SR_{FOA}	Falling slew rate (80% to 20%) of a 1-V step (10 pF load, unity gain) Power = low, Opamp bias = low Power = medium, Opamp bias = high Power = high, Opamp bias = high	 0.01 0.5 4.0	 – – –	 – – –	 V/µs V/µs V/µs	
BW_{OA}	Gain bandwidth product Power = low, Opamp bias = low Power = medium, Opamp bias = high Power = high, Opamp bias = high	 0.75 3.1 5.4	 – – –	 – – –	 MHz MHz MHz	
E_{NOA}	Noise at 1 kHz (Power = medium, Opamp bias = high)	–	100	–	nV/rt-Hz	

Table 24. 3.3-V AC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{ROA}	Rising settling time to 0.1% of a 1-V step (10 pF load, unity gain) Power = low, Opamp bias = low Power = medium, Opamp bias = high	 – –	 – –	 3.92 0.72	 µs µs	
t_{SOA}	Falling settling time to 0.1% of a 1-V step (10 pF load, unity gain) Power = low, Opamp bias = low Power = medium, Opamp bias = high	 – –	 – –	 5.41 0.72	 µs µs	
SR_{ROA}	Rising slew rate (20% to 80%) of a 1-V step (10 pF load, unity gain) Power = low, Opamp bias = low Power = medium, Opamp bias = high	 0.31 2.7	 – –	 – –	 V/µs V/µs	
SR_{FOA}	Falling slew rate (80% to 20%) of a 1-V step (10 pF load, unity gain) Power = low, Opamp bias = low Power = medium, Opamp bias = high	 0.24 1.8	 – –	 – –	 V/µs V/µs	
BW_{OA}	Gain bandwidth product Power = low, Opamp bias = low Power = medium, Opamp bias = high	 0.67 2.8	 – –	 – –	 MHz MHz	
E_{NOA}	Noise at 1 kHz (Power = medium, Opamp bias = high)	–	100	–	nV/rt-Hz	

AC Low-Power Comparator Specifications

Table 25 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V at 25 °C and are for design guidance only.

Table 25. AC Low-Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{RLPC}	LPC response time	–	–	50	µs	≥ 50 mV overdrive comparator reference set within V_{REFLPC}.

AC Digital Block Specifications

Table 26 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 26. AC Digital Block Specifications

Function	Description	Min	Typ	Max	Units	Notes
All functions	Block input clock frequency					
	V_{DD} ≥ 4.75 V	–	–	50.4[17]	MHz	
	V_{DD} < 4.75 V	–	–	25.2[17]	MHz	
Timer	Input clock frequency					
	No capture, V_{DD} ≥ 4.75 V	–	–	50.4[17]	MHz	
	No capture, V_{DD} < 4.75 V	–	–	25.2[17]	MHz	
	With capture	–	–	25.2[17]	MHz	
	Capture pulse width	50[16]	–	–	ns	
Counter	Input clock frequency					
	No enable input, V_{DD} ≥ 4.75 V	–	–	50.4[17]	MHz	
	No enable input, V_{DD} < 4.75 V	–	–	25.2[17]	MHz	
	With enable input	–	–	25.2[17]	MHz	
	Enable input pulse width	50[16]	–	–	ns	
Dead Band	Kill pulse width					
	Asynchronous restart mode	20	–	–	ns	
	Synchronous restart mode	50[16]	–	–	ns	
	Disable mode	50[16]	–	–	ns	
	Input clock frequency					
	V_{DD} ≥ 4.75 V	–	–	50.4[17]	MHz	
	V_{DD} < 4.75 V	–	–	25.2[17]	MHz	
CRCPRS (PRS Mode)	Input clock frequency					
	V_{DD} ≥ 4.75 V	–	–	50.4[17]	MHz	
	V_{DD} < 4.75 V	–	–	25.2[17]	MHz	
CRCPRS (CRC Mode)	Input clock frequency	–	–	25.2[17]	MHz	
SPIM	Input clock frequency	–	–	8.4[17]	MHz	The SPI serial clock (SCLK) frequency is equal to the input clock frequency divided by 2.
SPIS	Input clock (SCLK) frequency	–	–	4.2[17]	MHz	The input clock is the SPI SCLK in SPIS mode.
	Width of SS_Negated between transmissions	50[16]	–	–	ns	
Transmitter	Input clock frequency					The baud rate is equal to the input clock frequency divided by 8.
	V_{DD} ≥ 4.75 V, 2 stop bits	–	–	50.4[17]	MHz	
	V_{DD} ≥ 4.75 V, 1 stop bit	–	–	25.2[17]	MHz	
	V_{DD} < 4.75 V	–	–	25.2[17]	MHz	

Notes
16. 50 ns minimum input pulse width is based on the input synchronizers running at 24 MHz (42 ns nominal period).
17. Accuracy derived from IMO with appropriate trim for V_{DD} range.

Table 26. AC Digital Block Specifications (continued)

Function	Description	Min	Typ	Max	Units	Notes
Receiver	Input clock frequency					The baud rate is equal to the input clock frequency divided by 8.
	$V_{DD} \geq 4.75$ V, 2 stop bits	–	–	50.4[18]	MHz	
	$V_{DD} \geq 4.75$ V, 1 stop bit	–	–	25.2[18]	MHz	
	$V_{DD} < 4.75$ V	–	–	25.2[18]	MHz	

AC Analog Output Buffer Specifications

Table 27 and Table 28 list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 27. 5-V AC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{ROB}	Rising settling time to 0.1%, 1-V step, 100 pF load					
	Power = low	–	–	4	µs	
	Power = high	–	–	4	µs	
t_{SOB}	Falling settling time to 0.1%, 1-V step, 100 pF load					
	Power = low	–	–	3.4	µs	
	Power = high	–	–	3.4	µs	
SR_{ROB}	Rising slew rate (20% to 80%), 1-V step, 100 pF load					
	Power = low	0.5	–	–	V/µs	
	Power = high	0.5	–	–	V/µs	
SR_{FOB}	Falling slew rate (80% to 20%), 1-V step, 100 pF load					
	Power = low	0.55	–	–	V/µs	
	Power = high	0.55	–	–	V/µs	
BW_{OB}	Small signal bandwidth, 20 mV_{pp}, 3 dB BW, 100 pF load					
	Power = low	0.8	–	–	MHz	
	Power = high	0.8	–	–	MHz	
BW_{OB}	Large signal bandwidth, 1 V_{pp}, 3 dB BW, 100 pF load					
	Power = low	300	–	–	kHz	
	Power = high	300	–	–	kHz	

Table 28. 3.3-V AC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{ROB}	Rising settling time to 0.1%, 1-V step, 100 pF load					
	Power = low	–	–	4.7	µs	
	Power = high	–	–	4.7	µs	
t_{SOB}	Falling settling time to 0.1%, 1-V step, 100 pF load					
	Power = low	–	–	4	µs	
	Power = high	–	–	4	µs	
SR_{ROB}	Rising slew rate (20% to 80%), 1-V step, 100 pF load					
	Power = low	0.36	–	–	V/µs	
	Power = high	0.36	–	–	V/µs	
SR_{FOB}	Falling slew rate (80% to 20%), 1-V step, 100 pF load					
	Power = low	0.4	–	–	V/µs	
	Power = high	0.4	–	–	V/µs	
BW_{OB}	Small signal bandwidth, 20 mV_{pp}, 3 dB BW, 100 pF load					
	Power = low	0.7	–	–	MHz	
	Power = high	0.7	–	–	MHz	
BW_{OB}	Large signal bandwidth, 1 V_{pp}, 3 dB BW, 100 pF load					
	Power = low	200	–	–	kHz	
	Power = high	200	–	–	kHz	

Note
18. Accuracy derived from IMO with appropriate trim for V_{DD} range.

AC External Clock Specifications

Table 29 and Table 30 list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 29. 5-V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency	0.093	–	24.6	MHz	
–	High period	20.6	–	5300	ns	
–	Low period	20.6	–	–	ns	
–	Power-up IMO to switch	150	–	–	µs	

Table 30. 3.3-V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency with CPU clock divide by 1	0.093	–	12.3	MHz	Maximum CPU frequency is 12 MHz at 3.3 V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.
F_{OSCEXT}	Frequency with CPU clock divide by 2 or greater	0.093	–	24.6	MHz	If the frequency of the external clock is greater than 12 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider will ensure that the fifty percent duty cycle requirement is met.
–	High period with CPU Clock divide by 1	41.7	–	5300	ns	
–	Low period with CPU Clock divide by 1	41.7	–	–	ns	
–	Power-up IMO to switch	150	–	–	µs	

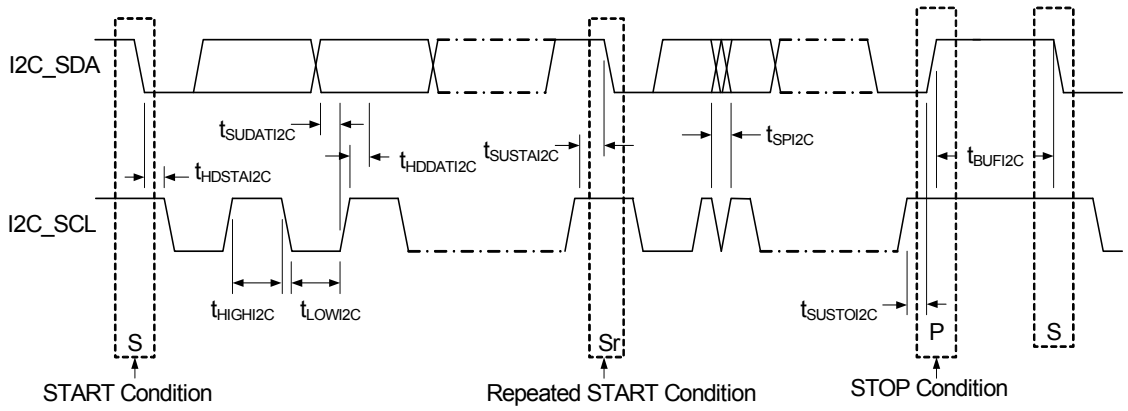
AC I²C Specifications

Table 32 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 32. AC Characteristics of the I²C SDA and SCL Pins

Symbol	Description	Standard Mode		Fast Mode		Units	Notes
		Min	Max	Min	Max		
F_{SCLI2C}	SCL clock frequency	0	100[20]	0	400[20]	kHz	
$t_{HDSTAI2C}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	4.0	–	0.6	–	µs	
t_{LOWI2C}	LOW period of the SCL clock	4.7	–	1.3	–	µs	
$t_{HIGHI2C}$	HIGH period of the SCL clock	4.0	–	0.6	–	µs	
$t_{SUSTAI2C}$	Setup time for a repeated START condition	4.7	–	0.6	–	µs	
$t_{HDDATI2C}$	Data hold time	0	–	0	–	µs	
$t_{SUDATI2C}$	Data setup time	250	–	100[21]	–	ns	
$t_{SUSTOI2C}$	Setup time for STOP condition	4.0	–	0.6	–	µs	
t_{BUFI2C}	Bus-free time between a STOP and START condition	4.7	–	1.3	–	µs	
t_{SPI2C}	Pulse width of spikes are suppressed by the input filter.	–	–	0	50	ns	

Figure 13. Definition for Timing for Fast/Standard Mode on the I²C Bus



Notes

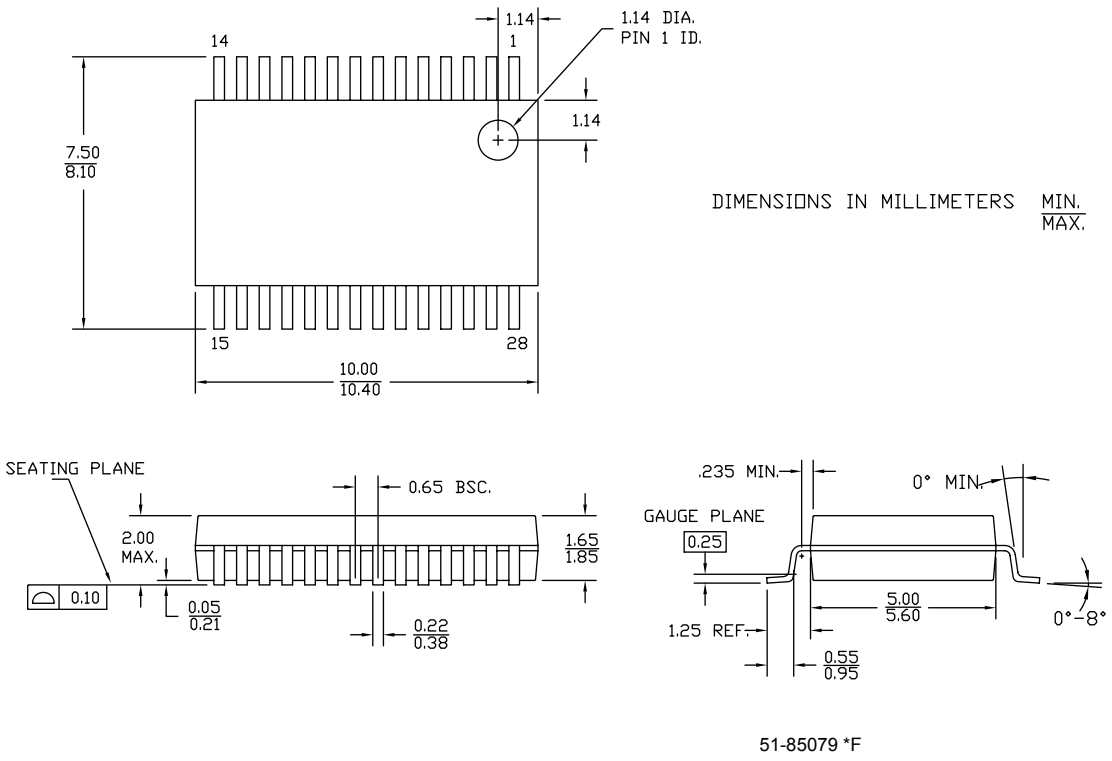
20. F_{SCLI2C} is derived from SysClk of the PSoC. This specification assumes that SysClk is operating at 24 MHz, nominal. If SysClk is at a lower frequency, then the F_{SCLI2C} specification adjusts accordingly.
21. A Fast-Mode I²C-bus device can be used in a Standard-Mode I²C-bus system, but the requirement $t_{SUDATI2C} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SUDATI2C} = 1000 + 250 = 1250$ ns (according to the Standard-Mode I²C-bus specification) before the SCL line is released.

Packaging Information

This section illustrates the packaging specifications for the automotive CY8C29x66 PSoC device, along with the thermal impedances and solder reflow for each package and the typical package capacitance on crystal pins.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the emulator pod drawings at http://www.cypress.com.

Figure 14. 28-Pin (210-Mil) SSOP



51-85079 *F

Device Programmers

All device programmers can be purchased from the Cypress Online Store. The online store also has the most up to date information on kit contents, descriptions, and availability.

CY3210-MiniProg1

The CY3210-MiniProg1 kit allows a user to program PSoC devices through the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC via a provided USB 2.0 cable. The kit includes:

- MiniProg programming unit
- MiniEval socket programming and evaluation board
- 28-pin CY8C29466-24PXI PDIP PSoC device sample
- PSoC Designer software CD
- Getting Started guide
- USB 2.0 cable

CY3207ISSP In-System Serial Programmer (ISSP)

The CY3207ISSP is a production programmer. It includes protection circuitry and an industrial case that is more robust than the MiniProg in a production-programming environment.

Note: CY3207ISSP needs special software and is not compatible with PSoC Programmer. This software is free and can be downloaded from http://www.cypress.com. The kit includes:

- CY3207 programmer unit
- PSoC ISSP software CD
- 110 ~ 240-V power supply, Euro-Plug adapter
- USB 2.0 cable

Accessories (Emulation and Programming)

Table 37. Emulation and Programming Accessories

Part Number	Pin Package	Pod Kit[23]	Foot Kit[24]	Adapter[25]
CY8C29466-24PVXA	28-pin SSOP	CY3250-29XXX	CY3250-28SSOP-FK	AS-28-28-02SS-6ENP-GANG
CY8C29666-24PVXA	48-pin SSOP	CY3250-29XXX	CY3250-48SSOP-FK	AS-48-48-01SS-6-GANG

Notes
23. Pod kit contains an emulation pod, a flex-cable (connects the pod to the ICE), two feet, and device samples.
24. Foot kit includes surface mount feet that can be soldered to the target PCB.
25. Programming adapter converts non-DIP package to DIP footprint. Specific details and ordering information for each of the adapters are available at http://www.emulation.com.

Reference Information

Acronyms

The following table lists the acronyms that are used in this document.

Table 39. Acronyms Used in this Datasheet

Acronym	Description	Acronym	Description
AC	alternating current	LVD	low-voltage detect
ADC	analog-to-digital converter	MAC	multiply accumulate
AEC	Automotive Electronics Council	MCU	microcontroller unit
API	application programming interface	MIPS	million instructions per second
CMOS	complementary metal oxide semiconductor	PCB	printed circuit board
CPU	central processing unit	PDIP	plastic dual-in-line package
CRC	cyclic redundancy check	PGA	programmable gain amplifier
CT	continuous time	PLL	phase-locked loop
DAC	digital-to-analog converter	POR	power-on reset
DC	direct current	PPOR	precision POR
DTMF	dual-tone multi-frequency	PRS	pseudo-random sequence
ECO	external crystal oscillator	PSoC®	Programmable System-on-Chip
EEPROM	electrically erasable programmable read-only memory	PWM	pulse-width modulator
GPIO	general-purpose I/O	RTC	real time clock
I/O	input/output	SAR	successive approximation register
ICE	in-circuit emulator	SC	switched capacitor
IDE	integrated development environment	SLIMO	slow IMO
I^2C	inter-integrated circuit	SPI	serial peripheral interface
ILO	internal low-speed oscillator	SRAM	static random-access memory
IMO	internal main oscillator	SROM	supervisory read-only memory
IP	intellectual property	SSOP	shrink small-outline package
IrDA	infrared data association	UART	universal asynchronous receiver transmitter
ISSP	in-system serial programming	USB	universal serial bus
LCD	liquid crystal display	WDT	watchdog timer
LED	light-emitting diode	XRES	external reset
LPC	low power comparator		

Reference Documents

CY8CPLC20, CY8CLED16P01, CY8C29x66, CY8C27x43, CY8C24x94, CY8C24x23, CY8C24x23A, CY8C22x13, CY8C21x34, CY8C21x23, CY7C64215, CY7C603xx, CY8CNP1xx, and CYWUSB6953 PSoC® Programmable System-on-Chip Technical Reference Manual (TRM) (001-14463)

Design Aids – Reading and Writing PSoC® Flash – AN2015 (001-40459)

Understanding Data Sheet Jitter Specifications for Cypress Timing Products – AN5054 (001-14503)

Document Conventions

Units of Measure

The following table lists the units of measure that are used in this document.

Table 40. Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
dB	decibel	mVpp	millivolts peak-to-peak
°C	degree Celsius	nA	nanoampere
fF	femto-farad	ns	nanosecond
kHz	kilohertz	nV	nanovolt
kΩ	kilohm	Ω	ohm
MHz	megahertz	ppm	parts per million
µA	microampere	%	percent
µs	microsecond	pF	picofarad
µV	microvolt	ps	picosecond
µW	microwatt	pA	pikoampere
mA	milliampere	rt-Hz	root hertz
mm	millimeter	V	volt
ms	millisecond	W	watt
mV	millivolt		

Numeric Conventions

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase ‘h’ (for example, ‘14h’ or ‘3Ah’). Hexadecimal numbers may also be represented by a ‘0x’ prefix, the C coding convention. Binary numbers have an appended lowercase ‘b’ (for example, ‘01010100b’ or ‘01000011b’). Numbers not indicated by an ‘h’, ‘b’, or ‘0x’ are in decimal format.

Glossary

active high	1. A logic signal having its asserted state as the logic 1 state. 2. A logic signal having the logic 1 state as the higher voltage of the two states.
analog blocks	The basic programmable opamp circuits. These are SC (switched capacitor) and CT (continuous time) blocks. These blocks can be interconnected to provide ADCs, DACs, multi-pole filters, gain stages, and much more.
analog-to-digital converter (ADC)	A device that changes an analog signal to a digital signal of corresponding magnitude. Typically, an ADC converts a voltage to a digital number. The digital-to-analog converter (DAC) performs the reverse operation.
Application programming interface (API)	A series of software routines that comprise an interface between a computer application and lower level services and functions (for example, user modules and libraries). APIs serve as building blocks for programmers that create software applications.
asynchronous	A signal whose data is acknowledged or acted upon immediately, irrespective of any clock signal.
bandgap reference	A stable voltage reference design that matches the positive temperature coefficient of VT with the negative temperature coefficient of VBE, to produce a zero temperature coefficient (ideally) reference.
bandwidth	1. The frequency range of a message or information processing system measured in hertz. 2. The width of the spectral region over which an amplifier (or absorber) has substantial gain (or loss); it is sometimes represented more specifically as, for example, full width at half maximum.

Glossary (continued)

duty cycle	The relationship of a clock period high time to its low time, expressed as a percent.
emulator	Duplicates (provides an emulation of) the functions of one system with a different system, so that the second system appears to behave like the first system.
external reset (XRES)	An active high signal that is driven into the PSoC device. It causes all operation of the CPU and blocks to stop and return to a pre-defined state.
flash	An electrically programmable and erasable, non-volatile technology that provides you the programmability and data storage of EPROMs, plus in-system erasability. Non-volatile means that the data is retained when power is off.
flash block	The smallest amount of flash ROM space that may be programmed at one time and the smallest amount of flash space that may be protected.
frequency	The number of cycles or events per unit of time, for a periodic function.
gain	The ratio of output current, voltage, or power to input current, voltage, or power, respectively. Gain is usually expressed in dB.
I^2C	A two-wire serial computer bus by Philips Semiconductors (now NXP Semiconductors). It is used to connect low-speed peripherals in an embedded system. The original system was created in the early 1980s as a battery control interface, but it was later used as a simple internal bus system for building control electronics. I2C uses only two bi-directional pins, clock and data, both running at the V_{DD} supply voltage and pulled high with resistors. The bus operates up to100 kbits/second in standard mode and 400 kbits/second in fast mode.
ICE	The in-circuit emulator that allows you to test the project in a hardware environment, while viewing the debugging device activity in a software environment (PSoC Designer).
input/output (I/O)	A device that introduces data into or extracts data from a system.
interrupt	A suspension of a process, such as the execution of a computer program, caused by an event external to that process, and performed in such a way that the process can be resumed.
interrupt service routine (ISR)	A block of code that normal code execution is diverted to when the CPU receives a hardware interrupt. Many interrupt sources may each exist with its own priority and individual ISR code block. Each ISR code block ends with the RETI instruction, returning the device to the point in the program where it left normal program execution.
jitter	1. A misplacement of the timing of a transition from its ideal position. A typical form of corruption that occurs on serial data streams. 2. The abrupt and unwanted variations of one or more signal characteristics, such as the interval between successive pulses, the amplitude of successive cycles, or the frequency or phase of successive cycles.
low voltage detect (LVD)	A circuit that senses V_{DD} and provides an interrupt to the system when V_{DD} falls below a selected threshold.
M8C	An 8-bit Harvard-architecture microprocessor. The microprocessor coordinates all activity inside a PSoC by interfacing to the flash, SRAM, and register space.
master device	A device that controls the timing for data exchanges between two devices. Or when devices are cascaded in width, the master device is the one that controls the timing for data exchanges between the cascaded devices and an external interface. The controlled device is called the *slave device*.

Document History Page

Document Title: CY8C29466, CY8C29666 Automotive PSoC® Programmable System-on-Chip™ Document Number: 001-12899				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	772096	HMT	See ECN	New silicon, new document (Revision **).
*A	2697720	VIVG/ PYRS	04/24/09	Updated template Content edits
*B	2769233	BTK	09/25/09	Updated Features section. Updated text of PSoC Functional Overview section. Updated Getting Started section. Made corrections and minor text edits to Pinouts section. Changed the name of some sections for added clarity. Improved formatting of the register tables. Added clarifying comments to some electrical specifications. Changed T_{RAMP} specification per MASJ input. Fixed all AC specifications to conform to a ±5% IMO accuracy. Made other miscellaneous minor text edits. Deleted some non-applicable or redundant information. Added a footnote to clarify that 8 of the 12 analog inputs are regular and the other 4 are direct SC block connections. Updated the Development Tool Selection section. Improved the bookmark structure. Edited F_{IMO6}, T_{ERASEB}, T_{WRITE}, T_{RSCLK}, T_{FSCLK}, V_{IHP}, V_{PPORxR}, and 5 V RefLo specifications according to MASJ input. Removed 'TM' from Programmable System-on-Chip in the title.
*C	2822792	BTK/ AESA	12/07/2009	Added T_{PRGH}, T_{PRGC}, I_{OL}, I_{OH}, F_{32KU}, DC_{ILO}, and $T_{POWERUP}$ electrical specifications. Updated the footnotes for the DC Programming Specifications table. Added maximum values and updated typical values for T_{ERASEB} and T_{WRITE} electrical specifications. Replaced T_{RAMP} electrical specification with $SR_{POWERUP}$ electrical specification. Added "Contents" on page 2.
*D	2888007	NJF	03/30/2010	Updated Cypress website links. Added $T_{BAKETEMP}$ and $T_{BAKETIME}$ parameters in Absolute Maximum Ratings Updated Packaging Information. Updated Ordering Code Definitions. Removed Third Party Tools and Build a PSoC Emulator into your Board. Updated Development Kits and Evaluation Tools. Updated links in Sales, Solutions, and Legal Information.
*E	2987146	BTK	07/19/2010	Updated Pinouts section to add 48-pin package. Updated Packaging Information section to add 48-pin package. Updated Development Tool Selection section to add 48-pin package development tool information. Updated Ordering Information section to add new 48-pin package product. Moved Acronyms section to the end of the document. Added part number CY8C29666 to the title.
*F	3111512	BTK/NJF	07/25/2011	Updated I^2C timing diagram to improve clarity. Updated wording, formatting, and notes of the AC Digital Block Specifications table to improve clarity. Added V_{DDP}, V_{DDLV}, and V_{DDHV} electrical specifications to give more information for programming the device. Updated solder reflow temperature specifications to give more clarity. Updated the jitter specifications. Updated PSoC Device Characteristics table. Updated the F_{32KU} electrical specification. Updated note for R_{PD} electrical specification. Updated note for the T_{STG} electrical specification to add more clarity. Added Tape and Reel Information section. Added C_L electrical specification. Updated Analog Reference specifications. Updated V_{OSOA}, TCV_{OSOA}, V_{OSOB}, and TCV_{OSOB} electrical specifications.
*G	3543452	KAUL	03/06/2012	Updated Tape and Reel Information under Packaging Information.