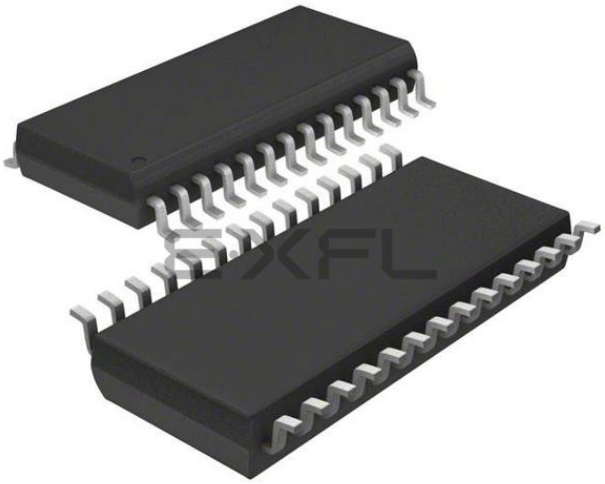

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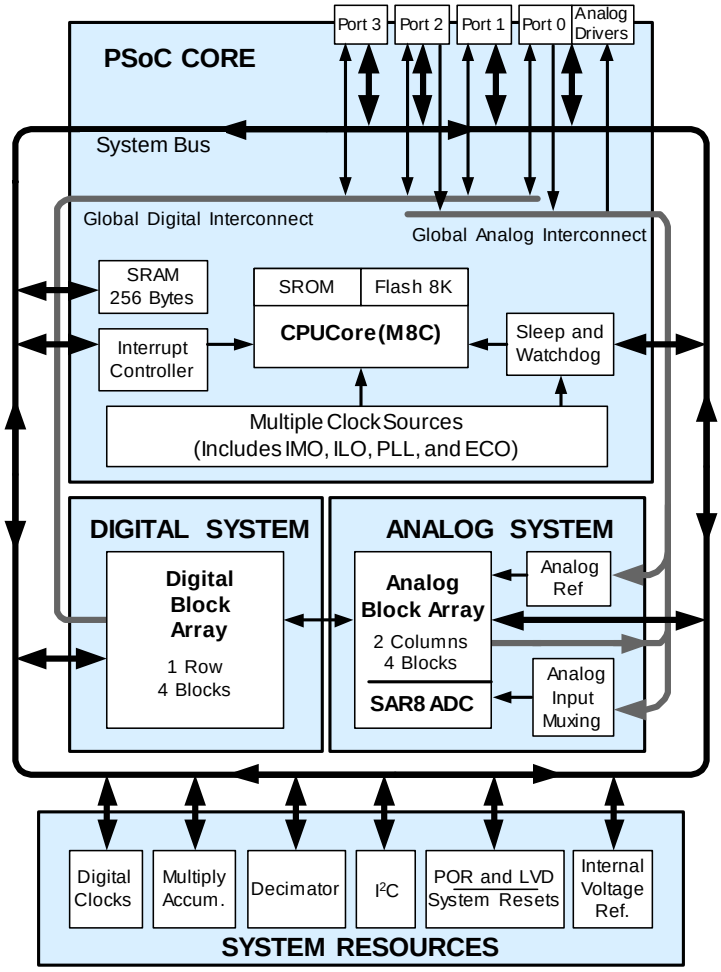
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	25
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.25V
Data Converters	A/D 2x14b; D/A 2x9b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c24633-24pvxi

Block Diagram



Additional System Resources

System resources, some of which have been previously listed, provide additional capability useful to complete systems. Additional resources include a multiplier, decimator, low voltage detection, and power on reset. Brief statements describing the merits of each system resource are presented below.

- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks can be routed to both the digital and analog systems. Additional clocks can be generated using digital PSoC blocks as clock dividers.
- A multiply accumulate (MAC) provides a fast 8-bit multiplier with 32-bit accumulate, to assist in both general math as well as digital filters.
- The decimator provides a custom hardware filter for digital signal processing applications including the creation of Delta Sigma ADCs.
- The I^2C module provides 100 and 400 kHz communication over two wires. Slave, master, and multi-master modes are all supported.
- Low-voltage detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced power-on reset (POR) circuit eliminates the need for a system supervisor.
- An internal 1.3 V reference provides an absolute reference for the analog system, including ADCs and DACs.

PSoC Device Characteristics

Depending on your PSoC device characteristics, the digital and analog systems can have 16, 8, or 4 digital blocks and 12, 6, or 3 analog blocks. The following table lists the resources available for specific PSoC device groups.

Table 1. PSoC Device Characteristics

PSoC Part Number	Digital I/O	Digital Rows	Digital Blocks	Analog Inputs	Analog Outputs	Analog Columns	Analog Blocks	SRAM Size	Flash Size	SAR ADC
CY8C29x66	up to 64	4	16	up to 12	4	4	12	2 K	32 K	No
CY8C28xxx	up to 44	up to 3	up to 12	up to 44	up to 4	up to 6	up to 12 + 4[1]	1 K	16 K	Yes
CY8C27x43	up to 44	2	8	up to 12	4	4	12	256	16 K	No
CY8C24x94	up to 56	1	4	up to 48	2	2	6	1 K	16 K	No
CY8C24x23A	up to 24	1	4	up to 12	2	2	6	256	4 K	No
CY8C23x33	up to 26	1	4	up to 12	2	2	4	256	8 K	Yes
CY8C22x45	up to 38	2	8	up to 38	0	4	6[1]	1 K	16 K	No
CY8C21x45	up to 24	1	4	up to 24	0	4	6[1]	512	8 K	Yes
CY8C21x34	up to 28	1	4	up to 28	0	2	4[1]	512	8 K	No
CY8C21x23	up to 16	1	4	up to 8	0	2	4[1]	256	4 K	No
CY8C20x34	up to 28	0	0	up to 28	0	0	3[1,2]	512	8 K	No
CY8C20xx6	up to 36	0	0	up to 36	0	0	3[1,2]	up to 2 K	up to 32 K	No

Notes
1. Limited analog functionality.
2. Two analog blocks and one CapSense®.

Development Tools

PSoC Designer™ is the revolutionary integrated design environment (IDE) that you can use to customize PSoC to meet your specific application requirements. PSoC Designer software accelerates system design and time to market. Develop your applications using a library of precharacterized analog and digital peripherals (called user modules) in a drag-and-drop design environment. Then, customize your design by leveraging the dynamically generated application programming interface (API) libraries of code. Finally, debug and test your designs with the integrated debug environment, including in-circuit emulation and standard software debug features. PSoC Designer includes:

- Application editor graphical user interface (GUI) for device and user module configuration and dynamic reconfiguration
- Extensive user module catalog
- Integrated source-code editor (C and assembly)
- Free C compiler with no size restrictions or time limits
- Built-in debugger
- In-circuit emulation
- Built-in support for communication interfaces:
  - Hardware and software I^2C slaves and masters
  - Full-speed USB 2.0
  - Up to four full-duplex universal asynchronous receiver/transmitters (UARTs), SPI master and slave, and wireless

PSoC Designer supports the entire library of PSoC 1 devices and runs on Windows XP, Windows Vista, and Windows 7.

PSoC Designer Software Subsystems

Design Entry

In the chip-level view, choose a base device to work with. Then select different onboard analog and digital components that use the PSoC blocks, which are called user modules. Examples of user modules are analog-to-digital converters (ADCs), digital-to-analog converters (DACs), amplifiers, and filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration makes it possible to change configurations at run time. In essence, this lets you to use more than 100 percent of PSoC's resources for an application.

Code Generation Tools

The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. You can develop your design in C, assembly, or a combination of the two.

Assemblers. The assemblers allow you to merge assembly code seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices. The optimizing C compilers provide all of the features of C, tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

PSoC Designer has a debug environment that provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow you to read and program and read and write data memory, and read and write I/O registers. You can read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also lets you to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer.

In-Circuit Emulator

A low-cost, high-functionality in-circuit emulator (ICE) is available for development support. This hardware can program single devices.

The emulator consists of a base unit that connects to the PC using a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full-speed (24 MHz) operation.

Table 4. Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW		40			80			C0	
PRT0IE	01	RW		41			81			C1	
PRT0GS	02	RW		42			82			C2	
PRT0DM2	03	RW		43			83			C3	
PRT1DR	04	RW		44		ASD11CR0	84	RW		C4	
PRT1IE	05	RW		45		ASD11CR1	85	RW		C5	
PRT1GS	06	RW		46		ASD11CR2	86	RW		C6	
PRT1DM2	07	RW		47		ASD11CR3	87	RW		C7	
PRT2DR	08	RW		48			88			C8	
PRT2IE	09	RW		49			89			C9	
PRT2GS	0A	RW		4A			8A			CA	
PRT2DM2	0B	RW		4B			8B			CB	
PRT3DR	0C	RW		4C			8C			CC	
PRT3IE	0D	RW		4D			8D			CD	
PRT3GS	0E	RW		4E			8E			CE	
PRT3DM2	0F	RW		4F			8F			CF	
	10			50			90			D0	
	11			51			91			D1	
	12			52			92			D2	
	13			53			93			D3	
	14			54		ASC21CR0	94	RW		D4	
	15			55		ASC21CR1	95	RW		D5	
	16			56		ASC21CR2	96	RW	I^2C_CFG	D6	RW
	17			57		ASC21CR3	97	RW	I^2C_SCR	D7	#
	18			58			98		I^2C_DR	D8	RW
	19			59			99		I^2C_MSCR	D9	#
	1A			5A			9A		INT_CLR0	DA	RW
	1B			5B			9B		INT_CLR1	DB	RW
	1C			5C			9C			DC	
	1D			5D			9D		INT_CLR3	DD	RW
	1E			5E			9E		INT_MSK3	DE	RW
	1F			5F			9F			DF	
DBB00DR0	20	#	AMX_IN	60	RW		A0		INT_MSK0	E0	RW
DBB00DR1	21	W		61			A1		INT_MSK1	E1	RW
DBB00DR2	22	RW		62			A2		INT_VC	E2	RC
DBB00CR0	23	#	ARF_CR	63	RW		A3		RES_WDT	E3	W
DBB01DR0	24	#	CMP_CR0	64	#		A4		DEC_DH	E4	RC
DBB01DR1	25	W	ASY_CR	65	#		A5		DEC_DL	E5	RC
DBB01DR2	26	RW	CMP_CR1	66	RW		A6		DEC_CR0	E6	RW
DBB01CR0	27	#	SARADC_DL	67	RW		A7		DEC_CR1	E7	RW
DCB02DR0	28	#		68			A8		MUL0_X	E8	W
DCB02DR1	29	W	SARADC_C0	69	#		A9		MUL0_Y	E9	W
DCB02DR2	2A	RW	SARADC_C1	6A	RW		AA		MUL0_DH	EA	R
DCB02CR0	2B	#		6B			AB		MUL0_DL	EB	R
DCB03DR0	2C	#	TMP_DR0	6C	RW		AC		ACC0_DR1	EC	RW
DCB03DR1	2D	W	TMP_DR1	6D	RW		AD		ACC0_DR0	ED	RW
DCB03DR2	2E	RW	TMP_DR2	6E	RW		AE		ACC0_DR3	EE	RW
DCB03CR0	2F	#	TMP_DR3	6F	RW		AF		ACC0_DR2	EF	RW
	30		ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
	31		ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
	32		ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
	34		ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
	35		ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
	36		ACB01CR1 *	76	RW	RDI0RO1	B6	RW		F6	
	37		ACB01CR2 *	77	RW		B7		CPU_F	F7	RL
	38			78			B8			F8	
	39			79			B9			F9	
	3A			7A			BA			FA	
	3B			7B			BB			FB	
	3C			7C			BC			FC	
	3D			7D			BD			FD	
	3E			7E			BE		CPU_SCR1	FE	#
	3F			7F			BF		CPU_SCR0	FF	#

Blank fields are reserved. # Access is bit specific.

Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8C24633 PSoC device. For the most up to date electrical specifications, confirm that you have the most recent data sheet by going to the web at http://www.cypress.com/psoc.

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted.

Refer to Table 22 for the electrical specifications on the IMO using SLIMO mode.

Figure 6. Voltage versus CPU Frequency

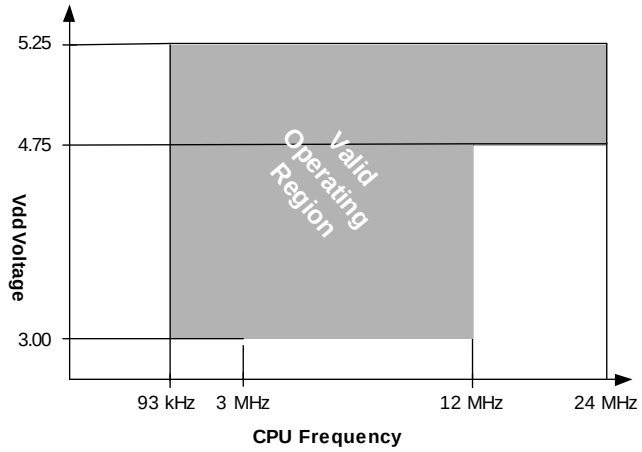
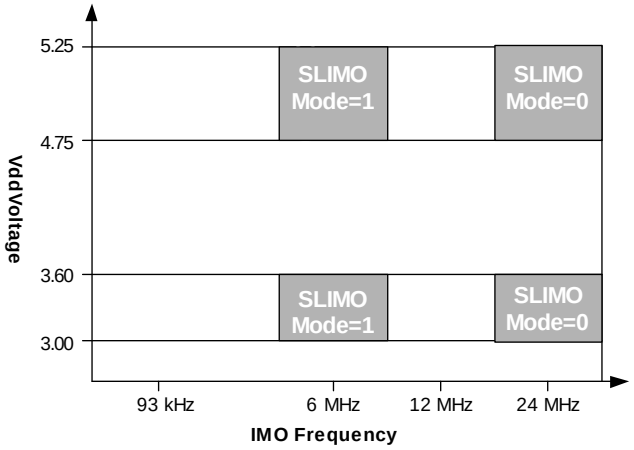


Figure 5a. IMO Frequency Trim Options



Absolute Maximum Ratings

Table 6. Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units	Notes
T_{STG}	Storage temperature	–55	25	+100	^{o}C	Higher storage temperatures reduce data retention time. Recommended storage temperature is +25 ^{o}C ± 25 ^{o}C. Extended duration storage temperatures above 65 ^{o}C degrade reliability.
$T_{BAKETEMP}$	Bake temperature	–	125	See package label	^{o}C	
$T_{BAKETIME}$	Bake time	See package label	–	72	hours	
T_A	Ambient temperature with power applied	-40	–	+85	^{o}C	
Vdd	Supply voltage on V_{dd} Relative to V_{ss}	-0.5	–	+6.0	V	
V_{IO}	DC input voltage	V_{ss} - 0.5	–	V_{dd} + 0.5	V	
V_{IOZ}	DC voltage applied to Tri-state	V_{ss} - 0.5	–	V_{dd} + 0.5	V	
I_{MIO}	Maximum current into any port pin	-25	–	+50	mA	
ESD	Electro static discharge voltage	2000	–	–	V	Human Body Model ESD.
LU	Latch up current	–	–	200	mA	

Operating Temperature

Table 7. Operating Temperature

Symbol	Description	Min	Typ	Max	Units	Notes
T_A	Ambient temperature	–40	–	+85	^{o}C	
T_J	Junction temperature	–40	–	+100	^{o}C	The temperature rise from ambient to junction is package specific. See Thermal Impedances by Package on page 41. The user must limit the power consumption to comply with this requirement.

Table 11. 3.3 V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input offset voltage (absolute value) Power = low, opamp bias = high Power = medium, opamp bias = high Power = high, opamp bias = high	 – – –	 1.65 1.32 –	 10 8 –	 mV mV mV	Power = high, opamp bias = high setting is not allowed for 3.3 V V_{DD} operation.
TCV_{OSOA}	Average input offset voltage drift	–	7.0	35.0	µV/°C	
I_{EBOA}	Input leakage current (port 0 analog pins)	–	20	–	pA	Gross tested to 1 µA
C_{INOA}	Input capacitance (port 0 analog pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25 °C
V_{CMOA}	Common mode voltage range	0.2	–	V_{DD} – 0.2	V	The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.
G_{OLOA}	Open loop gain power = low, ppamp, Opamp bias = low Power = medium, opamp bias = low Power = high, opamp bias = low	 60 60 80	 – – –	 – – –	 dB dB dB	Specification is applicable at low Opamp bias. For high opamp bias mode (except high power, high opamp bias), minimum is 60 dB.
$V_{OHIGHOA}$	High output voltage swing (internal signals) Power = low, opamp bias = low Power = medium, opamp bias = low Power = high, opamp bias = low	 V_{DD} – 0.2 V_{DD} – 0.2 V_{DD} – 0.2	 – – –	 – – –	 V V V	Power = high, opamp bias = high setting is not allowed for 3.3 V V_{DD} operation.
V_{OLOWOA}	Low output voltage swing (internal signals) Power = low, opamp bias = low Power = medium, opamp bias = low Power = high, opamp bias = low	 – – –	 – – –	 0.2 0.2 0.2	 V V V	Power = high, opamp bias = high setting is not allowed for 3.3 V V_{DD} operation.
I_{SOA}	Supply current (including associated AGND buffer) Power = low, opamp bias = low Power = low, opamp bias = high Power = medium, opamp bias = low Power = medium, opamp bias = high Power = high, opamp bias = low Power = high, opamp bias = high	 – – – – – –	 150 300 600 1200 2400 –	 200 400 800 1600 3200 –	 µA µA µA µA µA µA	Power = high, opamp bias = high setting is not allowed for 3.3 V V_{DD} operation.
$PSRR_{OA}$	Supply voltage rejection ratio	64	80	–	dB	$V_{SS} \le V_{IN} \le (V_{DD} – 2.25)$ or $(V_{DD} – 1.25\ V) \le V_{IN} \le V_{DD}$

DC Low Power Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 12. DC Low Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{REFLPC}	Low power comparator (LPC) reference voltage range	0.2	–	V_{dd} - 1	V	
I_{SLPC}	LPC supply current	–	10	40	µA	
V_{OSLPC}	LPC voltage offset	–	2.5	30	mV	

DC Analog Reference Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

The guaranteed specifications are measured through the analog continuous time PSoC blocks. The power levels for AGND refer to the power of the analog continuous Time PSoC block. The power levels for RefHi and RefLo refer to the analog reference control register. The limits stated for AGND include the offset error of the AGND buffer local to the analog continuous time PSoC block. reference control power is high.

Table 15. 5-V DC Analog Reference Specifications

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b000	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.136	$V_{DD}/2$ + 1.288	$V_{DD}/2$ + 1.409	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.138	$V_{DD}/2$ + 0.003	$V_{DD}/2$ + 0.132	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.417	$V_{DD}/2$ – 1.289	$V_{DD}/2$ – 1.154	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.202	$V_{DD}/2$ + 1.290	$V_{DD}/2$ + 1.358	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.055	$V_{DD}/2$ + 0.001	$V_{DD}/2$ + 0.055	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.369	$V_{DD}/2$ – 1.295	$V_{DD}/2$ – 1.218	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.211	$V_{DD}/2$ + 1.292	$V_{DD}/2$ + 1.357	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.055	$V_{DD}/2$	$V_{DD}/2$ + 0.052	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.368	$V_{DD}/2$ – 1.298	$V_{DD}/2$ – 1.224	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.215	$V_{DD}/2$ + 1.292	$V_{DD}/2$ + 1.353	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.040	$V_{DD}/2$ – 0.001	$V_{DD}/2$ + 0.033	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.368	$V_{DD}/2$ – 1.299	$V_{DD}/2$ – 1.225	V
0b001	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.076	P2[4] + P2[6] – 0.021	P2[4] + P2[6] + 0.041	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.025	P2[4] – P2[6] + 0.011	P2[4] – P2[6] + 0.085	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.069	P2[4] + P2[6] – 0.014	P2[4] + P2[6] + 0.043	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.029	P2[4] – P2[6] + 0.005	P2[4] – P2[6] + 0.052	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.072	P2[4] + P2[6] – 0.011	P2[4] + P2[6] + 0.048	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.031	P2[4] – P2[6] + 0.002	P2[4] – P2[6] + 0.057	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.070	P2[4] + P2[6] – 0.009	P2[4] + P2[6] + 0.047	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.033	P2[4] – P2[6] + 0.001	P2[4] – P2[6] + 0.039	V

Table 15. 5-V DC Analog Reference Specifications (continued)

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b101	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	P2[4] + Bandgap ($P2[4] = V_{DD}/2$)	P2[4] + 1.228	P2[4] + 1.284	P2[4] + 1.332	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap ($P2[4] = V_{DD}/2$)	P2[4] – 1.358	P2[4] – 1.293	P2[4] – 1.226	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	P2[4] + Bandgap ($P2[4] = V_{DD}/2$)	P2[4] + 1.236	P2[4] + 1.289	P2[4] + 1.332	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap ($P2[4] = V_{DD}/2$)	P2[4] – 1.357	P2[4] – 1.297	P2[4] – 1.229	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	P2[4] + Bandgap ($P2[4] = V_{DD}/2$)	P2[4] + 1.237	P2[4] + 1.291	P2[4] + 1.337	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap ($P2[4] = V_{DD}/2$)	P2[4] – 1.356	P2[4] – 1.299	P2[4] – 1.232	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	P2[4] + Bandgap ($P2[4] = V_{DD}/2$)	P2[4] + 1.237	P2[4] + 1.292	P2[4] + 1.337	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap ($P2[4] = V_{DD}/2$)	P2[4] – 1.357	P2[4] – 1.300	P2[4] – 1.233	V
0b110	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	2 × Bandgap	2.512	2.594	2.654	V
		V_{AGND}	AGND	Bandgap	1.250	1.303	1.346	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.011	V_{SS} + 0.027	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	2 × Bandgap	2.515	2.592	2.654	V
		V_{AGND}	AGND	Bandgap	1.253	1.301	1.340	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.006	V_{SS} + 0.02	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	2 × Bandgap	2.518	2.593	2.651	V
		V_{AGND}	AGND	Bandgap	1.254	1.301	1.338	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.004	V_{SS} + 0.017	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	2 × Bandgap	2.517	2.594	2.650	V
		V_{AGND}	AGND	Bandgap	1.255	1.300	1.337	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.003	V_{SS} + 0.015	V
0b111	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	3.2 × Bandgap	4.011	4.143	4.203	V
		V_{AGND}	AGND	1.6 × Bandgap	2.020	2.075	2.118	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.011	V_{SS} + 0.026	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	3.2 × Bandgap	4.022	4.138	4.203	V
		V_{AGND}	AGND	1.6 × Bandgap	2.023	2.075	2.114	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.006	V_{SS} + 0.017	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	3.2 × Bandgap	4.026	4.141	4.207	V
		V_{AGND}	AGND	1.6 × Bandgap	2.024	2.075	2.114	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.004	V_{SS} + 0.015	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	3.2 × Bandgap	4.030	4.143	4.206	V
		V_{AGND}	AGND	1.6 × Bandgap	2.024	2.076	2.112	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.003	V_{SS} + 0.013	V

Table 16. 3.3-V DC Analog Reference Specifications (continued)

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b100	All power settings Not allowed at 3.3 V	–	–	–	–	–	–	–
0b101	RefPower = high opamp bias = high	V_{REFHI}	Ref High	P2[4] + Bandgap ($P2[4] = V_{DD}/2$)	P2[4] + 1.211	P2[4] + 1.285	P2[4] + 1.348	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap ($P2[4] = V_{DD}/2$)	P2[4] – 1.354	P2[4] – 1.290	P2[4] – 1.197	V
	RefPower = high opamp bias = low	V_{REFHI}	Ref High	P2[4] + Bandgap ($P2[4] = V_{DD}/2$)	P2[4] + 1.209	P2[4] + 1.289	P2[4] + 1.353	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap ($P2[4] = V_{DD}/2$)	P2[4] – 1.352	P2[4] – 1.294	P2[4] – 1.222	V
	RefPower = medium opamp bias = high	V_{REFHI}	Ref High	P2[4] + Bandgap ($P2[4] = V_{DD}/2$)	P2[4] + 1.218	P2[4] + 1.291	P2[4] + 1.351	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap ($P2[4] = V_{DD}/2$)	P2[4] – 1.351	P2[4] – 1.296	P2[4] – 1.224	V
	RefPower = medium opamp bias = low	V_{REFHI}	Ref High	P2[4] + Bandgap ($P2[4] = V_{DD}/2$)	P2[4] + 1.215	P2[4] + 1.292	P2[4] + 1.354	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap ($P2[4] = V_{DD}/2$)	P2[4] – 1.352	P2[4] – 1.297	P2[4] – 1.227	V
0b110	RefPower = high opamp bias = high	V_{REFHI}	Ref High	2 × Bandgap	2.460	2.594	2.695	V
		V_{AGND}	AGND	Bandgap	1.257	1.302	1.335	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.01	V_{SS} + 0.029	V
	RefPower = high opamp bias = low	V_{REFHI}	Ref High	2 × Bandgap	2.462	2.592	2.692	V
		V_{AGND}	AGND	Bandgap	1.256	1.301	1.332	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.005	V_{SS} + 0.017	V
	RefPower = medium opamp bias = high	V_{REFHI}	Ref High	2 × Bandgap	2.473	2.593	2.682	V
		V_{AGND}	AGND	Bandgap	1.257	1.301	1.330	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.003	V_{SS} + 0.014	V
	RefPower = medium opamp bias = low	V_{REFHI}	Ref High	2 × Bandgap	2.470	2.594	2.685	V
		V_{AGND}	AGND	Bandgap	1.256	1.300	1.332	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.002	V_{SS} + 0.012	V
0b111	All power settings Not allowed at 3.3 V	–	–	–	–	–	–	–

DC I²C Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 20. DC I²C Specifications[11]

Symbol	Description	Min	Typ	Max	Units	Notes
V_{ILI2C}	Input low level	–	–	0.3 × V_{DD}	V	3.0 V ≤ V_{DD} ≤ 3.6 V
		–	–	0.25 × V_{DD}	V	4.75 V ≤ V_{DD} ≤ 5.25 V
V_{IHI2C}	Input high level	0.7 × V_{DD}	–	–	V	3.0 V ≤ V_{DD} ≤ 5.25 V

SAR8 ADC DC Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 21. SAR8 ADC DC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
$V_{ADCVREF}$	Reference voltage at pin P3[0] when configured as ADC reference voltage	3.0	–	5.25	V	The voltage level at P3[0] (when configured as ADC reference voltage) should always be maintained to be less than chip supply voltage level on V_{dd} pin. $V_{ADCVREF}$ < V_{dd}.
$I_{ADCVREF}$	Current when P3[0] is configured as ADC V_{REF}	3	–	–	mA	
INL	R-2R integral non-linearity[12]	-1.2	–	+1.2	LSB	The maximum LSB is over a sub-range not exceeding 1/16 of the full-scale range.
DNL	R-2R differential non-linearity[13]	-1	–	+1	LSB	Output is monatonic.

Notes
11. All GPIOs meet the DC GPIO V_{IL} and V_{IH} specifications found in the DC GPIO Specifications sections. The I²C GPIO pins also meet the above specs.
12. At the 7F and 80 points, the maximum INL is 1.5 LSB.
13. For the 7F to 80 transition, the DNL specification is waived.

AC Electrical Characteristics

AC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 22. 5V and 3.3V AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{IMO24}	Internal main oscillator frequency for 24 MHz	22.8	24	25.2[14,15,16]	MHz	Trimmed for 5 V or 3.3 V operation using factory trim values. See Figure 5b on page 15. SLIMO mode = 0.
F_{IMO6}	Internal main oscillator frequency for 6 MHz	5.5	6	6.5[14,15,16]	MHz	Trimmed for 5 V or 3.3 V operation using factory trim values. See Figure 5b on page 15. SLIMO mode = 1.
F_{CPU1}	CPU frequency (5 V nominal)	0.093	24	24.6[14,15]	MHz	SLIMO mode = 0.
F_{CPU2}	CPU frequency (3.3 V nominal)	0.093	12	12.3[15,16]	MHz	SLIMO mode = 0.
F_{48M}	digital psoc block frequency	0	48	49.2[14,15,17]	MHz	Refer to the Table 27 on page 36.
F_{24M}	Digital PSoC block frequency	0	24	24.6[15,17]	MHz	
F_{32K1}	Internal low speed oscillator frequency	15	32	75	kHz	
F_{32K2}	External crystal oscillator	–	32.768	–	kHz	Accuracy is capacitor and crystal dependent. 50% duty cycle.
F_{32K_U}	Internal low speed oscillator untrimmed frequency	5	–	100	kHz	
F_{PLL}	PLL frequency	–	23.986	–	MHz	Is a multiple (x732) of crystal frequency.
DC_{ILO}	Internal low speed oscillator duty cycle	20	50	80	%	
$T_{PLLSLEW}$	PLL Lock time	0.5	–	10	ms	
$T_{PLLSLEWSLOW}$	PLL Lock time for low gain setting	0.5	–	50	ms	
T_{OS}	External crystal oscillator startup to 1%	–	1700	2620	ms	
T_{OSACC}	External crystal oscillator startup to 100 ppm	–	2800	3800	ms	The crystal oscillator frequency is within 100 ppm of its final value by the end of the T_{osacc} period. Correct operation assumes a properly loaded 1 uW maximum drive level 32.768 kHz crystal. 3.0 V ≤ V_{dd} ≤ 5.5 V, –40 °C ≤ T_A ≤ 85 °C.
T_{XRST}	External reset pulse width	10	–	–	µs	
DC24M	24 MHz duty cycle	40	50	60	%	
Step24M	24 MHz trim step size	–	50	–	kHz	
Fout48M	48 MHz output frequency	46.8	48.0	49.2[14,16]	MHz	Trimmed. Utilizing factory trim values.
F_{MAX}	Maximum frequency of signal on row input or row output.	–	–	12.3	MHz	
T_{RAMP}	Supply ramp time	NA	–	–	µs	
SR_{POWER_UP}	Power supply slew rate	–	–	250	V/ms	
$T_{POWERUP}$	Time from End of POR to CPU Executing Code	–	16	100	ms	
t_{jit_IMO} [18]	24 MHz IMO cycle-to-cycle jitter (RMS)	–	200	700	ps	
	24 MHz IMO long term N cycle-to-cycle jitter (RMS)	–	300	900	ps	N = 32
	24 MHz IMO period jitter (RMS)	–	100	400	ps	
t_{jit_PLL} [18]	24 MHz IMO cycle-to-cycle jitter (RMS)	–	200	800	ps	
	24 MHz IMO long term N cycle-to-cycle jitter (RMS)	–	300	1200	ps	N = 32
	24 MHz IMO period jitter (RMS)	–	100	700	ps	

Notes
14. 4.75V < Vdd < 5.25V.
15. Accuracy derived from Internal Main Oscillator with appropriate trim for Vdd range.
16. 3.0V < Vdd < 3.6V.
17. See the individual user module data sheets for information on maximum frequencies for user modules.
18. Refer to Cypress Jitter Specifications application note, Understanding Datasheet Jitter Specifications for Cypress Timing Products – AN5054 for more information.

Figure 7. PLL Lock Timing Diagram

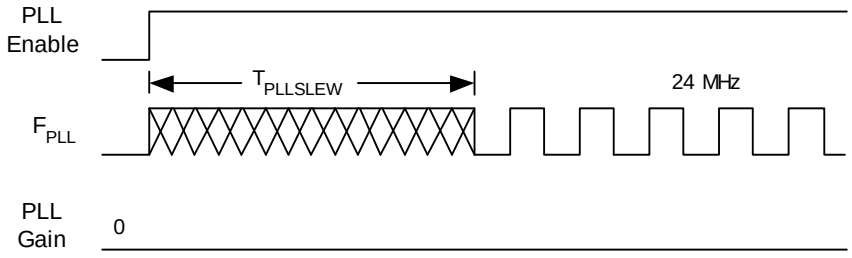


Figure 8. PLL Lock for Low Gain Setting Timing Diagram

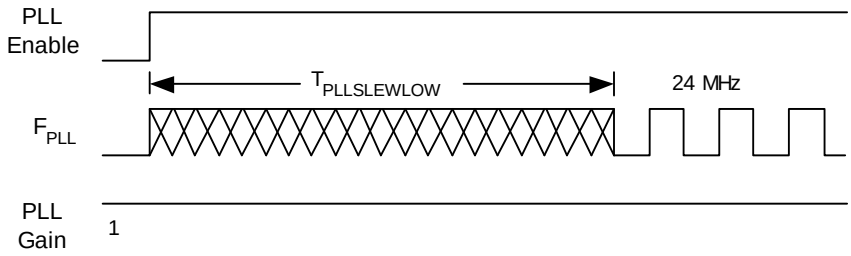


Figure 9. External Crystal Oscillator Startup Timing Diagram

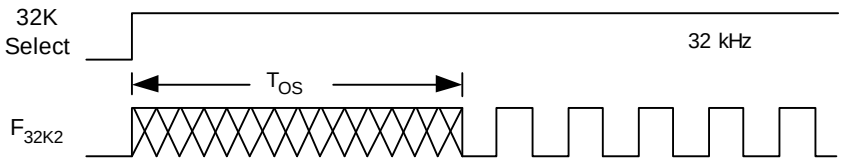
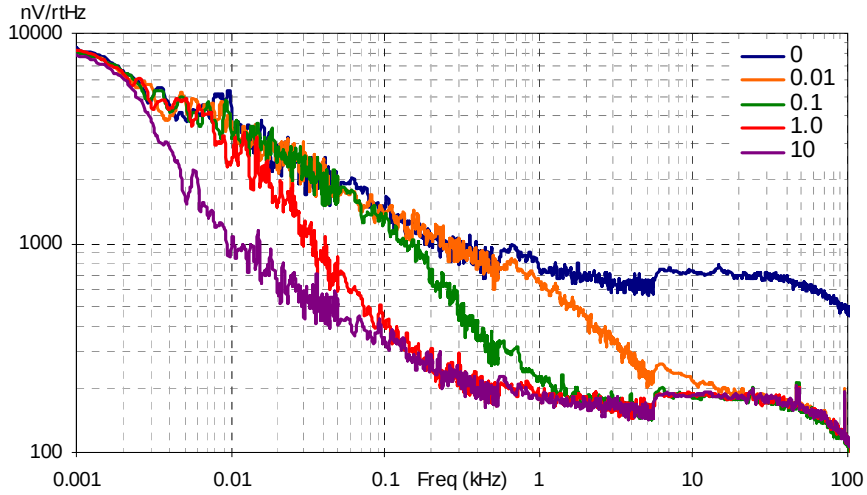


Table 25. 3.3 V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input offset voltage (absolute value) Power = low, opamp bias = high Power = medium, opamp bias = high Power = high, opamp bias = high	 – – –	 1.65 1.32 –	 10 8 –	 mV mV mV	Power = high, opamp bias = high setting is not allowed for 3.3 V V_{DD} operation.
TCV_{OSOA}	Average input offset voltage drift	–	7.0	35.0	µV/°C	
I_{EBOA}	Input leakage current (port 0 analog pins)	–	20	–	pA	Gross tested to 1 µA
C_{INOA}	Input capacitance (port 0 analog pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25 °C
V_{CMOA}	Common mode voltage range	0.2	–	V_{DD} – 0.2	V	The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.
G_{OLOA}	Open loop gain Power = low, opamp bias = low Power = medium, opamp bias = low Power = high, opamp bias = low	 60 60 80	 – – –	 – – –	 dB dB dB	Specification is applicable at low opamp bias. For high opamp bias mode (except high power, high Opamp bias), minimum is 60 dB.
$V_{OHIGHOA}$	High output voltage swing (internal signals) Power = low, opamp bias = low Power = medium, opamp bias = low Power = high, opamp bias = low	 V_{DD} – 0.2 V_{DD} – 0.2 V_{DD} – 0.2	 – – –	 – – –	 V V V	Power = high, opamp bias = high setting is not allowed for 3.3 V V_{DD} operation.
V_{OLOWOA}	Low output voltage swing (internal signals) Power = low, ppamp opamp bias = low Power = medium, opamp bias = low Power = high, opamp bias = low	 – – –	 – – –	 0.2 0.2 0.2	 V V V	Power = high, opamp bias = high setting is not allowed for 3.3 V V_{DD} operation.
I_{SOA}	Supply current (including associated AGND buffer) Power = low, opamp bias = low Power = low, opamp bias = high Power = medium, opamp bias = low Power = medium, opamp bias = high Power = high, opamp bias = low Power = high, opamp bias = high	 – – – – – –	 150 300 600 1200 2400 –	 200 400 800 1600 3200 –	 µA µA µA µA µA µA	Power = high, opamp bias = high setting is not allowed for 3.3 V V_{DD} operation.
$PSRR_{OA}$	Supply voltage rejection ratio	64	80	–	dB	$V_{SS} \le V_{IN} \le (V_{DD} – 2.25)$ or $(V_{DD} – 1.25\ V) \le V_{IN} \le V_{DD}$

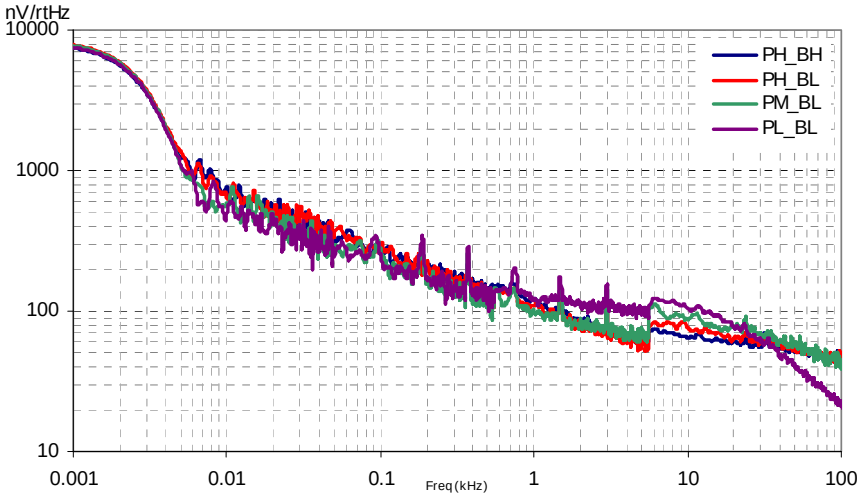
When bypassed by a capacitor on P2[4], the noise of the analog ground signal distributed to each block is reduced by a factor of up to 5 (14 dB). This is at frequencies above the corner frequency defined by the on-chip 8.1k resistance and the external capacitor.

Figure 11. Typical AGND Noise with P2[4] Bypass



At low frequencies, the opamp noise is proportional to 1/f, power independent, and determined by device geometry. At high frequencies, increased power level reduces the noise spectrum level.

Figure 12. Typical Opamp Noise



AC Low Power Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 26. AC Low Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{RLPC}	LPC response time	–	–	50	µs	≥ 50 mV overdrive comparator reference set within V_{REFLPC}.

AC Analog Output Buffer Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 28. 5 V AC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{ROB}	Rising settling time to 0.1%, 1 V step, 100 pF load Power = low Power = high	 – –	 – –	 2.5 2.5	 µs µs	
T_{SOB}	Falling settling time to 0.1%, 1 V step, 100 pf load Power = low Power = high	 – –	 – –	 2.2 2.2	 µs µs	
SR_{ROB}	Rising slew rate (20% to 80%), 1V step, 100 pf load Power = low power = High	 0.65 0.65	 – –	 – –	 V/µs V/µs	
SR_{FOB}	Falling slew rate (80% to 20%), 1V step, 100 pf load Power = low Power = high	 0.65 0.65	 – –	 – –	 V/µs V/µs	
BW_{OB}	Small signal bandwidth, 20 mv_{pp}, 3db bw, 100 pf load Power = low Power = high	 0.8 0.8	 – –	 – –	 MHz MHz	
BW_{OB}	Large signal bandwidth, 1V_{pp}, 3db bw, 100 pf load Power = low Power = high	 300 300	 – –	 – –	 kHz kHz	

Table 29. 3.3 V AC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{ROB}	Rising settling time to 0.1%, 1 V step, 100 pF load Power = low Power = high	 – –	 – –	 3.8 3.8	 µs µs	
T_{SOB}	Falling settling time to 0.1%, 1V Step, 100 pF load Power = low power = High	 – –	 – –	 2.6 2.6	 µs µs	
SR_{ROB}	Rising slew rate (20% to 80%), 1V step, 100 pF load Power = Low Power = High	 0.5 0.5	 – –	 – –	 V/µs V/µs	
SR_{FOB}	falling slew rate (80% to 20%), 1V step, 100 pF load Power = low Power = high	 0.5 0.5	 – –	 – –	 V/µs V/µs	
BW_{OB}	Small signal bandwidth, 20 mV_{pp}, 3dB BW, 100 pF load Power = low Power = high	 0.7 0.7	 – –	 – –	 MHz MHz	
BW_{OB}	Large signal bandwidth, 1V_{pp}, 3dB BW, 100 pF load Power = low Power = high	 200 200	 – –	 – –	 kHz kHz	

AC I²C Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

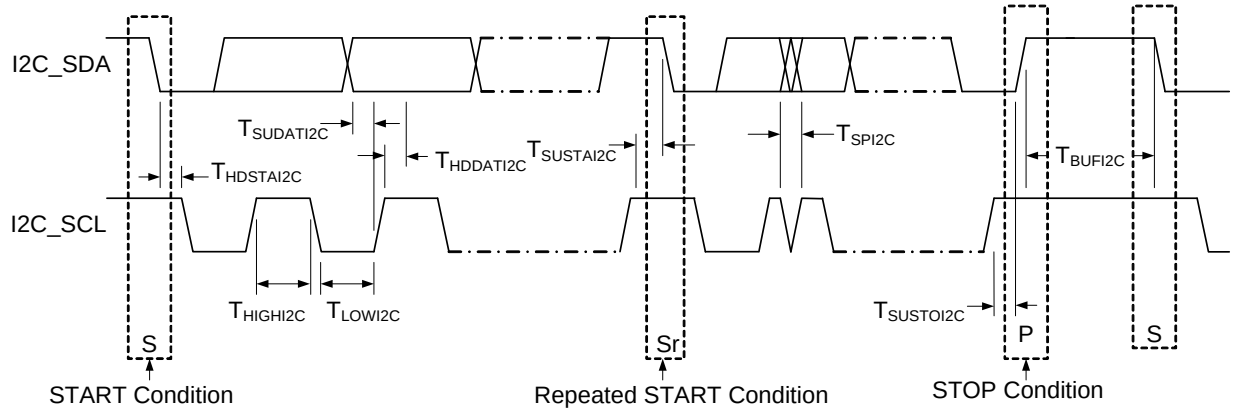
Table 34. AC Characteristics of the I²C SDA and SCL Pins for V_{dd} > 3.0 V

Symbol	Description	Standard-Mode		Fast-Mode		Units	Notes
		Min	Max	Min	Max		
F_{SCLI2C}	SCL clock frequency	0	100	0	400	kHz	
$T_{HDSTAI2C}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	4.0	–	0.6	–	µs	
T_{LOWI2C}	LOW period of the SCL Clock	4.7	–	1.3	–	µs	
$T_{HIGHI2C}$	HIGH period of the SCL Clock	4.0	–	0.6	–	µs	
$T_{SUSTAI2C}$	Set-up time for a repeated START Condition	4.7	–	0.6	–	µs	
$T_{HDDATI2C}$	Data hold time	0	–	0	–	µs	
$T_{SUDATI2C}$	Data set-up time	250	–	100[22]	–	ns	
$T_{SUSTOI2C}$	Set-up time for STOP Condition	4.0	–	0.6	–	µs	
T_{BUFI2C}	Bus free time between a stop and start condition	4.7	–	1.3	–	µs	
T_{SPI2C}	Pulse width of spikes are suppressed by the input filter.	–	–	0	50	ns	

Table 35. AC Characteristics of the I²C SDA and SCL Pins for V_{dd} < 3.0 V (Fast-Mode Not Supported)

Symbol	Description	Standard-Mode		Fast-Mode		Units	Notes
		Min	Max	Min	Max		
F_{SCLI2C}	SCL clock frequency	0	100	–	–	kHz	
$T_{HDSTAI2C}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	4.0	–	–	–	µs	
T_{LOWI2C}	LOW period of the SCL Clock	4.7	–	–	–	µs	
$T_{HIGHI2C}$	HIGH period of the SCL Clock	4.0	–	–	–	µs	
$T_{SUSTAI2C}$	Set-up Time for a Repeated START Condition	4.7	–	–	–	µs	
$T_{HDDATI2C}$	Data hold time	0	–	–	–	µs	
$T_{SUDATI2C}$	Data set-up time	250	–	–	–	ns	
$T_{SUSTOI2C}$	Set-up time for STOP Condition	4.0	–	–	–	µs	
T_{BUFI2C}	Bus free time between a STOP and START Condition	4.7	–	–	–	µs	
T_{SPI2C}	Pulse width of spikes are suppressed by the input filter.	–	–	–	–	ns	

Figure 13. Definition for Timing for Fast-/Standard-Mode on the I²C Bus



Note

22. A Fast-Mode I2C-bus device can be used in a Standard-Mode I²C-bus system, but the requirement $T_{SUDATI2C} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + T_{SUDATI2C} = 1000 + 250 = 1250$ ns (according to the Standard-Mode I2C-bus specification) before the SCL line is released.

Thermal Impedances

Table 36. Thermal Impedances by Package

Package	Typical θ_{JA} [23]
28-pin SSOP	95 °C/W
56-pin SSOP	67 °C/W

Capacitance on Crystal Pins

Table 37. Typical Package Capacitance on Crystal Pins

Package	Package Capacitance	
28-pin SSOP	2.8 pF	
56-pin SSOP	Pin 27 0.33 pF	Pin 31 0.35 pF

Solder Reflow Peak Temperature

Following is the minimum solder reflow peak temperature to achieve good solderability.

Table 38. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Time at Maximum Peak Temperature
28-pin SSOP	260 °C	30 s
56-pin SSOP	260 °C	30 s

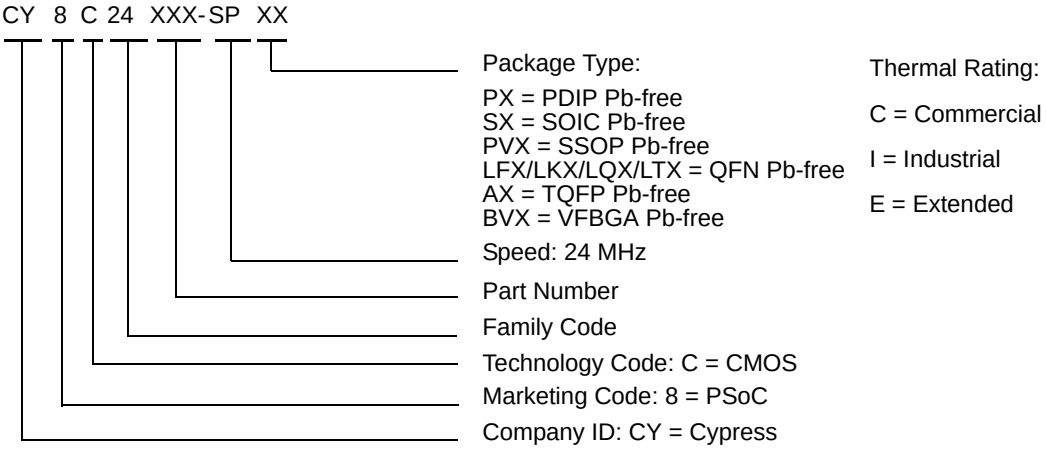
Ordering Information

The following table lists the CY8C24633 PSoC device family key package features and ordering codes .

Table 39. CY8C24x33 PSoC Device Family Key Features and Ordering Information

Package	Ordering Code	Flash (Kbytes)	RAM (Bytes)	Temperature Range	Digital Blocks (Rows of 4)	Analog Blocks (Columns of 3)	Digital I/O Pins	Analog Inputs	Analog Outputs	XRES Pin
28-Pin (210 Mil) SSOP	CY8C24633-24PVXI	8	256	–40 °C to +85 °C	4	4	25	12	2	Yes
28-Pin (210 Mil) SSOP (Tape and Reel)	CY8C24633-24PVXIT	8	256	–40 °C to +85 °C	4	4	25	12	2	Yes
56-Pin OCD SSOP	CY8C24033-24PVXI[24]	8	256	–40 °C to +85 °C	4	4	24	12	2	Yes

Ordering Code Definitions



Notes
23. $T_J = T_A + POWER \times \theta_{JA}$.
24. This part may be used for in-circuit debugging. It is NOT available for production.

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