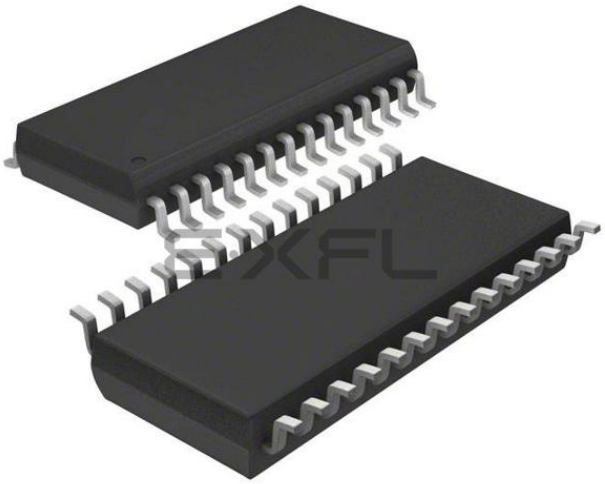


Welcome to E-XFL.COM

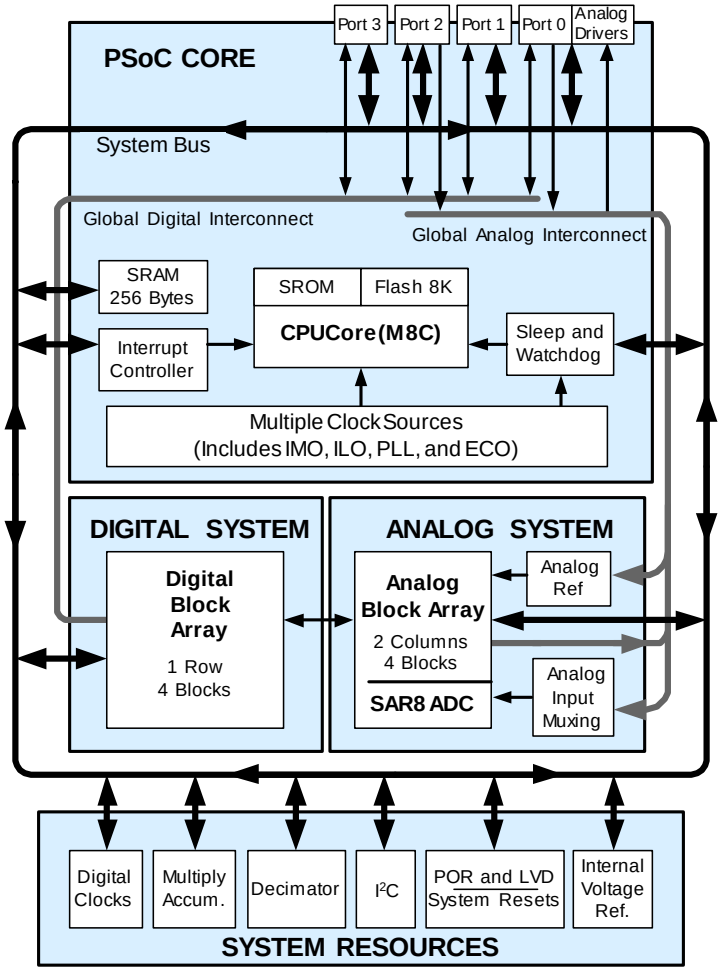
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	25
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.25V
Data Converters	A/D 2x14b; D/A 2x9b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c24633-24pvxit

Block Diagram



More Information

Cypress provides a wealth of data at www.cypress.com to help you to select the right PSoC device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the knowledge base article "How to Design with PSoC® 1, PowerPSoC®, and PLC – KBA88292". Following is an abbreviated list for PSoC 1:

- Overview: PSoC Portfolio, PSoC Roadmap
- Product Selectors: PSoC 1, PSoC 3, PSoC 4, PSoC 5LP
- In addition, PSoC Designer includes a device selection tool.
- Application notes: Cypress offers a large number of PSoC application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with PSoC 1 are:
  - Getting Started with PSoC® 1 – AN75320
  - PSoC® 1 - Getting Started with GPIO – AN2094
  - PSoC® 1 Analog Structure and Configuration – AN74170
  - PSoC® 1 Switched Capacitor Analog Blocks – AN2041
  - Selecting Analog Ground and Reference – AN2219

Note: For CY8C24633 devices related Application note please click here.

- Development Kits:
  - CY3210-PSoCEval1 supports all PSoC 1 Mixed-Signal Array families, including automotive, except CY8C25/26xxx devices. The kit includes an LCD module, potentiometer, LEDs, and breadboarding space.
  - CY3214-PSoCEvalUSB features a development board for the CY8C24x94 PSoC device. Special features of the board include USB and CapSense development and debugging support.

Note: For CY8C24633 devices related Development Kits please click here.

The MiniProg1 and MiniProg3 devices provide interfaces for flash programming and debug.

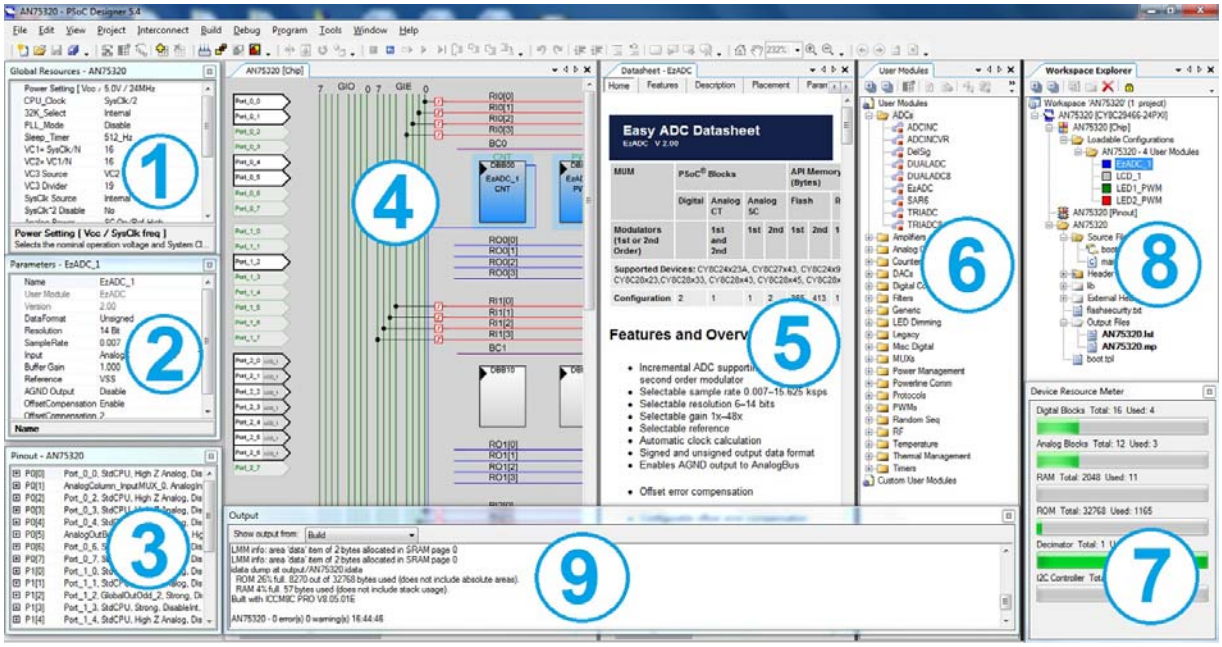
PSoC Designer

PSoC Designer is a free Windows-based Integrated Design Environment (IDE). Develop your applications using a library of pre-characterized analog and digital peripherals in a drag-and-drop design environment. Then, customize your design leveraging the dynamically generated API libraries of code. Figure 1 shows PSoC Designer windows. **Note:** This is not the default view.

1. **Global Resources –** all device hardware settings.
2. **Parameters –** the parameters of the currently selected User Modules.
3. **Pinout –** information related to device pins.
4. **Chip-Level Editor –** a diagram of the resources available on the selected chip.
5. **Datasheet –** the datasheet for the currently selected UM
6. **User Modules –** all available User Modules for the selected device.
7. **Device Resource Meter –** device resource usage for the current project configuration.
8. **Workspace –** a tree level diagram of files associated with the project.
9. **Output –** output from project build and debug operations.

Note: For detailed information on PSoC Designer, go to PSoC® Designer > Help > Documentation > Designer Specific Documents > IDE User Guide.

Figure 1. PSoC Designer Layout



PSoC Functional Overview

The PSoC family consists of many programmable system-on-chip with on-chip controller devices. These devices are designed to replace multiple traditional MCU-based system components with one, low cost single-chip programmable device. PSoC devices include configurable blocks of analog and digital logic, as well as programmable interconnects. This architecture allows the user to create customized peripheral configurations that match the requirements of each individual application. Additionally, a fast CPU, flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts and packages.

The PSoC architecture, as illustrated in the Block Diagram, is comprised of four main areas: PSoC core, digital system, Analog system, and system resources. Configurable global buses allows all the device resources to be combined into a complete custom system. The PSoC CY8C24x33 family can have up to three I/O ports that connect to the global digital and analog interconnects, providing access to four digital blocks and four analog blocks.

The PSoC Core

The PSoC core is a powerful engine that supports a rich feature set. The core includes a CPU, memory, clocks, and configurable general purpose I/O (GPIO).

The M8C CPU core is a powerful processor with speeds up to 24 MHz, providing a four MIPS 8-bit Harvard-architecture microprocessor. The CPU utilizes an interrupt controller with 11 vectors, to simplify programming of real time embedded events. Program execution is timed and protected using the included sleep and watch dog timers (WDT).

Memory encompasses 8 KB of flash for program storage, 256 bytes of SRAM for data storage, and up to 2 KB of EEPROM emulated using the flash. Program flash uses four protection levels on blocks of 64 bytes, allowing customized software IP protection.

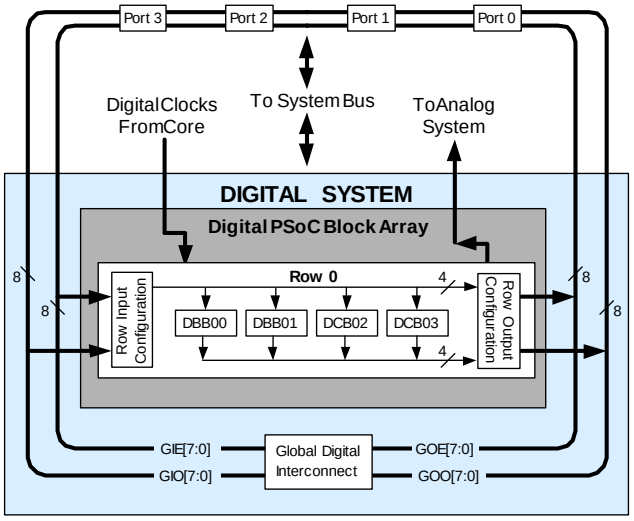
The PSoC device incorporates flexible internal clock generators, including a 24 MHz internal main oscillator (IMO) accurate to ±5% over temperature and voltage. The 24 MHz IMO can also be doubled to 48 MHz for use by the digital system. A low power 32 kHz internal low speed oscillator (ILO) is provided for the sleep timer and WDT. If crystal accuracy is desired, the ECO (32.768 kHz external crystal oscillator) is available for use as a real time clock (RTC) and can optionally generate a crystal-accurate 24 MHz system clock using a PLL. The clocks, together with programmable clock dividers (as a system resource), provide the flexibility to integrate almost any timing requirement into the PSoC device.

PSoC GPIOs provide connection to the CPU, digital and analog resources of the device. Each pin's drive mode may be selected from eight options, allowing great flexibility in external interfacing. Every pin also has the capability to generate a system interrupt on high level, low level, and change from last read.

The Digital System

The Digital System is composed of four digital PSoC blocks. Each block is an 8-bit resource that can be used alone or combined with other blocks to form 8-, 16-, 24-, and 32-bit peripherals, which are called user module references.

Figure 2. Digital System Block Diagram



Digital peripheral configurations include those listed below.

- PWMs (8- and 16-bit)
- PWMs with dead band (8- and 16-bit)
- Counters (8- to 32-bit)
- Timers (8- to 32-bit)
- UART 8 bit with selectable parity (up to 1)
- SPI master and slave (up to 1)
- I^2C slave and master (1 available as a system resource)
- Cyclical redundancy checker/generator (8- to 32-bit)
- IrDA (up to 1)
- Pseudo random sequence generators (8- to 32-bit)

The digital blocks are connected to any GPIO through a series of global buses that route any signal to any pin. The buses also allow signal multiplexing and performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

Digital blocks are provided in rows of four, where the number of blocks varies by PSoC device family. This allows the optimum choice of system resources for your application. Family resources are shown in Table 1 on page 7.

The Analog System

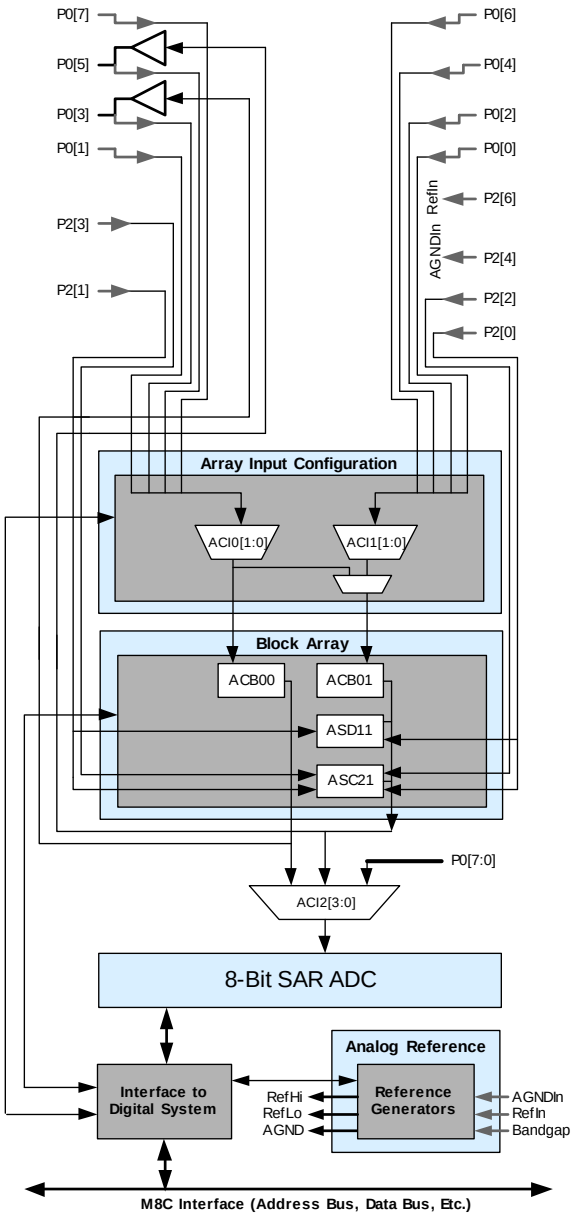
The analog system is composed of an 8-bit SAR ADC and four configurable blocks. The programmable 8-bit SAR ADC is an optimized ADC that runs up to 300 Ksps, with monotonic guarantee. It also has the features to support a motor control application.

Each analog block is comprised of an opamp circuit allowing the creation of complex analog signal flows. Analog peripherals are very flexible and can be customized to support specific application requirements. Some of the more common PSoC analog functions (most available as user modules) are listed below.

- Filters (2 and 4 pole band pass, low-pass, and notch)
- Amplifiers (up to two, with selectable gain to 48x)
- Instrumentation amplifiers (1 with selectable gain to 93x)
- Comparators (up to two, with 16 selectable thresholds)
- DACs (up to two, with 6- to 9-bit resolution)
- Multiplying DACs (up to 2, with 6- to 9-bit resolution)
- High current output drivers (two with 30 mA drive as a core resource)
- 1.3 V reference (as a system resource)
- DTMF dialer
- Modulators
- Correlators
- Peak detectors
- Many other topologies possible

Analog blocks are arranged in a column of three, which includes one continuous time (CT) and two switched capacitor (SC) blocks. The analog column 0 contains the SAR8 ADC block rather than the standard SC blocks.

Figure 3. Analog System Block Diagram



Additional System Resources

System resources, some of which have been previously listed, provide additional capability useful to complete systems. Additional resources include a multiplier, decimator, low voltage detection, and power on reset. Brief statements describing the merits of each system resource are presented below.

- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks can be routed to both the digital and analog systems. Additional clocks can be generated using digital PSoC blocks as clock dividers.
- A multiply accumulate (MAC) provides a fast 8-bit multiplier with 32-bit accumulate, to assist in both general math as well as digital filters.
- The decimator provides a custom hardware filter for digital signal processing applications including the creation of Delta Sigma ADCs.
- The I^2C module provides 100 and 400 kHz communication over two wires. Slave, master, and multi-master modes are all supported.
- Low-voltage detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced power-on reset (POR) circuit eliminates the need for a system supervisor.
- An internal 1.3 V reference provides an absolute reference for the analog system, including ADCs and DACs.

PSoC Device Characteristics

Depending on your PSoC device characteristics, the digital and analog systems can have 16, 8, or 4 digital blocks and 12, 6, or 3 analog blocks. The following table lists the resources available for specific PSoC device groups.

Table 1. PSoC Device Characteristics

PSoC Part Number	Digital I/O	Digital Rows	Digital Blocks	Analog Inputs	Analog Outputs	Analog Columns	Analog Blocks	SRAM Size	Flash Size	SAR ADC
CY8C29x66	up to 64	4	16	up to 12	4	4	12	2 K	32 K	No
CY8C28xxx	up to 44	up to 3	up to 12	up to 44	up to 4	up to 6	up to 12 + 4[1]	1 K	16 K	Yes
CY8C27x43	up to 44	2	8	up to 12	4	4	12	256	16 K	No
CY8C24x94	up to 56	1	4	up to 48	2	2	6	1 K	16 K	No
CY8C24x23A	up to 24	1	4	up to 12	2	2	6	256	4 K	No
CY8C23x33	up to 26	1	4	up to 12	2	2	4	256	8 K	Yes
CY8C22x45	up to 38	2	8	up to 38	0	4	6[1]	1 K	16 K	No
CY8C21x45	up to 24	1	4	up to 24	0	4	6[1]	512	8 K	Yes
CY8C21x34	up to 28	1	4	up to 28	0	2	4[1]	512	8 K	No
CY8C21x23	up to 16	1	4	up to 8	0	2	4[1]	256	4 K	No
CY8C20x34	up to 28	0	0	up to 28	0	0	3[1,2]	512	8 K	No
CY8C20xx6	up to 36	0	0	up to 36	0	0	3[1,2]	up to 2 K	up to 32 K	No

Notes
1. Limited analog functionality.
2. Two analog blocks and one CapSense®.

Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed-function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and lowering inventory costs. These configurable resources, called PSoC blocks, have the ability to implement a wide variety of user-selectable functions. The PSoC development process is:

1. Select user modules.
2. Configure user modules.
3. Organize and connect.
4. Generate, verify, and debug.

Select User Modules

PSoC Designer provides a library of prebuilt, pretested hardware peripheral components called “user modules.” User modules make selecting and implementing peripheral devices, both analog and digital, simple.

Configure User Modules

Each user module that you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a PWM User Module configures one or more digital PSoC blocks, one for each eight bits of resolution. Using these parameters, you can establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All of the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These user module datasheets explain the internal operation of the user module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information that you may need to successfully implement your design.

Organize and Connect

Build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. Perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides APIs with high-level functions to control and respond to hardware events at run time, and interrupt service routines that you can adapt as needed.

A complete code development environment lets you to develop and customize your applications in C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer's Debugger (accessed by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full-speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint, and watch-variable features, the debug interface provides a large trace buffer. It lets you to define complex breakpoint events that include monitoring address and data bus values, memory locations, and external signals.

Pinouts

The PSoC CY8C24633 is available in 28-pin SSOP and 56-pin SSOP OCD packages. Refer to the following information for details. Every port pin (labeled with a “P”), except V_{ss}, V_{dd}, and XRES in the following tables and illustrations, is capable of Digital I/O.

28-Pin Part Pinout

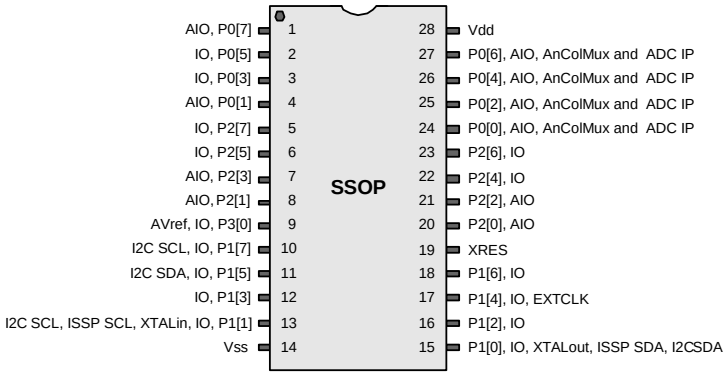
The 28-pin part is for the CY8C24633 PSoC device.

Table 2. 28-Pin Part Pinout (SSOP)

Pin No.	Digital	Analog	Pin Name	Description
1	I/O	I	P0[7]	Analog col mux IP and ADC IP
2	I/O	I/O	P0[5]	Analog col mux IP and column O/P and ADC IP
3	I/O	I/O	P0[3]	Analog col mux IP and column O/P and ADC IP
4	I/O	I	P0[1]	Analog col mux IP and ADC IP
5	I/O		P2[7]	GPIO
6	I/O		P2[5]	GPIO
7	I/O	I	P2[3]	Direct switched capacitor input
8	I/O	I	P2[1]	Direct switched capacitor input
9	I/O	AVref	P3[0][3]	GPIO/ADC Vref (optional)
10	I/O		P1[7]	I^2C SCL
11	I/O		P1[5]	I^2C SDA
12	I/O		P1[3]	GPIO
13	I/O		P1[1][4]	GPIO, Xtal input, I2C SCL, ISSP SCL
14	Power		Vss	Ground pin
15	I/O		P1[0][4]	GPIO, Xtal output, I2C SDA, ISSP SDA
16	I/O		P1[2]	GPIO
17	I/O		P1[4]	GPIO, external clock IP
18	I/O		P1[6]	GPIO
19			XRES	External reset
20	I/O	I	P2[0]	Direct switched capacitor input
21	I/O	I	P2[2]	Direct switched capacitor input
22	I/O		P2[4]	GPIO
23	I/O		P2[6]	GPIO
24	I/O	I	P0[0]	Analog Col Mux IP and ADC IP
25	I/O	I	P0[2]	Analog Col Mux IP and ADC IP
26	I/O	I	P0[4]	Analog Col Mux IP and ADC IP
27	I/O	I	P0[6]	Analog Col Mux IP and ADC IP
28	Power		Vdd	Supply voltage

LEGEND A = Analog, I = Input, and O = Output

Figure 4. CY8C24633 PSoC Device



Notes
3. Even though P3[0] is an odd port, it resides on the left side of the pinout.
4. ISSP pin, which is not High Z at POR.

Table 4. Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW		40			80			C0	
PRT0IE	01	RW		41			81			C1	
PRT0GS	02	RW		42			82			C2	
PRT0DM2	03	RW		43			83			C3	
PRT1DR	04	RW		44		ASD11CR0	84	RW		C4	
PRT1IE	05	RW		45		ASD11CR1	85	RW		C5	
PRT1GS	06	RW		46		ASD11CR2	86	RW		C6	
PRT1DM2	07	RW		47		ASD11CR3	87	RW		C7	
PRT2DR	08	RW		48			88			C8	
PRT2IE	09	RW		49			89			C9	
PRT2GS	0A	RW		4A			8A			CA	
PRT2DM2	0B	RW		4B			8B			CB	
PRT3DR	0C	RW		4C			8C			CC	
PRT3IE	0D	RW		4D			8D			CD	
PRT3GS	0E	RW		4E			8E			CE	
PRT3DM2	0F	RW		4F			8F			CF	
	10			50			90			D0	
	11			51			91			D1	
	12			52			92			D2	
	13			53			93			D3	
	14			54		ASC21CR0	94	RW		D4	
	15			55		ASC21CR1	95	RW		D5	
	16			56		ASC21CR2	96	RW	I^2C_CFG	D6	RW
	17			57		ASC21CR3	97	RW	I^2C_SCR	D7	#
	18			58			98		I^2C_DR	D8	RW
	19			59			99		I^2C_MSCR	D9	#
	1A			5A			9A		INT_CLR0	DA	RW
	1B			5B			9B		INT_CLR1	DB	RW
	1C			5C			9C			DC	
	1D			5D			9D		INT_CLR3	DD	RW
	1E			5E			9E		INT_MSK3	DE	RW
	1F			5F			9F			DF	
DBB00DR0	20	#	AMX_IN	60	RW		A0		INT_MSK0	E0	RW
DBB00DR1	21	W		61			A1		INT_MSK1	E1	RW
DBB00DR2	22	RW		62			A2		INT_VC	E2	RC
DBB00CR0	23	#	ARF_CR	63	RW		A3		RES_WDT	E3	W
DBB01DR0	24	#	CMP_CR0	64	#		A4		DEC_DH	E4	RC
DBB01DR1	25	W	ASY_CR	65	#		A5		DEC_DL	E5	RC
DBB01DR2	26	RW	CMP_CR1	66	RW		A6		DEC_CR0	E6	RW
DBB01CR0	27	#	SARADC_DL	67	RW		A7		DEC_CR1	E7	RW
DCB02DR0	28	#		68			A8		MUL0_X	E8	W
DCB02DR1	29	W	SARADC_C0	69	#		A9		MUL0_Y	E9	W
DCB02DR2	2A	RW	SARADC_C1	6A	RW		AA		MUL0_DH	EA	R
DCB02CR0	2B	#		6B			AB		MUL0_DL	EB	R
DCB03DR0	2C	#	TMP_DR0	6C	RW		AC		ACC0_DR1	EC	RW
DCB03DR1	2D	W	TMP_DR1	6D	RW		AD		ACC0_DR0	ED	RW
DCB03DR2	2E	RW	TMP_DR2	6E	RW		AE		ACC0_DR3	EE	RW
DCB03CR0	2F	#	TMP_DR3	6F	RW		AF		ACC0_DR2	EF	RW
	30		ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
	31		ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
	32		ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
	34		ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
	35		ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
	36		ACB01CR1 *	76	RW	RDI0RO1	B6	RW		F6	
	37		ACB01CR2 *	77	RW		B7		CPU_F	F7	RL
	38			78			B8			F8	
	39			79			B9			F9	
	3A			7A			BA			FA	
	3B			7B			BB			FB	
	3C			7C			BC			FC	
	3D			7D			BD			FD	
	3E			7E			BE		CPU_SCR1	FE	#
	3F			7F			BF		CPU_SCR0	FF	#

Blank fields are reserved. # Access is bit specific.

Absolute Maximum Ratings

Table 6. Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units	Notes
T_{STG}	Storage temperature	–55	25	+100	^{o}C	Higher storage temperatures reduce data retention time. Recommended storage temperature is +25 ^{o}C ± 25 ^{o}C. Extended duration storage temperatures above 65 ^{o}C degrade reliability.
$T_{BAKETEMP}$	Bake temperature	–	125	See package label	^{o}C	
$T_{BAKETIME}$	Bake time	See package label	–	72	hours	
T_A	Ambient temperature with power applied	-40	–	+85	^{o}C	
Vdd	Supply voltage on V_{dd} Relative to V_{ss}	-0.5	–	+6.0	V	
V_{IO}	DC input voltage	V_{ss} - 0.5	–	V_{dd} + 0.5	V	
V_{IOZ}	DC voltage applied to Tri-state	V_{ss} - 0.5	–	V_{dd} + 0.5	V	
I_{MIO}	Maximum current into any port pin	-25	–	+50	mA	
ESD	Electro static discharge voltage	2000	–	–	V	Human Body Model ESD.
LU	Latch up current	–	–	200	mA	

Operating Temperature

Table 7. Operating Temperature

Symbol	Description	Min	Typ	Max	Units	Notes
T_A	Ambient temperature	–40	–	+85	^{o}C	
T_J	Junction temperature	–40	–	+100	^{o}C	The temperature rise from ambient to junction is package specific. See Thermal Impedances by Package on page 41. The user must limit the power consumption to comply with this requirement.

DC Operational Amplifier Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

The operational amplifier is a component of both the analog continuous time PSoC blocks and the analog switched Cap PSoC blocks. The guaranteed specifications are measured in the analog continuous Time PSoC block. Typical parameters apply to 5 V at 25°C and are for design guidance only.

Table 10. 5 V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input offset voltage (absolute value) Power = Low, opamp bias = high Power = medium, opamp bias = high Power = high, opamp bias = high	 – – –	 1.6 1.3 1.2	 10 8 7.5	 mV mV mV	
TCV_{OSOA}	Average input offset voltage drift	–	7.0	35.0	µV/°C	
I_{EBOA}	Input leakage current (Port 0 Analog Pins)	–	20	–	pA	Gross tested to 1 µA.
C_{INOA}	Input capacitance (port 0 analog pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25 °C.
V_{CMOA}	Common mode voltage range Common Mode Voltage Range (high power or high opamp bias)	0.0 0.5	– –	V_{dd} V_{dd} - 0.5	V V	The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.
G_{OLOA}	Open loop gain Power = low, opamp bias = high Power = medium, opamp bias = high Power = high, opamp bias = high	 60 60 80	 – – –	 – – –	 dB dB dB	Specification is applicable at high power. For all other bias modes (except high power, high opamp bias), minimum is 60 dB.
$V_{OHIGHOA}$	High output voltage swing (internal signals) Power = low, opamp bias = high Power = medium, opamp bias = high Power = high, opamp bias = high	 V_{dd} - 0.2 V_{dd} - 0.2 V_{dd} - 0.5	 – – –	 – – –	 V V V	
V_{OLOWOA}	Low output voltage swing (internal signals) Power = low, opamp bias = high Power = medium, opamp bias = high Power = high, opamp bias = high	 – – –	 – – –	 0.2 0.2 0.5	 V V V	
I_{SOA}	Supply current (including associated AGND buffer) Power = low, opamp bias = high Power = medium, opamp bias = low Power = medium, opamp bias = high Power = high, opamp bias = low Power = high, opamp bias = high	 – – – – –	 300 600 1200 2400 4600	 400 800 1600 3200 6400	 µA µA µA µA µA	
$PSRR_{OA}$	Supply voltage rejection ratio	52	80	–	dB	V_{ss} ≤ VIN ≤ (V_{dd} -2.25) or (V_{dd} - 1.25 V) ≤ VIN ≤ V_{dd}.

DC Analog Reference Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

The guaranteed specifications are measured through the analog continuous time PSoC blocks. The power levels for AGND refer to the power of the analog continuous Time PSoC block. The power levels for RefHi and RefLo refer to the analog reference control register. The limits stated for AGND include the offset error of the AGND buffer local to the analog continuous time PSoC block. reference control power is high.

Table 15. 5-V DC Analog Reference Specifications

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b000	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.136	$V_{DD}/2$ + 1.288	$V_{DD}/2$ + 1.409	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.138	$V_{DD}/2$ + 0.003	$V_{DD}/2$ + 0.132	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.417	$V_{DD}/2$ – 1.289	$V_{DD}/2$ – 1.154	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.202	$V_{DD}/2$ + 1.290	$V_{DD}/2$ + 1.358	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.055	$V_{DD}/2$ + 0.001	$V_{DD}/2$ + 0.055	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.369	$V_{DD}/2$ – 1.295	$V_{DD}/2$ – 1.218	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.211	$V_{DD}/2$ + 1.292	$V_{DD}/2$ + 1.357	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.055	$V_{DD}/2$	$V_{DD}/2$ + 0.052	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.368	$V_{DD}/2$ – 1.298	$V_{DD}/2$ – 1.224	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.215	$V_{DD}/2$ + 1.292	$V_{DD}/2$ + 1.353	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.040	$V_{DD}/2$ – 0.001	$V_{DD}/2$ + 0.033	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.368	$V_{DD}/2$ – 1.299	$V_{DD}/2$ – 1.225	V
0b001	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.076	P2[4] + P2[6] – 0.021	P2[4] + P2[6] + 0.041	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.025	P2[4] – P2[6] + 0.011	P2[4] – P2[6] + 0.085	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.069	P2[4] + P2[6] – 0.014	P2[4] + P2[6] + 0.043	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.029	P2[4] – P2[6] + 0.005	P2[4] – P2[6] + 0.052	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.072	P2[4] + P2[6] – 0.011	P2[4] + P2[6] + 0.048	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.031	P2[4] – P2[6] + 0.002	P2[4] – P2[6] + 0.057	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.070	P2[4] + P2[6] – 0.009	P2[4] + P2[6] + 0.047	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.033	P2[4] – P2[6] + 0.001	P2[4] – P2[6] + 0.039	V

DC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 19. DC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{DDP}	V_{DD} for programming and erase	4.5	5	5.5	V	This specification applies to the functional requirements of external programmer tools
V_{DDLV}	Low V_{DD} for verify	3.0	3.1	3.2	V	This specification applies to the functional requirements of external programmer tools
V_{DDHV}	High V_{DD} for verify	5.1	5.2	5.3	V	This specification applies to the functional requirements of external programmer tools
$V_{DDIWRITE}$	Supply voltage for flash write operation	3.0	–	5.25	V	This specification applies to this device when it is executing internal flash writes
I_{DDP}	Supply current during programming or verify	–	5	25	mA	
V_{ILP}	Input low voltage during programming or verify	–	–	0.8	V	
V_{IHP}	Input high voltage during programming or verify	2.1	–	–	V	
I_{ILP}	Input current when applying V_{ilp} to P1[0] or P1[1] during programming or verify	–	–	0.2	mA	Driving internal pull-down resistor.
I_{IHP}	Input Current when applying Vihp to P1[0] or P1[1] During Programming or Verify	–	–	1.5	mA	Driving internal pull-down resistor.
V_{OLV}	Output low voltage during programming or verify	–	–	Vss + 0.75	V	
V_{OHV}	Output high voltage during programming or verify	V_{dd} - 1.0	–	Vdd	V	
$Flash_{ENPB}$	Flash endurance (per block)	50,000[9]	–	–	–	Erase/write cycles per block.
$Flash_{ENT}$	Flash endurance (total)[10]	1,800,000	–	–	–	Erase/write cycles.
$Flash_{DR}$	Flash data retention	10	–	–	Years	

Notes

9. The 50,000 cycle flash endurance per block will only be guaranteed if the flash is operating within one voltage range. Voltage ranges are 2.4 V to 3.0 V, 3.0 V to 3.6 V, and 4.75 V to 5.25 V.
10. A maximum of 36 x 50,000 block endurance cycles is allowed. This can be balanced between operations on 36x1 blocks of 50,000 maximum cycles each, 36x2 blocks of 25,000 maximum cycles each, or 36x4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36x50,000 and that no single block ever sees more than 50,000 cycles).
    For the full industrial range, use a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the flash APIs Application Note AN2015 at http://www.cypress.com under Application Notes for more information.

DC I²C Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 20. DC I²C Specifications[11]

Symbol	Description	Min	Typ	Max	Units	Notes
V_{ILI2C}	Input low level	–	–	0.3 × V_{DD}	V	3.0 V ≤ V_{DD} ≤ 3.6 V
		–	–	0.25 × V_{DD}	V	4.75 V ≤ V_{DD} ≤ 5.25 V
V_{IHI2C}	Input high level	0.7 × V_{DD}	–	–	V	3.0 V ≤ V_{DD} ≤ 5.25 V

SAR8 ADC DC Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 21. SAR8 ADC DC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
$V_{ADCVREF}$	Reference voltage at pin P3[0] when configured as ADC reference voltage	3.0	–	5.25	V	The voltage level at P3[0] (when configured as ADC reference voltage) should always be maintained to be less than chip supply voltage level on V_{dd} pin. $V_{ADCVREF}$ < V_{dd}.
$I_{ADCVREF}$	Current when P3[0] is configured as ADC V_{REF}	3	–	–	mA	
INL	R-2R integral non-linearity[12]	-1.2	–	+1.2	LSB	The maximum LSB is over a sub-range not exceeding 1/16 of the full-scale range.
DNL	R-2R differential non-linearity[13]	-1	–	+1	LSB	Output is monatonic.

Notes
11. All GPIOs meet the DC GPIO V_{IL} and V_{IH} specifications found in the DC GPIO Specifications sections. The I²C GPIO pins also meet the above specs.
12. At the 7F and 80 points, the maximum INL is 1.5 LSB.
13. For the 7F to 80 transition, the DNL specification is waived.

AC Electrical Characteristics

AC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 22. 5V and 3.3V AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{IMO24}	Internal main oscillator frequency for 24 MHz	22.8	24	25.2[14,15,16]	MHz	Trimmed for 5 V or 3.3 V operation using factory trim values. See Figure 5b on page 15. SLIMO mode = 0.
F_{IMO6}	Internal main oscillator frequency for 6 MHz	5.5	6	6.5[14,15,16]	MHz	Trimmed for 5 V or 3.3 V operation using factory trim values. See Figure 5b on page 15. SLIMO mode = 1.
F_{CPU1}	CPU frequency (5 V nominal)	0.093	24	24.6[14,15]	MHz	SLIMO mode = 0.
F_{CPU2}	CPU frequency (3.3 V nominal)	0.093	12	12.3[15,16]	MHz	SLIMO mode = 0.
F_{48M}	digital psoc block frequency	0	48	49.2[14,15,17]	MHz	Refer to the Table 27 on page 36.
F_{24M}	Digital PSoC block frequency	0	24	24.6[15,17]	MHz	
F_{32K1}	Internal low speed oscillator frequency	15	32	75	kHz	
F_{32K2}	External crystal oscillator	–	32.768	–	kHz	Accuracy is capacitor and crystal dependent. 50% duty cycle.
F_{32K_U}	Internal low speed oscillator untrimmed frequency	5	–	100	kHz	
F_{PLL}	PLL frequency	–	23.986	–	MHz	Is a multiple (x732) of crystal frequency.
DC_{ILO}	Internal low speed oscillator duty cycle	20	50	80	%	
$T_{PLLSLEW}$	PLL Lock time	0.5	–	10	ms	
$T_{PLLSLEWSLOW}$	PLL Lock time for low gain setting	0.5	–	50	ms	
T_{OS}	External crystal oscillator startup to 1%	–	1700	2620	ms	
T_{OSACC}	External crystal oscillator startup to 100 ppm	–	2800	3800	ms	The crystal oscillator frequency is within 100 ppm of its final value by the end of the T_{osacc} period. Correct operation assumes a properly loaded 1 uW maximum drive level 32.768 kHz crystal. 3.0 V ≤ V_{dd} ≤ 5.5 V, –40 °C ≤ T_A ≤ 85 °C.
T_{XRST}	External reset pulse width	10	–	–	µs	
DC24M	24 MHz duty cycle	40	50	60	%	
Step24M	24 MHz trim step size	–	50	–	kHz	
Fout48M	48 MHz output frequency	46.8	48.0	49.2[14,16]	MHz	Trimmed. Utilizing factory trim values.
F_{MAX}	Maximum frequency of signal on row input or row output.	–	–	12.3	MHz	
T_{RAMP}	Supply ramp time	NA	–	–	µs	
SR_{POWER_UP}	Power supply slew rate	–	–	250	V/ms	
$T_{POWERUP}$	Time from End of POR to CPU Executing Code	–	16	100	ms	
t_{jit_IMO} [18]	24 MHz IMO cycle-to-cycle jitter (RMS)	–	200	700	ps	
	24 MHz IMO long term N cycle-to-cycle jitter (RMS)	–	300	900	ps	N = 32
	24 MHz IMO period jitter (RMS)	–	100	400	ps	
t_{jit_PLL} [18]	24 MHz IMO cycle-to-cycle jitter (RMS)	–	200	800	ps	
	24 MHz IMO long term N cycle-to-cycle jitter (RMS)	–	300	1200	ps	N = 32
	24 MHz IMO period jitter (RMS)	–	100	700	ps	

Notes
14. 4.75V < Vdd < 5.25V.
15. Accuracy derived from Internal Main Oscillator with appropriate trim for Vdd range.
16. 3.0V < Vdd < 3.6V.
17. See the individual user module data sheets for information on maximum frequencies for user modules.
18. Refer to Cypress Jitter Specifications application note, Understanding Datasheet Jitter Specifications for Cypress Timing Products – AN5054 for more information.

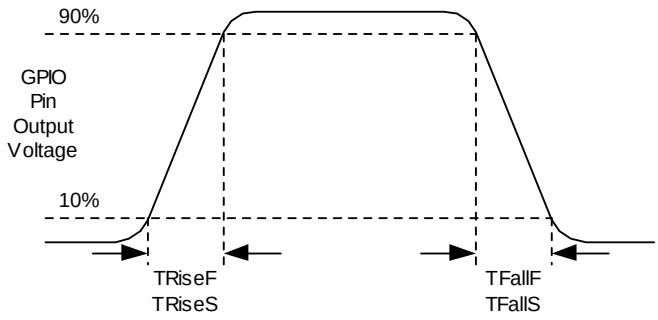
AC GPIO Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C an d are for design guidance only.

Table 23. 5 V and 3.3 V AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO operating frequency	0	–	12	MHz	Normal strong mode
TRiseF	Rise time, normal strong mode, Cload = 50 pF	3	–	18	ns	V_{dd} = 4.5 to 5.25 V, 10% - 90%
TFallF	Fall time, normal strong mode, Cload = 50 pF	2	–	18	ns	V_{dd} = 4.5 to 5.25 V, 10% - 90%
TRiseS	Rise time, slow strong mode, Cload = 50 pF	10	27	–	ns	V_{dd} = 3 to 5.25 V, 10% - 90%
TFallS	Fall time, slow strong mode, Cload = 50 pF	10	22	–	ns	V_{dd} = 3 to 5.25 V, 10% - 90%

Figure 10. GPIO Timing Diagram



AC Digital Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 27. 5-V and 3.3-V AC Digital Block Specifications

Function	Description	Min	Typ	Max	Unit	Notes
All functions	Block input clock frequency					
	V_{DD} ≥ 4.75 V	–	–	49.2	MHz	
	V_{DD} < 4.75 V	–	–	24.6	MHz	
Timer	Input clock frequency					
	No capture, V_{DD} ≥ 4.75 V	–	–	49.2	MHz	
	No capture, V_{DD} < 4.75 V	–	–	24.6	MHz	
	With capture	–	–	24.6	MHz	
	Capture pulse width	50[19]	–	–	ns	
Counter	Input clock frequency					
	No enable input, V_{DD} ≥ 4.75 V	–	–	49.2	MHz	
	No enable input, V_{DD} < 4.75 V	–	–	24.6	MHz	
	With enable input	–	–	24.6	MHz	
	Enable input pulse width	50[19]	–	–	ns	
Dead Band	Kill pulse width					
	Asynchronous restart mode	20	–	–	ns	
	Synchronous restart mode	50[19]	–	–	ns	
	Disable mode	50[19]	–	–	ns	
	Input clock frequency					
	V_{DD} ≥ 4.75 V	–	–	49.2	MHz	
	V_{DD} < 4.75 V	–	–	24.6	MHz	
CRCPRS (PRS Mode)	Input clock frequency					
	V_{DD} ≥ 4.75 V	–	–	49.2	MHz	
	V_{DD} < 4.75 V	–	–	24.6	MHz	
CRCPRS (CRC Mode)	Input clock frequency	–	–	24.6	MHz	
SPIM	Input clock frequency	–	–	8.2	MHz	The SPI serial clock (SCLK) frequency is equal to the input clock frequency divided by 2.
SPIS	Input clock (SCLK) frequency	–	–	4.1	MHz	The input clock is the SPI SCLK in SPIS mode.
	Width of SS_negated between transmissions	50[19]	–	–	ns	
Transmitter	Input clock frequency					The baud rate is equal to the input clock frequency divided by 8.
	V_{DD} ≥ 4.75 V, 2 stop bits	–	–	49.2	MHz	
	V_{DD} ≥ 4.75 V, 1 stop bit	–	–	24.6	MHz	
	V_{DD} < 4.75 V	–	–	24.6	MHz	
Receiver	Input clock frequency					The baud rate is equal to the input clock frequency divided by 8.
	V_{DD} ≥ 4.75 V, 2 stop bits	–	–	49.2	MHz	
	V_{DD} ≥ 4.75 V, 1 stop bit	–	–	24.6	MHz	
	V_{DD} < 4.75 V	–	–	24.6	MHz	

Note
19. 50 ns minimum input pulse width is based on the input synchronizers running at 24 MHz (42 ns nominal period).

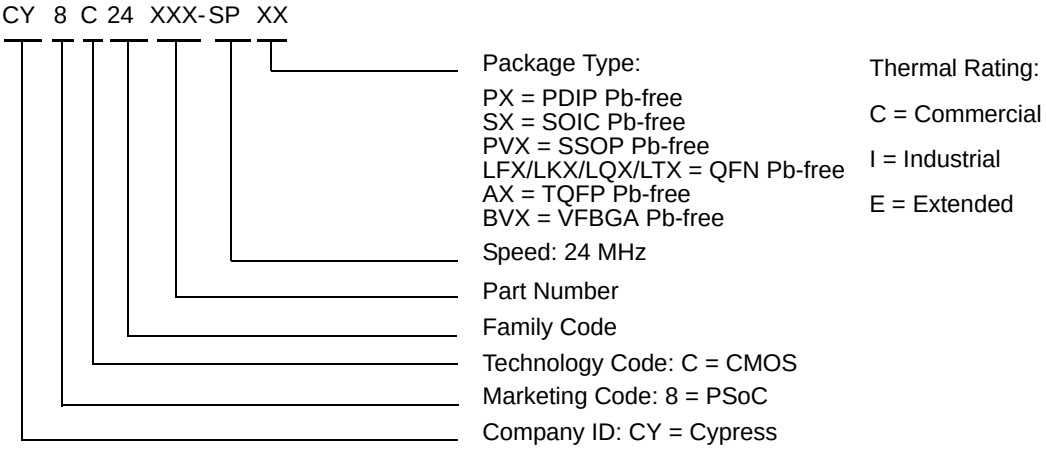
Ordering Information

The following table lists the CY8C24633 PSoC device family key package features and ordering codes .

Table 39. CY8C24x33 PSoC Device Family Key Features and Ordering Information

Package	Ordering Code	Flash (Kbytes)	RAM (Bytes)	Temperature Range	Digital Blocks (Rows of 4)	Analog Blocks (Columns of 3)	Digital I/O Pins	Analog Inputs	Analog Outputs	XRES Pin
28-Pin (210 Mil) SSOP	CY8C24633-24PVXI	8	256	–40 °C to +85 °C	4	4	25	12	2	Yes
28-Pin (210 Mil) SSOP (Tape and Reel)	CY8C24633-24PVXIT	8	256	–40 °C to +85 °C	4	4	25	12	2	Yes
56-Pin OCD SSOP	CY8C24033-24PVXI[24]	8	256	–40 °C to +85 °C	4	4	24	12	2	Yes

Ordering Code Definitions

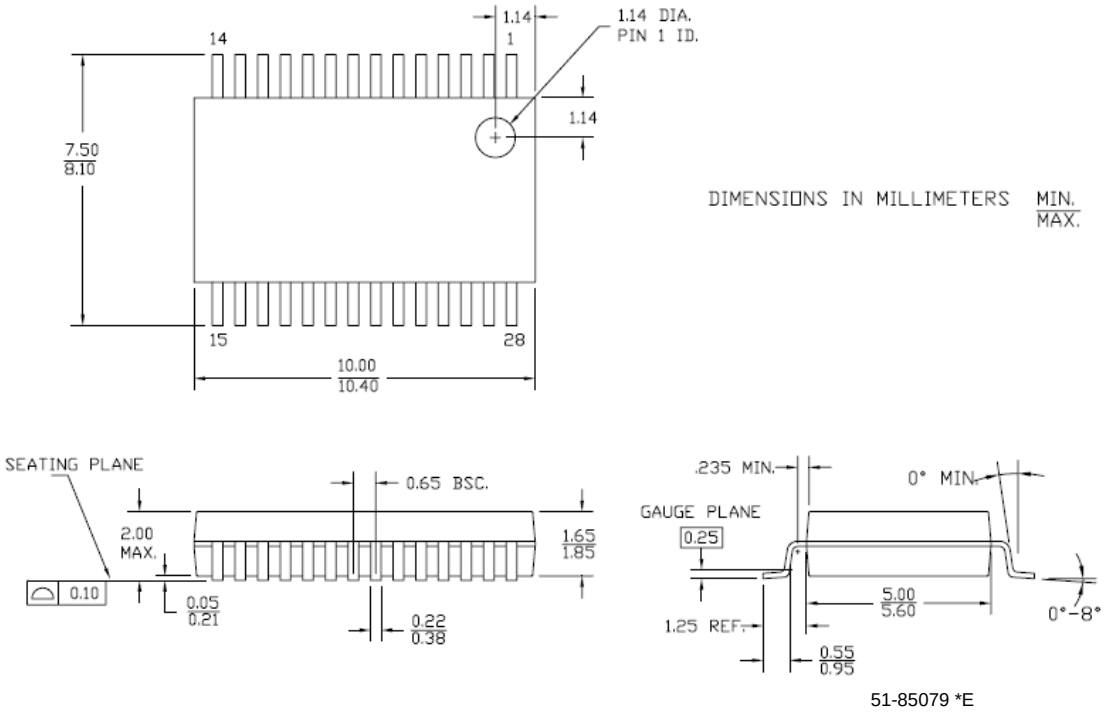


Notes
23. $T_J = T_A + POWER \times \theta_{JA}$.
24. This part may be used for in-circuit debugging. It is NOT available for production.

Packaging Information

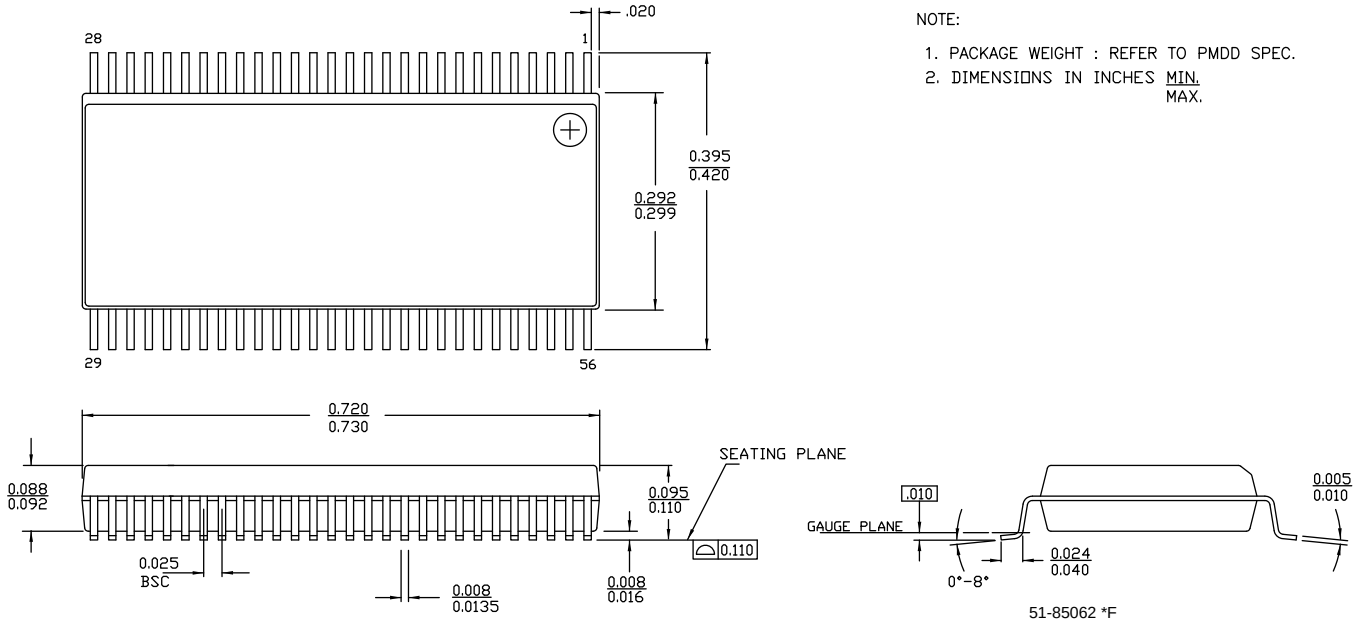
This section illustrates the packaging specifications for the CY8C24633 PSoC device, along with the thermal impedances for each package, solder reflow peak temperature, and the typical package capacitance on crystal pins.

Figure 14. 28-Pin (210-Mil) SSOP



51-85079 *E

Figure 15. 56-Pin (300-Mil) SSOP



51-85062 *F

mixed-signal	The reference to a circuit containing both analog and digital techniques and components.
modulator	A device that imposes a signal on a carrier.
noise	1. A disturbance that affects a signal and that may distort the information carried by the signal. The random variations of one or more characteristics of any entity such as voltage, current, or data.
oscillator	A circuit that may be crystal controlled and is used to generate a clock frequency.
parity	A technique for testing transmitting data. Typically, a binary digit is added to the data to make the sum of all the digits of the binary data either always even (even parity) or always odd (odd parity).
phase-locked loop (PLL)	An electronic circuit that controls an oscillator so that it maintains a constant phase angle relative to a reference signal.
pinouts	The pin number assignment: the relation between the logical inputs and outputs of the PSoC device and their physical counterparts in the printed circuit board (PCB) package. Pinouts involve pin numbers as a link between schematic and PCB design (both being computer generated files) and may also involve pin names.
port	A group of pins, usually eight.
power on reset (POR)	A circuit that forces the PSoC device to reset when the voltage is lower than a pre-set level. This is one type of hardware reset.
PSoC®	Cypress Semiconductor's PSoC® is a registered trademark and Programmable System-on-Chip™ is a trademark of Cypress.
PSoC Designer™	The software for Cypress' Programmable System-on-Chip technology.
pulse width modulator (PWM)	An output in the form of duty cycle which varies as a function of the applied measurand
RAM	An acronym for random access memory. A data-storage device from which data can be read out and new data can be written in.
register	A storage device with a specific capacity, such as a bit or byte.
reset	A means of bringing a system back to a know state. See hardware reset and software reset.
ROM	An acronym for read only memory. A data-storage device from which data can be read out, but new data cannot be written in.
serial	1. Pertaining to a process in which all events occur one after the other. Pertaining to the sequential or consecutive occurrence of two or more related activities in a single device or channel.
settling time	The time it takes for an output signal or value to stabilize after the input has changed from one value to another.
shift register	A memory storage device that sequentially shifts a word either left or right to output a stream of serial data.
slave device	A device that allows another device to control the timing for data exchanges between two devices. Or when devices are cascaded in width, the slave device is the one that allows another device to control the timing of data exchanges between the cascaded devices and an external interface. The controlling device is called the master device.

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