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#### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Discontinued at Digi-Key
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	72MHz
Connectivity	I <sup>2</sup> C, SMBus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	20
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.25К х 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 12x14b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	24-VFQFN Exposed Pad
Supplier Device Package	24-QFN (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm8lb10f16e-a-qfn24r

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### 2. Ordering Information



#### Figure 2.1. EFM8LB1 Part Numbering

All EFM8LB1 family members have the following features:

- CIP-51 Core running up to 72 MHz
- Three Internal Oscillators (72 MHz, 24.5 MHz and 80 kHz)
- SMBus
- I2C Slave
- SPI
- 2 UARTs
- · 6-Channel Programmable Counter Array (PWM, Clock Generation, Capture/Compare)
- · Six 16-bit Timers
- Four Configurable Logic Units
- 14-bit Analog-to-Digital Converter with integrated multiplexer, voltage reference, temperature sensor, channel sequencer, and directto-XRAM data transfer
- Two Analog Comparators
- 16-bit CRC Unit
- AEC-Q100 qualified (pending)

In addition to these features, each part number in the EFM8LB1 family has a set of features that vary across the product line. The product selection guide shows the features available on each family member.

### Table 2.1. Product Selection Guide

Ordering Part Number	Flash Memory (kB)	RAM (Bytes)	Digital Port I/Os (Total)	ADC0 Channels	Voltage DACs	Comparator 0 Inputs	Comparator 1 Inputs	Pb-free (RoHS Compliant)	Temperature Range	Package
EFM8LB12F64E-A-QFN32	64	4352	29	20	4	10	9	Yes	-40 to +105 °C	QFN32
EFM8LB12F64E-A-QFP32	64	4352	28	20	4	10	9	Yes	-40 to +105 °C	QFP32
EFM8LB12F64E-A-QFN24	64	4352	20	12	4	6	6	Yes	-40 to +105 °C	QFN24
EFM8LB12F64E-A-QSOP24	64	4352	21	13	4	6	7	Yes	-40 to +105 °C	QSOP24

#### Universal Asynchronous Receiver/Transmitter (UART1)

UART1 is an asynchronous, full duplex serial port offering a variety of data formatting options. A dedicated baud rate generator with a 16-bit timer and selectable prescaler is included, which can generate a wide range of baud rates. A received data FIFO allows UART1 to receive multiple bytes before data is lost and an overflow occurs.

UART1 provides the following features:

- · Asynchronous transmissions and receptions
- Dedicated baud rate generator supports baud rates up to SYSCLK/2 (transmit) or SYSCLK/8 (receive)
- 5, 6, 7, 8, or 9 bit data
- Automatic start and stop generation
- Automatic parity generation and checking
- · Single-byte buffer on transmit and receive
- Auto-baud detection
- · LIN break and sync field detection
- CTS / RTS hardware flow control

#### Serial Peripheral Interface (SPI0)

The serial peripheral interface (SPI) module provides access to a flexible, full-duplex synchronous serial bus. The SPI can operate as a master or slave device in both 3-wire or 4-wire modes, and supports multiple masters and slaves on a single SPI bus. The slave-select (NSS) signal can be configured as an input to select the SPI in slave mode, or to disable master mode operation in a multi-master environment, avoiding contention on the SPI bus when more than one master attempts simultaneous data transfers. NSS can also be configured as a firmware-controlled chip-select output in master mode, or disable to reduce the number of pins required. Additional general purpose port I/O pins can be used to select multiple slave devices in master mode.

- Supports 3- or 4-wire master or slave modes
- · Supports external clock frequencies up to 12 Mbps in master or slave mode
- · Support for all clock phase and polarity modes
- 8-bit programmable clock rate (master)
- Programmable receive timeout (slave)
- Two byte FIFO on transmit and receive
- · Can operate in suspend or snooze modes and wake the CPU on reception of a byte
- · Support for multiple masters on the same data lines

#### System Management Bus / I2C (SMB0)

The SMBus I/O interface is a two-wire, bi-directional serial bus. The SMBus is compliant with the System Management Bus Specification, version 1.1, and compatible with the I<sup>2</sup>C serial bus.

The SMBus module includes the following features:

- · Standard (up to 100 kbps) and Fast (400 kbps) transfer speeds
- · Support for master, slave, and multi-master modes
- Hardware synchronization and arbitration for multi-master mode
- · Clock low extending (clock stretching) to interface with faster masters
- · Hardware support for 7-bit slave and general call address recognition
- Firmware support for 10-bit slave address decoding
- · Ability to inhibit all slave states
- Programmable data setup/hold times
- Transmit and receive buffers to help increase throughput in faster applications

### 3.7 Analog

### 14/12/10-Bit Analog-to-Digital Converter (ADC0)

The ADC is a successive-approximation-register (SAR) ADC with 14-, 12-, and 10-bit modes, integrated track-and hold and a programmable window detector. The ADC is fully configurable under software control via several registers. The ADC may be configured to measure different signals using the analog multiplexer. The voltage reference for the ADC is selectable between internal and external reference sources.

- Up to 20 external inputs
- Single-ended 14-bit, 12-bit and 10-bit modes
- Supports an output update rate of up to 1 Msps in 12-bit mode
- · Channel sequencer logic with direct-to-XDATA output transfers
- Operation in a low power mode at lower conversion speeds
- Asynchronous hardware conversion trigger, selectable between software, external I/O and internal timer and configurable logic sources
- Output data window comparator allows automatic range checking
- Support for output data accumulation
- Conversion complete and window compare interrupts supported
- Flexible output data formatting
- Includes a fully-internal fast-settling 1.65 V reference and an on-chip precision 2.4 / 1.2 V reference, with support for using the supply as the reference, an external reference and signal ground
- Integrated factory-calibrated temperature sensor

## 12-Bit Digital-to-Analog Converters (DAC0, DAC1, DAC2, DAC3)

The DAC modules are 12-bit Digital-to-Analog Converters with the capability to synchronize multiple outputs together. The DACs are fully configurable under software control. The voltage reference for the DACs is selectable between internal and external reference sources.

- Voltage output with 12-bit performance
- · Hardware conversion trigger, selectable between software, external I/O and internal timer and configurable logic sources
- · Outputs may be configured to persist through reset and maintain output state to avoid system disruption
- Multiple DAC outputs can be synchronized together
- DAC pairs (DAC0 and 1 or DAC2 and 3) support complementary output waveform generation
- · Outputs may be switched between two levels according to state of configurable logic / PWM input trigger
- Flexible input data formatting
- · Supports references from internal supply, on-chip precision reference, or external VREF pin

### Low Current Comparators (CMP0, CMP1)

An analog comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. External input connections to device I/O pins and internal connections are available through separate multiplexers on the positive and negative inputs. Hysteresis, response time, and current consumption may be programmed to suit the specific needs of the application.

The comparator includes the following features:

- · Up to 10 (CMP0) or 9 (CMP1) external positive inputs
- · Up to 10 (CMP0) or 9 (CMP1) external negative inputs
- · Additional input options:
  - Internal connection to LDO output
  - Direct connection to GND
  - Direct connection to VDD
  - Dedicated 6-bit reference DAC
- Synchronous and asynchronous outputs can be routed to pins via crossbar
- Programmable hysteresis between 0 and ±20 mV
- Programmable response time
- Interrupts generated on rising, falling, or both edges
- PWM output kill feature

### 4. Electrical Specifications

#### 4.1 Electrical Characteristics

All electrical parameters in all tables are specified under the conditions listed in Table 4.1 Recommended Operating Conditions on page 13, unless stated otherwise.

Table 4.1. Recommended Operating Conditions

### 4.1.1 Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Operating Supply Voltage on VDD	V <sub>DD</sub>		2.2	_	3.6	V
Operating Supply Voltage on VIO <sup>2,</sup> 3	V <sub>IO</sub>		TBD		V <sub>DD</sub>	V
System Clock Frequency	f <sub>SYSCLK</sub>		0	—	73.5	MHz
Operating Ambient Temperature	T <sub>A</sub>		-40	—	105	°C
Neter						

#### Note:

1. All voltages with respect to GND

2. In certain package configurations, the VIO and VDD supplies are bonded to the same pin.

3. GPIO levels are undefined whenever VIO is less than 1 V.

### 4.1.4 Flash Memory

Parameter	Symbol	Test Condition	Min	Тур	Max	Units
Write Time <sup>1,2</sup>	t <sub>WRITE</sub>	One Byte,	19	20	21	μs
		F <sub>SYSCLK</sub> = 24.5 MHz				
Erase Time <sup>1 ,2</sup>	t <sub>ERASE</sub>	One Page,	5.2	5.35	5.5	ms
		F <sub>SYSCLK</sub> = 24.5 MHz				
V <sub>DD</sub> Voltage During Programming <sup>3</sup>	V <sub>PROG</sub>		2.2		3.6	V
Endurance (Write/Erase Cycles)	N <sub>WE</sub>		20k	100k		Cycles

### Table 4.4. Flash Memory

Note:

1. Does not include sequencing time before and after the write/erase operation, which may be multiple SYSCLK cycles.

2. The internal High-Frequency Oscillator 0 has a programmable output frequency, which is factory programmed to 24.5 MHz. If user firmware adjusts the oscillator speed, it must be between 22 and 25 MHz during any flash write or erase operation. It is recommended to write the HFO0CAL register back to its reset value when writing or erasing flash.

3. Flash can be safely programmed at any voltage above the supply monitor threshold (V<sub>VDDM</sub>).

4. Data Retention Information is published in the Quarterly Quality and Reliability Report.

#### 4.1.5 Power Management Timing

#### Table 4.5. Power Management Timing

Parameter	Symbol	Test Condition	Min	Тур	Max	Units
Idle Mode Wake-up Time	t <sub>IDLEWK</sub>		2	_	3	SYSCLKs
Suspend Mode Wake-up Time	t <sub>SUS-</sub>	SYSCLK = HFOSC0	—	170	_	ns
	PENDWK	CLKDIV = 0x00				
Snooze Mode Wake-up Time	t <sub>SLEEPWK</sub>	SYSCLK = HFOSC0	—	12	_	μs
		CLKDIV = 0x00				

## 4.1.8 Crystal Oscillator

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Crystal Frequency	f <sub>XTAL</sub>		0.02	_	25	MHz
Crystal Drive Current	I <sub>XTAL</sub>	XFCN = 0	—	0.5	_	μA
		XFCN = 1	—	1.5	_	μA
		XFCN = 2	—	4.8	_	μA
		XFCN = 3	—	14	—	μA
		XFCN = 4	_	40	_	μA
		XFCN = 5	—	120	_	μA
		XFCN = 6	_	550	_	μA
		XFCN = 7		2.6		mA

### Table 4.8. Crystal Oscillator

## 4.1.10 Voltage Reference

Table 4.1	0. Volt	age Re	ference
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Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Internal Fast Settling Reference		1			1	
Output Voltage	V <sub>REFFS</sub>		1.62	1.65	1.68	V
(Full Temperature and Supply Range)						
Temperature Coefficient	TC <sub>REFFS</sub>			50	_	ppm/°C
Turn-on Time	t <sub>REFFS</sub>		_	_	1.5	μs
Power Supply Rejection	PSRR <sub>REF</sub> FS			400		ppm/V
On-chip Precision Reference						
Valid Supply Range	V <sub>DD</sub>	1.2 V Output	2.2		3.6	V
		2.4 V Output	2.7	_	3.6	V
Output Voltage	V <sub>REFP</sub>	1.2 V Output, T = 25 °C	TBD	1.2	TBD	V
		2.4 V Output, T = 25 °C	TBD	2.4	TBD	V
Turn-on Time, settling to 0.5 LSB	t <sub>VREFP</sub>	4.7 μF tantalum + 0.1 μF ceramic bypass on VREF pin	_	3	_	ms
		0.1 µF ceramic bypass on VREF pin	_	100	_	μs
Load Regulation	LR <sub>VREFP</sub>	Load = 0 to 200 µA to GND	—	TBD	—	μV/μΑ
Load Capacitor	C <sub>VREFP</sub>	Load = 0 to 200 µA to GND	0.1	_	_	μF
Short-circuit current	ISC <sub>VREFP</sub>		—	_	8	mA
Power Supply Rejection	PSRR <sub>VRE</sub> FP		_	TBD	_	ppm/V
External Reference			1	1	1	
Input Current	I <sub>EXTREF</sub>	ADC Sample Rate = 1 Msps; VREF = 3.0 V	_	5	_	μA

### 4.1.13 Comparators

Parameter	Symbol	Test Condition	Min	Тур	Мах	Unit
Response Time, CPMD = 00	t <sub>RESP0</sub>	+100 mV Differential		100	_	ns
(Highest Speed)		-100 mV Differential	_	150	_	ns
Response Time, CPMD = 11 (Low-	t <sub>RESP3</sub>	+100 mV Differential		1.5	_	μs
est Power)		-100 mV Differential		3.5	_	μs
Positive Hysteresis	HYS <sub>CP+</sub>	CPHYP = 00		0.4	_	mV
Mode 0 (CPMD = 00)		CPHYP = 01		8		mV
		CPHYP = 10		16		mV
		CPHYP = 11		32	_	mV
Negative Hysteresis	HYS <sub>CP-</sub>	CPHYN = 00		-0.4		mV
Mode 0 (CPMD = 00)		CPHYN = 01		-8	_	mV
		CPHYN = 10		-16	_	mV
		CPHYN = 11		-32	_	mV
Positive Hysteresis	HYS <sub>CP+</sub>	CPHYP = 00		0.5	_	mV
Mode 1 (CPMD = 01)		CPHYP = 01		6	_	mV
		CPHYP = 10	_	12	_	mV
		CPHYP = 11	_	24	_	mV
Negative Hysteresis	HYS <sub>CP-</sub>	CPHYN = 00	_	-0.5	_	mV
Mode 1 (CPMD = 01)		CPHYN = 01	_	-6	_	mV
		CPHYN = 10	_	-12	_	mV
		CPHYN = 11	_	-24	_	mV
Positive Hysteresis	HYS <sub>CP+</sub>	CPHYP = 00	_	0.7	_	mV
Mode 2 (CPMD = 10)		CPHYP = 01	_	4.5	_	mV
		CPHYP = 10	_	9	_	mV
		CPHYP = 11	_	18	_	mV
Negative Hysteresis	HYS <sub>CP-</sub>	CPHYN = 00	_	-0.6	_	mV
Mode 2 (CPMD = 10)		CPHYN = 01	_	-4.5	_	mV
		CPHYN = 10	_	-9	_	mV
		CPHYN = 11		-18	_	mV
Positive Hysteresis	HYS <sub>CP+</sub>	CPHYP = 00	_	1.5	_	mV
Mode 3 (CPMD = 11)		CPHYP = 01	_	4	_	mV
		CPHYP = 10	_	8	_	mV
		CPHYP = 11		16	_	mV

#### Table 4.13. Comparators

### 4.2 Thermal Conditions

#### Table 4.16. Thermal Conditions

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Thermal Resistance	θ <sub>JA</sub>	QFN24 Packages	—	TBD	_	°C/W
		QFN32 Packages	—	TBD	_	°C/W
		QFP32 Packages	_	80	_	°C/W
		QSOP24 Packages	—	65	—	°C/W
Note: 1. Thermal resistance assumes a	multi-layer F	PCB with any exposed pad soldered to	a PCB pad.			

#### 4.3 Absolute Maximum Ratings

Stresses above those listed in Table 4.17 Absolute Maximum Ratings on page 27 may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at http://www.silabs.com/support/quality/pages/default.aspx.

Table 4.17.	Absolute	Maximum	Ratings
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Parameter	Symbol	Test Condition	Min	Max	Unit
Ambient Temperature Under Bias	T <sub>BIAS</sub>		-55	125	°C
Storage Temperature	T <sub>STG</sub>		-65	150	°C
Voltage on VDD	V <sub>DD</sub>		GND-0.3	4.2	V
Voltage on VIO <sup>2</sup>	V <sub>IO</sub>		GND-0.3	V <sub>DD</sub> +0.3	V
Voltage on I/O pins or RSTb, excluding	V <sub>IN</sub>	V <sub>IO</sub> > TBD V	GND-0.3	TBD	V
P3.0-P3.3 (QFN32 and QFP32)		V <sub>IO</sub> < TBD V	GND-0.3 TBD	TBD	V
Voltage on P2.0-P2.3 (QFN24 and QSOP24) or P3.0-P3.3 (QFN32 and QFP32)	V <sub>IN</sub>		GND-0.3	V <sub>DD</sub> +0.3	V
Total Current Sunk into Supply Pin	I <sub>VDD</sub>		—	400	mA
Total Current Sourced out of Ground Pin	I <sub>GND</sub>		400	—	mA
Current Sourced or Sunk by any I/O Pin or RSTb	I <sub>IO</sub>		-100	100	mA

#### Note:

1. Exposure to maximum rating conditions for extended periods may affect device reliability.

2. In certain package configurations, the VIO and VDD supplies are bonded to the same pin.

#### 5.2 Debug

The diagram below shows a typical connection diagram for the debug connections pins. The pin sharing resistors are only required if the functionality on the C2D (a GPIO pin) and the C2CK (RSTb) is routed to external circuitry. For example, if the RSTb pin is connected to an external switch with debouncing filter or if the GPIO sharing with the C2D pin is connected to an external circuit, the pin sharing resistors and connections to the debug adapter must be placed on the hardware. Otherwise, these components and connections can be omitted.

For more information on debug connections, see the example schematics and information available in AN127: "Pin Sharing Techniques for the C2 Interface." Application notes can be found on the Silicon Labs website (http://www.silabs.com/8bit-appnotes) or in Simplicity Studio.



Figure 5.2. Debug Connection Diagram

#### 5.3 Other Connections

Other components or connections may be required to meet the system-level requirements. Application Note AN203: "8-bit MCU Printed Circuit Board Design Notes" contains detailed information on these connections. Application Notes can be accessed on the Silicon Labs website (www.silabs.com/8bit-appnotes).

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
22	P1.3	Multifunction I/O	Yes	P1MAT 3	
				CLU0B 13	
				CLU1B.11	
				CLU2B 11	
				CLU3A.13	
23	P1.2	Multifunction I/O	Yes	P1MAT.2	ADC0.8
				CLU0A.13	CMP0P.8
				CLU1A.11	CMP0N.8
				CLU2B.10	
				CLU3A.12	
				CLU3B.13	
24	P1.1	Multifunction I/O	Yes	P1MAT.1	ADC0.7
				CLU0B.12	CMP0P.7
				CLU1B.10	CMP0N.7
				CLU2A.11	
				CLU3B.12	
25	P1.0	Multifunction I/O	Yes	P1MAT.0	ADC0.6
				CLU1OUT	CMP0P.6
				CLU0A.12	CMP0N.6
				CLU1A.10	CMP1P.1
				CLU2A.10	CMP1N.1
26	P0.7	Multifunction I/O	Yes	P0MAT.7	ADC0.5
				INT0.7	CMP0P.5
				INT1.7	CMP0N.5
				CLU0B.11	CMP1P.0
				CLU1B.9	CMP1N.0
				CLU3A.11	
27	P0.6	Multifunction I/O	Yes	P0MAT.6	ADC0.4
				CNVSTR	CMP0P.4
				INT0.6	CMP0N.4
				INT1.6	
				CLU0A.11	
				CLU1B.8	
				CLU3A.10	

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
18	P1.7	Multifunction I/O	Yes	P1MAT.7	ADC0.13
				CLU0B.15	CMP0P.9
				CLU1B.13	CMP0N.9
				CLU2A.13	
19	P1.6	Multifunction I/O	Yes	P1MAT.6	ADC0.12
				CLU0A.15	
				CLU1B.12	
				CLU2A.12	
20	P1.5	Multifunction I/O	Yes	P1MAT.5	ADC0.11
				CLU0B.14	
				CLU1A.13	
				CLU2B.13	
				CLU3B.11	
21	P1.4	Multifunction I/O	Yes	P1MAT.4	ADC0.10
				CLU0A.14	
				CLU1A.12	
				CLU2B.12	
				CLU3B.10	
22	P1.3	Multifunction I/O	Yes	P1MAT.3	ADC0.9
				CLU0B.13	
				CLU1B.11	
				CLU2B.11	
				CLU3A.13	
23	P1.2	Multifunction I/O	Yes	P1MAT.2	ADC0.8
				CLU0A.13	CMP0P.8
				CLU1A.11	CMP0N.8
				CLU2B.10	
				CLU3A.12	
				CLU3B.13	
24	P1.1	Multifunction I/O	Yes	P1MAT.1	ADC0.7
				CLU0B.12	CMP0P.7
				CLU1B.10	CMP0N.7
				CLU2A.11	
				CLU3B.12	

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
25	P1.0	Multifunction I/O	Yes	P1MAT.0	ADC0.6
				CLU1OUT	CMP0P.6
				CLU0A.12	CMP0N.6
				CLU1A.10	CMP1P.1
				CLU2A.10	CMP1N.1
26	P0.7	Multifunction I/O	Yes	P0MAT.7	ADC0.5
				INT0.7	CMP0P.5
				INT1.7	CMP0N.5
				CLU0B.11	CMP1P.0
				CLU1B.9	CMP1N.0
				CLU3A.11	
27	P0.6	Multifunction I/O	Yes	P0MAT.6	ADC0.4
				CNVSTR	CMP0P.4
				INT0.6	CMP0N.4
				INT1.6	
				CLU0A.11	
				CLU1B.8	
				CLU3A.10	
28	P0.5	Multifunction I/O	Yes	P0MAT.5	ADC0.3
				INT0.5	CMP0P.3
				INT1.5	CMP0N.3
				UART0_RX	
				CLU0B.10	
				CLU1A.9	
29	P0.4	Multifunction I/O	Yes	P0MAT.4	ADC0.2
				INT0.4	CMP0P.2
				INT1.4	CMP0N.2
				UART0_TX	
				CLU0A.10	
				CLU1A.8	

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
30	P0.3	Multifunction I/O	Yes	P0MAT.3	XTAL2
				EXTCLK	
				INT0.3	
				INT1.3	
				CLU0B.9	
				CLU2B.10	
				CLU3A.9	
31	P0.2	Multifunction I/O	Yes	P0MAT.2	XTAL1
				INT0.2	ADC0.1
				INT1.2	CMP0P.1
				CLU0OUT	CMP0N.1
				CLU0A.9	
				CLU2B.8	
				CLU3A.8	
32	P0.1	Multifunction I/O	Yes	P0MAT.1	ADC0.0
				INT0.1	CMP0P.0
				INT1.1	CMP0N.0
				CLU0B.8	AGND
				CLU2A.9	
				CLU3B.9	





Table 6.3.	<b>Pin Definitions</b>	for EFM8LB1x	-QFN24
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Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	P0.1	Multifunction I/O	Yes	P0MAT.1	ADC0.0
				INT0.1	CMP0P.0
				INT1.1	CMP0N.0
				CLU0B.8	AGND
				CLU2A.9	
				CLU3B.9	





Pin	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
Number					
1	P0.3	Multifunction I/O	Yes	P0MAT.3	XTAL2
				EXTCLK	
				INT0.3	
				INT1.3	
				CLU0B.9	
				CLU2B.10	
				CLU3A.9	

Dimension	Min	Мах				
Note:						
1. All dimensions shown are in millimeters	(mm) unless otherwise noted.					
2. Dimensioning and Tolerancing is per the	e ANSI Y14.5M-1994 specification.					
3. This Land Pattern Design is based on the	ne IPC-7351 guidelines.					
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabri- cation Allowance of 0.05mm.						
5. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad.						
6. A stainless steel, laser-cut and electro-p	6. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release					
7. The stencil thickness should be 0.125 m	7. The stencil thickness should be 0.125 mm (5 mils).					
8. The ratio of stencil aperture to land pad	8. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.					
9. A 2 x 2 array of 1.10 mm square openin	gs on a 1.30 mm pitch should be used for the	center pad.				

- 10. A No-Clean, Type-3 solder paste is recommended.
- 11. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

### 7.3 QFN32 Package Marking



Figure 7.3. QFN32 Package Marking

The package marking consists of:

- PPPPPPP The part number designation.
- TTTTTT A trace or manufacturing code.
- YY The last 2 digits of the assembly year.
- WW The 2-digit workweek when the device was assembled.
- # The device revision (A, B, etc.).





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# 9. QFN24 Package Specifications

### 9.1 QFN24 Package Dimensions



Figure 9.1. QFN24 Package Drawing

Dimension	Min	Тур	Мах	
A	0.8	0.85	0.9	
A1	0.00	—	0.05	
A2	—	0.65	—	
A3	0.203 REF			
b	0.15	0.2	0.25	
b1	0.25	0.3	0.35	
D	3.00 BSC			
E		3.00 BSC		



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