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### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Discontinued at Digi-Key
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	72MHz
Connectivity	I <sup>2</sup> C, SMBus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	20
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 12x14b; D/A 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	24-VFQFN Exposed Pad
Supplier Device Package	24-QFN (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm8lb12f32e-a-qfn24r

Email: info@E-XFL.COM

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## Timers (Timer 0, Timer 1, Timer 2, Timer 3, Timer 4, and Timer 5)

Several counter/timers are included in the device: two are 16-bit counter/timers compatible with those found in the standard 8051, and the rest are 16-bit auto-reload timers for timing peripherals or for general purpose use. These timers can be used to measure time intervals, count external events and generate periodic interrupt requests. Timer 0 and Timer 1 are nearly identical and have four primary modes of operation. The other timers offer both 16-bit and split 8-bit timer functionality with auto-reload and capture capabilities.

Timer 0 and Timer 1 include the following features:

- Standard 8051 timers, supporting backwards-compatibility with firmware and hardware.
- Clock sources include SYSCLK, SYSCLK divided by 12, 4, or 48, the External Clock divided by 8, or an external pin.
- · 8-bit auto-reload counter/timer mode
- 13-bit counter/timer mode
- 16-bit counter/timer mode
- Dual 8-bit counter/timer mode (Timer 0)

Timer 2, Timer 3, Timer 4, and Timer 5 are 16-bit timers including the following features:

- · Clock sources for all timers include SYSCLK, SYSCLK divided by 12, or the External Clock divided by 8
- · LFOSC0 divided by 8 may be used to clock Timer 3 and Timer 4 in active or suspend/snooze power modes
- Timer 4 is a low-power wake source, and can be chained together with Timer 3
- 16-bit auto-reload timer mode
- Dual 8-bit auto-reload timer mode
- · External pin capture
- · LFOSC0 capture
- Comparator 0 capture
- Configurable Logic output capture

### Watchdog Timer (WDT0)

The device includes a programmable watchdog timer (WDT) running off the low-frequency oscillator. A WDT overflow forces the MCU into the reset state. To prevent the reset, the WDT must be restarted by application software before overflow. If the system experiences a software or hardware malfunction preventing the software from restarting the WDT, the WDT overflows and causes a reset. Following a reset, the WDT is automatically enabled and running with the default maximum time interval. If needed, the WDT can be disabled by system software or locked on to prevent accidental disabling. Once locked, the WDT cannot be disabled until the next system reset. The state of the RST pin is unaffected by this reset.

The Watchdog Timer has the following features:

- · Programmable timeout interval
- · Runs from the low-frequency oscillator
- · Lock-out feature to prevent any modification until a system reset

#### 3.6 Communications and Other Digital Peripherals

#### Universal Asynchronous Receiver/Transmitter (UART0)

UART0 is an asynchronous, full duplex serial port offering modes 1 and 3 of the standard 8051 UART. Enhanced baud rate support allows a wide range of clock sources to generate standard baud rates. Received data buffering allows UART0 to start reception of a second incoming data byte before software has finished reading the previous data byte.

The UART module provides the following features:

- · Asynchronous transmissions and receptions
- Baud rates up to SYSCLK/2 (transmit) or SYSCLK/8 (receive)
- 8- or 9-bit data
- · Automatic start and stop generation
- · Single-byte buffer on transmit and receive

#### Universal Asynchronous Receiver/Transmitter (UART1)

UART1 is an asynchronous, full duplex serial port offering a variety of data formatting options. A dedicated baud rate generator with a 16-bit timer and selectable prescaler is included, which can generate a wide range of baud rates. A received data FIFO allows UART1 to receive multiple bytes before data is lost and an overflow occurs.

UART1 provides the following features:

- · Asynchronous transmissions and receptions
- Dedicated baud rate generator supports baud rates up to SYSCLK/2 (transmit) or SYSCLK/8 (receive)
- 5, 6, 7, 8, or 9 bit data
- Automatic start and stop generation
- Automatic parity generation and checking
- · Single-byte buffer on transmit and receive
- Auto-baud detection
- · LIN break and sync field detection
- CTS / RTS hardware flow control

#### Serial Peripheral Interface (SPI0)

The serial peripheral interface (SPI) module provides access to a flexible, full-duplex synchronous serial bus. The SPI can operate as a master or slave device in both 3-wire or 4-wire modes, and supports multiple masters and slaves on a single SPI bus. The slave-select (NSS) signal can be configured as an input to select the SPI in slave mode, or to disable master mode operation in a multi-master environment, avoiding contention on the SPI bus when more than one master attempts simultaneous data transfers. NSS can also be configured as a firmware-controlled chip-select output in master mode, or disable to reduce the number of pins required. Additional general purpose port I/O pins can be used to select multiple slave devices in master mode.

- Supports 3- or 4-wire master or slave modes
- · Supports external clock frequencies up to 12 Mbps in master or slave mode
- · Support for all clock phase and polarity modes
- 8-bit programmable clock rate (master)
- Programmable receive timeout (slave)
- Two byte FIFO on transmit and receive
- · Can operate in suspend or snooze modes and wake the CPU on reception of a byte
- · Support for multiple masters on the same data lines

#### System Management Bus / I2C (SMB0)

The SMBus I/O interface is a two-wire, bi-directional serial bus. The SMBus is compliant with the System Management Bus Specification, version 1.1, and compatible with the I<sup>2</sup>C serial bus.

The SMBus module includes the following features:

- · Standard (up to 100 kbps) and Fast (400 kbps) transfer speeds
- · Support for master, slave, and multi-master modes
- Hardware synchronization and arbitration for multi-master mode
- · Clock low extending (clock stretching) to interface with faster masters
- · Hardware support for 7-bit slave and general call address recognition
- Firmware support for 10-bit slave address decoding
- · Ability to inhibit all slave states
- Programmable data setup/hold times
- Transmit and receive buffers to help increase throughput in faster applications

#### I2C Slave (I2CSLAVE0)

The I2C Slave interface is a 2-wire, bidirectional serial bus that is compatible with the I2C Bus Specification 3.0. It is capable of transferring in high-speed mode (HS-mode) at speeds of up to 3.4 Mbps. Firmware can write to the I2C interface, and the I2C interface can autonomously control the serial transfer of data. The interface also supports clock stretching for cases where the core may be temporarily prohibited from transmitting a byte or processing a received byte during an I2C transaction. This module operates only as an I2C slave device.

The I2C module includes the following features:

- Standard (up to 100 kbps), Fast (400 kbps), Fast Plus (1 Mbps), and High-speed (3.4 Mbps) transfer speeds
- · Support for slave mode only
- · Clock low extending (clock stretching) to interface with faster masters
- · Hardware support for 7-bit slave address recognition
- · Hardware support for multiple slave addresses with the option to save the matching address in the receive FIFO

#### 16-bit CRC (CRC0)

The cyclic redundancy check (CRC) module performs a CRC using a 16-bit polynomial. CRC0 accepts a stream of 8-bit data and posts the 16-bit result to an internal register. In addition to using the CRC block for data manipulation, hardware can automatically CRC the flash contents of the device.

The CRC module is designed to provide hardware calculations for flash memory verification and communications protocols. The CRC module supports the standard CCITT-16 16-bit polynomial (0x1021), and includes the following features:

- Support for CCITT-16 polynomial
- · Byte-level bit reversal
- · Automatic CRC of flash contents on one or more 256-byte blocks
- · Initial seed selection of 0x0000 or 0xFFFF

#### Configurable Logic Units (CLU0, CLU1, CLU2, and CLU3)

The Configurable Logic block consists of multiple Configurable Logic Units (CLUs). CLUs are flexible logic functions which may be used for a variety of digital functions, such as replacing system glue logic, aiding in the generation of special waveforms, or synchronizing system event triggers.

- · Four configurable logic units (CLUs), with direct-pin and internal logic connections
- Each unit supports 256 different combinatorial logic functions (AND, OR, XOR, muxing, etc.) and includes a clocked flip-flop for synchronous operations
- · Units may be operated synchronously or asynchronously
- May be cascaded together to perform more complicated logic functions
- · Can operate in conjunction with serial peripherals such as UART and SPI or timing peripherals such as timers and PCA channels
- · Can be used to synchronize and trigger multiple on-chip resources (ADC, DAC, Timers, etc.)
- · Asynchronous output may be used to wake from low-power states

## 3.7 Analog

## 14/12/10-Bit Analog-to-Digital Converter (ADC0)

The ADC is a successive-approximation-register (SAR) ADC with 14-, 12-, and 10-bit modes, integrated track-and hold and a programmable window detector. The ADC is fully configurable under software control via several registers. The ADC may be configured to measure different signals using the analog multiplexer. The voltage reference for the ADC is selectable between internal and external reference sources.

- Up to 20 external inputs
- Single-ended 14-bit, 12-bit and 10-bit modes
- Supports an output update rate of up to 1 Msps in 12-bit mode
- · Channel sequencer logic with direct-to-XDATA output transfers
- Operation in a low power mode at lower conversion speeds
- Asynchronous hardware conversion trigger, selectable between software, external I/O and internal timer and configurable logic sources
- Output data window comparator allows automatic range checking
- Support for output data accumulation
- Conversion complete and window compare interrupts supported
- Flexible output data formatting
- Includes a fully-internal fast-settling 1.65 V reference and an on-chip precision 2.4 / 1.2 V reference, with support for using the supply as the reference, an external reference and signal ground
- Integrated factory-calibrated temperature sensor

# 12-Bit Digital-to-Analog Converters (DAC0, DAC1, DAC2, DAC3)

The DAC modules are 12-bit Digital-to-Analog Converters with the capability to synchronize multiple outputs together. The DACs are fully configurable under software control. The voltage reference for the DACs is selectable between internal and external reference sources.

- Voltage output with 12-bit performance
- · Hardware conversion trigger, selectable between software, external I/O and internal timer and configurable logic sources
- · Outputs may be configured to persist through reset and maintain output state to avoid system disruption
- Multiple DAC outputs can be synchronized together
- DAC pairs (DAC0 and 1 or DAC2 and 3) support complementary output waveform generation
- · Outputs may be switched between two levels according to state of configurable logic / PWM input trigger
- Flexible input data formatting
- · Supports references from internal supply, on-chip precision reference, or external VREF pin

## Low Current Comparators (CMP0, CMP1)

An analog comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. External input connections to device I/O pins and internal connections are available through separate multiplexers on the positive and negative inputs. Hysteresis, response time, and current consumption may be programmed to suit the specific needs of the application.

The comparator includes the following features:

- · Up to 10 (CMP0) or 9 (CMP1) external positive inputs
- · Up to 10 (CMP0) or 9 (CMP1) external negative inputs
- · Additional input options:
  - Internal connection to LDO output
  - Direct connection to GND
  - Direct connection to VDD
  - Dedicated 6-bit reference DAC
- Synchronous and asynchronous outputs can be routed to pins via crossbar
- Programmable hysteresis between 0 and ±20 mV
- Programmable response time
- Interrupts generated on rising, falling, or both edges
- PWM output kill feature

#### 3.8 Reset Sources

Reset circuitry allows the controller to be easily placed in a predefined default condition. On entry to this reset state, the following occur:

- The core halts program execution.
- · Module registers are initialized to their defined reset values unless the bits reset only with a power-on reset.
- · External port pins are forced to a known state.
- · Interrupts and timers are disabled.

All registers are reset to the predefined values noted in the register descriptions unless the bits only reset with a power-on reset. The contents of RAM are unaffected during a reset; any previously stored data is preserved as long as power is not lost. By default, the Port I/O latches are reset to 1 in open-drain mode, with weak pullups enabled during and after the reset. Optionally, firmware may configure the port I/O, DAC outputs, and precision reference to maintain state through system resets other than power-on resets. For Supply Monitor and power-on resets, the RSTb pin is driven low until the device exits the reset state. On exit from the reset state, the program counter (PC) is reset, and the system clock defaults to an internal oscillator. The Watchdog Timer is enabled, and program execution begins at location 0x0000.

Reset sources on the device include the following:

- Power-on reset
- External reset pin
- Comparator reset
- · Software-triggered reset
- Supply monitor reset (monitors VDD supply)
- · Watchdog timer reset
- · Missing clock detector reset
- · Flash error reset

### 3.9 Debugging

The EFM8LB1 devices include an on-chip Silicon Labs 2-Wire (C2) debug interface to allow flash programming and in-system debugging with the production part installed in the end application. The C2 interface uses a clock signal (C2CK) and a bi-directional C2 data signal (C2D) to transfer information between the device and a host system. See the C2 Interface Specification for details on the C2 protocol.

## 4.1.6 Internal Oscillators

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit			
High Frequency Oscillator 0 (24.5 MHz)									
Oscillator Frequency	f <sub>HFOSC0</sub>	Full Temperature and Supply Range	24	24.5	25	MHz			
Power Supply Sensitivity	PSS <sub>HFOS</sub> C0	T <sub>A</sub> = 25 °C	_	0.5	_	%/V			
Temperature Sensitivity	TS <sub>HFOSC0</sub>	V <sub>DD</sub> = 3.0 V	_	40	_	ppm/°C			
High Frequency Oscillator 1 (72 MHz)									
Oscillator Frequency	f <sub>HFOSC1</sub>	Full Temperature and Supply Range	70.5	72	73.5	MHz			
Power Supply Sensitivity	PSS <sub>HFOS</sub> C1	T <sub>A</sub> = 25 °C	_	TBD	_	%/V			
Temperature Sensitivity	TS <sub>HFOSC1</sub>	V <sub>DD</sub> = 3.0 V	_	TBD		ppm/°C			
Low Frequency Oscillator (80 kHz)									
Oscillator Frequency	f <sub>LFOSC</sub>	Full Temperature and Supply Range	75	80	85	kHz			
Power Supply Sensitivity	PSS <sub>LFOSC</sub>	T <sub>A</sub> = 25 °C	—	0.05	_	%/V			
Temperature Sensitivity	TS <sub>LFOSC</sub>	V <sub>DD</sub> = 3.0 V	—	65	_	ppm/°C			

### Table 4.6. Internal Oscillators

## 4.1.7 External Clock Input

## Table 4.7. External Clock Input

Parameter	Symbol	Test Condition	Min	Тур	Мах	Unit
External Input CMOS Clock	f <sub>CMOS</sub>		0	—	50	MHz
Frequency (at EXTCLK pin)						
External Input CMOS Clock High Time	t <sub>СМОЅН</sub>		9	—	—	ns
External Input CMOS Clock Low Time	t <sub>CMOSL</sub>		9	_	_	ns

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit				
Power Supply Rejection Ratio	PSRR <sub>ADC</sub>		—	TBD	_	dB				
DC Performance	DC Performance									
Integral Nonlinearity	INL	14 Bit Mode	_	TBD	_	LSB				
		12 Bit Mode	-1.4	TBD	+1.4	LSB				
		10 Bit Mode		TBD		LSB				
Differential Nonlinearity (Guaran-	DNL	14 Bit Mode	_	TBD	_	LSB				
teed Monotonic)		12 Bit Mode	_	TBD	0.9	LSB				
		10 Bit Mode	_	TBD		LSB				
Offset Error	E <sub>OFF</sub>	14 Bit Mode	_	TBD	_	LSB				
		12 Bit Mode	-2	TBD	2	LSB				
		10 Bit Mode	_	TBD	_	LSB				
Offset Temperature Coefficient	TC <sub>OFF</sub>		_	TBD	_	LSB/°C				
Slope Error	E <sub>M</sub>	14 Bit Mode		TBD		%				
		12 Bit Mode	_	TBD	TBD	%				
		10 Bit Mode	_	TBD		%				
Dynamic Performance 10 kHz Sine	Wave Input	1 dB below full scale, Max throughput	, using AGN	D pin						
Signal-to-Noise	SNR	14 Bit Mode	_	TBD	_	dB				
		12 Bit Mode	TBD	TBD	—	dB				
		10 Bit Mode	_	TBD	_	dB				
Signal-to-Noise Plus Distortion	SNDR	14 Bit Mode	—	TBD	—	dB				
		12 Bit Mode	TBD	TBD	_	dB				
		10 Bit Mode	_	TBD	—	dB				
Total Harmonic Distortion (Up to	THD	14 Bit Mode	_	TBD	—	dB				
5th Harmonic)		12 Bit Mode	—	TBD	_	dB				
		10 Bit Mode	_	TBD	_	dB				
Spurious-Free Dynamic Range	SFDR	14 Bit Mode	_	TBD	_	dB				
		12 Bit Mode		TBD		dB				
		10 Bit Mode		TBD		dB				

## Note:

1. This time is equivalent to four periods of a clock running at 18 MHz + 2%.

2. Conversion Time does not include Tracking Time. Total Conversion Time is:

Total Conversion Time = [RPT × (ADTK + NUMBITS + 1) × T(SARCLK)] + (T(ADCCLK) × 4)

where RPT is the number of conversions represented by the ADRPT field and ADCCLK is the clock selected for the ADC. 3. Absolute input pin voltage is limited by the  $V_{IO}$  supply.

#### 4.1.11 Temperature Sensor

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Uncalibrated Offset	V <sub>OFF</sub>	T <sub>A</sub> = 0 °C	_	TBD	_	mV
Uncalibrated Offset Error <sup>1</sup>	E <sub>OFF</sub>	T <sub>A</sub> = 0 °C	_	TBD	_	mV
Slope	М		—	2.83	—	mV/°C
Slope Error <sup>1</sup>	E <sub>M</sub>		_	TBD	_	μV/°C
Linearity			_	TBD	_	°C
Turn-on Time			—	TBD	—	μs
Temp Sensor Error Using Typical		T = 0 °C to 70 °C	TBD		TBD	°C
set <sup>2, 3</sup>		T = -20 °C to 85 °C	-3	—	3	°C
		T = -40 °C to 105 °C	TBD		TBD	°C

### Table 4.11. Temperature Sensor

### Note:

1. Represents one standard deviation from the mean.

2. The factory-calibrated offset value is stored in the read-only area of flash in locations 0xFFD4 (low byte) and 0xFFD5 (high byte). The 14-bit result represents the output of the ADC when sampling the temp sensor using the 1.65 V internal voltage reference.

3. Temp sensor error is based upon characterization and is not tested across temperature in production. The values represent three standard deviations above and below the mean.

## 4.1.15 Port I/O

## Table 4.15. Port I/O

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Output High Voltage (High Drive)	V <sub>OH</sub>	$I_{OH}$ = -7 mA, $V_{IO} \ge 3.0$ V	V <sub>IO</sub> - 0.7	—	—	V
		$I_{OH}$ = -3.3 mA, 2.2 V ≤ $V_{IO}$ < 3.0 V	V <sub>IO</sub> x 0.8	—	—	V
		$I_{OH}$ = -1.8 mA, 1.71 V $\leq$ V <sub>IO</sub> < 2.2 V				
Output Low Voltage (High Drive)	V <sub>OL</sub>	I <sub>OL</sub> = 13.5 mA, V <sub>IO</sub> ≥ 3.0 V	_	—	0.6	V
		$I_{OL}$ = 7 mA, 2.2 V ≤ $V_{IO}$ < 3.0 V	_	_	V <sub>IO</sub> x 0.2	V
		$I_{OL}$ = 3.6 mA, 1.71 V $\leq$ V <sub>IO</sub> < 2.2 V				
Output High Voltage (Low Drive)	V <sub>OH</sub>	I <sub>OH</sub> = -4.75 mA, V <sub>IO</sub> ≥ 3.0 V	V <sub>IO</sub> - 0.7	_	—	V
		$I_{OH}$ = -2.25 mA, 2.2 V ≤ V <sub>IO</sub> < 3.0 V	V <sub>IO</sub> x 0.8	—	—	V
		$I_{OH}$ = -1.2 mA, 1.71 V $\leq$ V <sub>IO</sub> < 2.2 V				
Output Low Voltage (Low Drive)	V <sub>OL</sub>	I <sub>OL</sub> = 6.5 mA, V <sub>IO</sub> ≥ 3.0 V	_	_	0.6	V
		$I_{OL}$ = 3.5 mA, 2.2 V ≤ $V_{IO}$ < 3.0 V	—	—	V <sub>IO</sub> x 0.2	V
		$I_{OL}$ = 1.8 mA, 1.71 V $\leq$ V <sub>IO</sub> < 2.2 V				
Input High Voltage	VIH		0.7 x	_	—	V
			V <sub>IO</sub>			
Input Low Voltage	VIL				0.3 x	V
					V <sub>IO</sub>	
Pin Capacitance	C <sub>IO</sub>		—	7	—	pF
Weak Pull-Up Current	I <sub>PU</sub>	V <sub>DD</sub> = 3.6	-30	-20	-10	μA
(V <sub>IN</sub> = 0 V)						
Input Leakage (Pullups off or Ana- log)	I <sub>LK</sub>	$GND < V_{IN} < V_{IO}$	TBD	—	TBD	μA
Input Leakage Current with VIN	I <sub>LK</sub>	V <sub>IO</sub> < V <sub>IN</sub> < V <sub>IO</sub> +2.5 V	0	5	150	μA
anove AIO		Any pin except P3.0, P3.1, P3.2, or P3.3				

# 5. Typical Connection Diagrams

### 5.1 Power

Figure 5.1 Power Connection Diagram on page 28 shows a typical connection diagram for the power pins of the device.



Figure 5.1. Power Connection Diagram

Pin	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
Number					
6	P3.7 /	Multifunction I/O /			
	C2D	C2 Debug Data			
7	P3.3	Multifunction I/O			DAC3
8	P3.2	Multifunction I/O			DAC2
9	P3.1	Multifunction I/O			DAC1
10	P3.0	Multifunction I/O			DAC0
11	P2.6	Multifunction I/O			ADC0.19
					CMP1P.8
					CMP1N.8
12	P2.5	Multifunction I/O		CLU3OUT	ADC0.18
					CMP1P.7
					CMP1N.7
13	P2.4	Multifunction I/O			ADC0.17
					CMP1P.6
					CMP1N.6
14	P2.3	Multifunction I/O	Yes	P2MAT.3	ADC0.16
				CLU1B.15	CMP1P.5
				CLU2B.15	CMP1N.5
				CLU3A.15	
15	P2.2	Multifunction I/O	Yes	P2MAT.2	ADC0.15
				CLU2OUT	CMP1P.4
				CLU1A.15	CMP1N.4
				CLU2B.14	
				CLU3A.14	
16	P2.1	Multifunction I/O	Yes	P2MAT.1	ADC0.14
				I2C0_SCL	CMP1P.3
				CLU1B.14	CMP1N.3
				CLU2A.15	
				CLU3B.15	
17	P2.0	Multifunction I/O	Yes	P2MAT.0	CMP1P.2
				I2C0_SDA	CMP1N.2
				CLU1A.14	
				CLU2A.14	
				CLU3B.14	

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
18	P1.7	Multifunction I/O	Yes	P1MAT.7	ADC0.13
				CLU0B.15	CMP0P.9
				CLU1B.13	CMP0N.9
				CLU2A.13	
19	P1.6	Multifunction I/O	Yes	P1MAT.6	ADC0.12
				CLU0A.15	
				CLU1B.12	
				CLU2A.12	
20	P1.5	Multifunction I/O	Yes	P1MAT.5	ADC0.11
				CLU0B.14	
				CLU1A.13	
				CLU2B.13	
				CLU3B.11	
21	P1.4	Multifunction I/O	Yes	P1MAT.4	ADC0.10
				CLU0A.14	
				CLU1A.12	
				CLU2B.12	
				CLU3B.10	
22	P1.3	Multifunction I/O	Yes	P1MAT.3	ADC0.9
				CLU0B.13	
				CLU1B.11	
				CLU2B.11	
				CLU3A.13	
23	P1.2	Multifunction I/O	Yes	P1MAT.2	ADC0.8
				CLU0A.13	CMP0P.8
				CLU1A.11	CMP0N.8
				CLU2B.10	
				CLU3A.12	
				CLU3B.13	
24	P1.1	Multifunction I/O	Yes	P1MAT.1	ADC0.7
				CLU0B.12	CMP0P.7
				CLU1B.10	CMP0N.7
				CLU2A.11	
				CLU3B.12	

Pin	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
2	P0.0	Multifunction I/O	Vos		
2	1 0.0		163		
				CLUUA.8	
				CLUZA.8	
-		Oneveral		CLU3B.8	
3		Ground			
4		Supply Power Input			
5	RSID/	Active-low Reset /			
	C2CK	C2 Debug Clock			
6	P3.0 /	Multifunction I/O /			
	C2D	C2 Debug Data			
7	P2.3	Multifunction I/O	Yes	P2MAT.3	DAC3
				CLU1B.15	
				CLU2B.15	
				CLU3A.15	
8	P2.2	Multifunction I/O	Yes	P2MAT.2	DAC2
				CLU1A.15	
				CLU2B.14	
				CLU3A.14	
9	P2.1	Multifunction I/O	Yes	P2MAT.1	DAC1
				CLU1B.14	
				CLU2A.15	
				CLU3B.15	
10	P2.0	Multifunction I/O	Yes	P2MAT.0	DAC0
				CLU1A.14	
				CLU2A.14	
				CLU3B.14	
11	P1.6	Multifunction I/O	Yes	P1MAT.6	ADC0.11
				CLU3OUT	CMP1P.5
				CLU0A.15	CMP1N.5
				CLU1B.12	
				CLU2A.12	





Pin	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
Number					
1	P0.3	Multifunction I/O	Yes	P0MAT.3	XTAL2
				EXTCLK	
				INT0.3	
				INT1.3	
				CLU0B.9	
				CLU2B.10	
				CLU3A.9	

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
2	P0.2	Multifunction I/O	Yes	P0MAT.2	XTAL1
				INT0.2	ADC0.1
				INT1.2	CMP0P.1
				CLU0OUT	CMP0N.1
				CLU0A.9	
				CLU2B.8	
				CLU3A.8	
3	P0.1	Multifunction I/O	Yes	P0MAT.1	ADC0.0
				INT0.1	CMP0P.0
				INT1.1	CMP0N.0
				CLU0B.8	AGND
				CLU2A.9	
				CLU3B.9	
4	P0.0	Multifunction I/O	Yes	P0MAT.0	VREF
				INT0.0	
				INT1.0	
				CLU0A.8	
				CLU2A.8	
				CLU3B.8	
5	GND	Ground			
6	VDD / VIO	Supply Power Input			
7	RSTb /	Active-low Reset /			
	C2CK	C2 Debug Clock			
8	P3.0 /	Multifunction I/O /			
	C2D	C2 Debug Data			
9	P2.3	Multifunction I/O	Yes	P2MAT.3	DAC3
				CLU1B.15	
				CLU2B.15	
				CLU3A.15	
10	P2.2	Multifunction I/O	Yes	P2MAT.2	DAC2
				CLU1A.15	
				CLU2B.14	
				CLU3A.14	

Pin	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
Number	D2.4	Multifunction 1/0	Vec		DAC1
	P2.1	Multifunction I/O	res		DACT
				CLU2A.15	
10	<b>D</b> 2 0	Multifunction I/O	Vaa		DACO
12	P2.0		res		DACU
				CLU2A.14	
12	D1 7	Multifunction I/O	Vaa	CLU3B.14	ADC0 12
13	P1.7		res		
				CLUUB. 13	
				CLUIB. 13	CMP IN.6
14	D1 6	Multifunction I/O	Vaa	CLUZA. 13	ADC0 11
14	P1.0		res		
				CLU3OUT	CMP1P.5
				CLUUA.15	CMP1N.5
				CLU1B.12	
	<b>D</b> 4.5			CLU2A.12	
15	P1.5	Multifunction I/O	Yes	P1MA1.5	ADC0.10
				CLU2OUT	CMP1P.4
				CLU0B.14	CMP1N.4
				CLU1A.13	
				CLU2B.13	
				CLU3B.11	
16	P1.4	Multifunction I/O	Yes	P1MAT.4	ADC0.9
				I2C0_SCL	CMP1P.3
				CLU0A.14	CMP1N.3
				CLU1A.12	
				CLU2B.12	
				CLU3B.10	
17	P1.3	Multifunction I/O	Yes	P1MAT.3	CMP1P.2
				I2C0_SDA	CMP1N.2
				CLU0B.13	
				CLU1B.11	
				CLU2B.11	
				CLU3A.13	

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
18	P1.2	Multifunction I/O	Yes	P1MAT.2	ADC0.8
				CLU0A.13	
				CLU1A.11	
				CLU2B.10	
				CLU3A.12	
				CLU3B.13	
19	P1.1	Multifunction I/O	Yes	P1MAT.1	ADC0.7
				CLU0B.12	
				CLU1B.10	
				CLU2A.11	
				CLU3B.12	
20	P1.0	Multifunction I/O	Yes	P1MAT.0	ADC0.6
				CLU0A.12	
				CLU1A.10	
				CLU2A.10	
21	P0.7	Multifunction I/O	Yes	P0MAT.7	ADC0.5
				INT0.7	CMP0P.5
				INT1.7	CMP0N.5
				CLU1OUT	CMP1P.1
				CLU0B.11	CMP1N.1
				CLU1B.9	
				CLU3A.11	
22	P0.6	Multifunction I/O	Yes	P0MAT.6	ADC0.4
				CNVSTR	CMP0P.4
				INT0.6	CMP0N.4
				INT1.6	CMP1P.0
				CLU0A.11	CMP1N.0
				CLU1B.8	
				CLU3A.10	
23	P0.5	Multifunction I/O	Yes	P0MAT.5	ADC0.3
				INT0.5	CMP0P.3
				INT1.5	CMP0N.3
				UART0_RX	
				CLU0B.10	
				CLU1A.9	





The package marking consists of:

- PPPPPPP The part number designation.
- TTTTTT A trace or manufacturing code.
- YY The last 2 digits of the assembly year.
- WW The 2-digit workweek when the device was assembled.
- # The device revision (A, B, etc.).

Dimension	Min	Тур	Мах
ааа		0.20	
bbb		0.18	
ссс		0.10	
ddd		0.10	
ccc ddd		0.10	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.

2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

3. This drawing conforms to JEDEC outline MO-137, variation AE.

4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

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