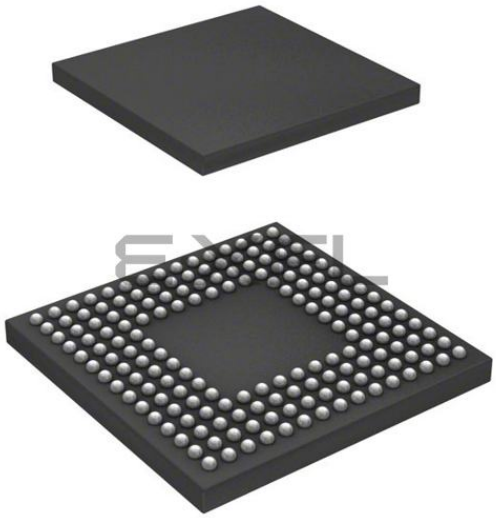

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	H8S/2600
Core Size	16-Bit
Speed	20MHz
Connectivity	FIFO, I²C, LPC, SCI, SmartCard
Peripherals	POR, PWM, WDT
Number of I/O	128
Program Memory Size	160KB (160K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	External
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LFBGA
Supplier Device Package	176-LFBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2117vbg20ihv

5.6 Interrupt Control Modes and Interrupt Operation

The interrupt controller has two modes: interrupt control mode 0 and interrupt control mode 1. Interrupt operations differ depending on the interrupt control mode. NMI and address break interrupts are always accepted except for in the reset state. The interrupt control mode is selected by SYSCR. Table 5.7 shows the interrupt control modes.

Table 5.7 Interrupt Control Modes

Interrupt Control Mode	SYSCR		Priority Setting Registers	Interrupt Mask Bits	Description
	INTM1	INTM0			
0	0	0	ICR	I	Interrupt mask control is performed by the I bit. Priority levels can be set with ICR.
1	0	1	ICR	I, UI	3-level interrupt mask control is performed by the I and UI bits. Priority levels can be set with ICR.

Figure 5.6 shows a block diagram of the priority determination circuit.

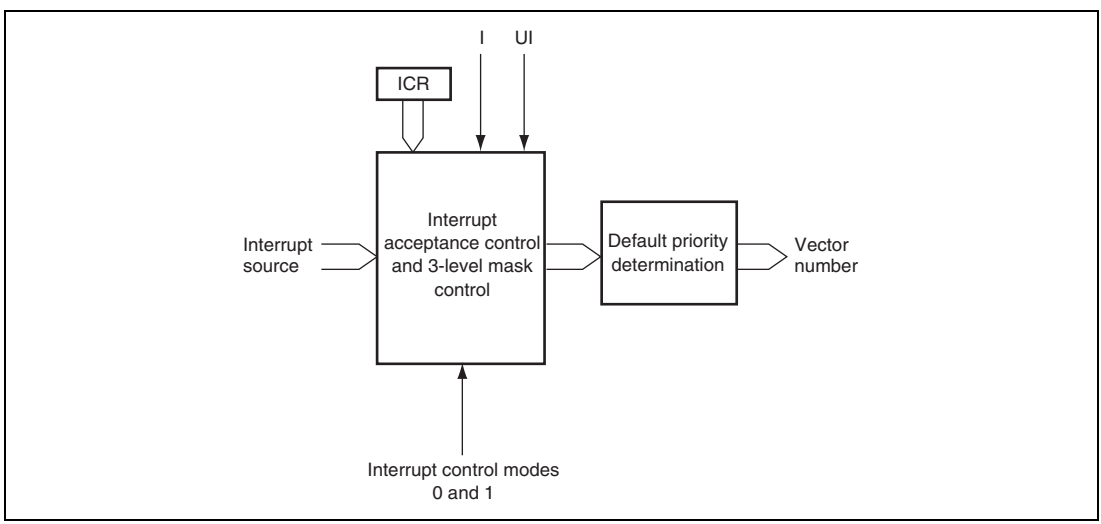

Figure 5.6 Block Diagram of Interrupt Control Operation

(2) PE0/ExEXCL

The pin function is switched as shown below according to the combination of the EXCLS bit in PTCNT0 and EXCLE bit in LPWRCR. When the EXCLS bit in PTCNT0 and EXCLE bit in LPWRCR are set to 1, this pin can be used as the ExEXCL input pin.

		Setting
		I/O Port
Module Name	Pin Function	ExEXCL
I/O port	PE0 input (initial setting)	0

7.2.15 Port F

(1) PF7/PWMU5, APF6/PWMU4A, PF5/PWMU3A, PF4/PWMU2A

The pin function is switched as shown below according to the combination of the register setting of the PWMU and the PFnDDR bit.

		Setting	
		PWMU	I/O Port
Module Name	Pin Function	PWMUmA_OE	PFnDDR
PWMU	PWMUmA output	1	1
I/O port	PFn output	0	1
	PFn input (initial setting)	—	0

(n = 5 to 2, m = 7 to 4)

Bit	Bit Name	Initial Value	R/W	Description
4	PWM4E	0	R/W	PWMU4 Output Enable • 8-bit single-pulse/pulse-division mode 0: PWMU4 output and counter operation are disabled. 1: PWMU4 output and counter operation are enabled. • 16-bit single-pulse mode 0: PWMU4 output and counter operation are disabled. 1: PWMU4 output and counter operation are enabled.
3	PWM3E	0	R/W	PWMU3 Output Enable 0: PWMU3 output and counter operation are disabled. 1: PWMU3 output and counter operation are enabled.
2	PWM2E	0	R/W	PWMU2 Output Enable • 8-bit single-pulse/pulse division mode 0: PWMU2 output and counter operation are disabled. 1: PWMU2 output and counter operation are enabled. • 16-bit single-pulse mode 0: PWMU2 output and counter operation are disabled. 1: PWMU2 output and counter operation are enabled.
1	PWM1E	0	R/W	PWMU1 Output Enable 0: PWMU1 output and counter operation are disabled. 1: PWMU1 output and counter operation are enabled.

Table 10.8 TPSC2 to TPSC0 (channel 2)

Channel	Bit 2 TPSC2	Bit 1 TPSC1	Bit 0 TPSC0	Description
2	0	0	0	Internal clock: counts on ϕ
			1	Internal clock: counts on $\phi/4$
		1	0	Internal clock: counts on $\phi/16$
			1	Internal clock: counts on $\phi/64$
	1	0	0	External clock: counts on TCLKA pin input
			1	External clock: counts on TCLKB pin input
		1	0	External clock: counts on TCLKC pin input
			1	Internal clock: counts on $\phi/1024$

Note: This setting is ignored when channel 2 is in phase counting mode.

(3) Determination of External Event (TDPCYI) Stoppage

Stoppage for an external event (TDPCYI) can be determined from the timer overflow flag. There are two types of such stoppage.

Stoppage for an external event can be considered to have occurred when the timer overflows within the period from the start of cycle measurement mode to the detection of the first edge (rising or falling, as selected by the POCTL bit in TDPCR1).

Figure 12.10 shows an example of the timing of this type of stoppage for an external event.

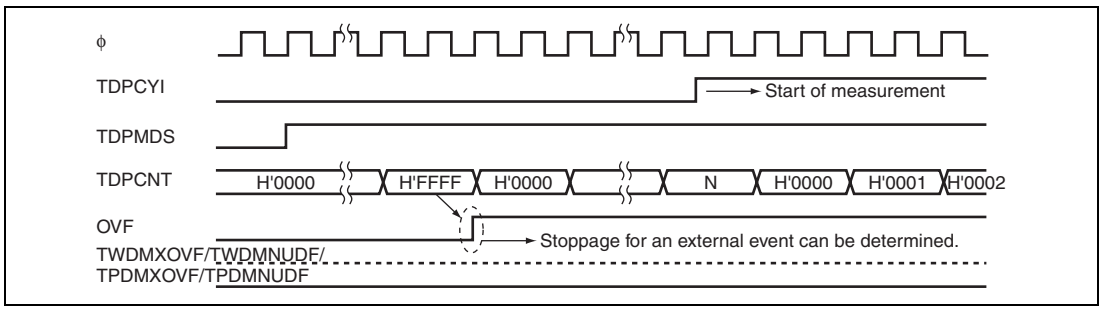

Figure 12.10 Example of Timing for Stoppage for an External Event (1)

When any of the TWDMXOVF, TWDMNUDF, TPDMXOVF, and TPDMNUDF flags is set to 1 while the CPSPE bit in TDPCR1 is 1, cycle measurement stops. Thereafter, when the corresponding flag is cleared, cycle measurement restarts. When the timer overflows before the first edge is detected after the restart of cycle measurement, it is possible to determine stoppage for an external event.

Figure 12.11 shows an example of the timing for this type of stoppage for an external event.

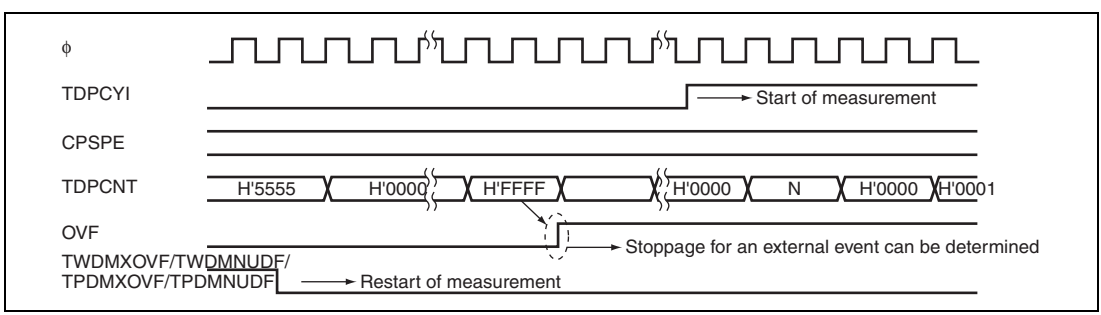

Figure 12.11 Example of Timing for Stoppage for an External Event (2)

13.3.8 Timer Connection Register I (TCONRI)

TCONRI controls the input capture function.

Bit	Bit Name	Initial Value	R/W	Description
7 to 5	—	All 0	R/W	Reserved The initial value should not be changed.
4	ICST	0	R/W	Input Capture Start Bit TMR_X has input capture registers (TICRR and TICRF). TICRR and TICRF can measure the width of a pulse by means of a single capture operation under the control of the ICST bit. When a rising edge followed by a falling edge is detected on TMRIX after the ICST bit is set to 1, the contents of TCNT at those points are captured into TICRR and TICRF, respectively, and the ICST bit is cleared to 0. [Clearing condition] When a rising edge followed by a falling edge is detected on TMRIX [Setting condition] When 1 is written in ICST after reading ICST = 0
3 to 0	—	All 0	R/W	Reserved The initial values should not be modified.

13.3.9 Timer Connection Register S (TCONRS)

TCONRS selects whether to access TMR_X or TMR_Y registers.

Bit	Bit Name	Initial Value	R/W	Description
7	TMRX/Y	0	R/W	TMR_X/TMR_Y Access Select For details, see table 13.4. 0: The TMR_X registers are accessed at addresses H'(FF)FFF0 to H'(FF)FFF5 1: The TMR_Y registers are accessed at addresses H'(FF)FFF0 to H'(FF)FFF5
6 to 0	—	All 0	R/W	Reserved The initial values should not be modified.

13.9 Usage Notes

13.9.1 Conflict between TCNT Write and Counter Clear

If a counter clear signal is generated during the T_2 state of a TCNT write cycle as shown in figure 13.13, clearing takes priority and the counter write is not performed.

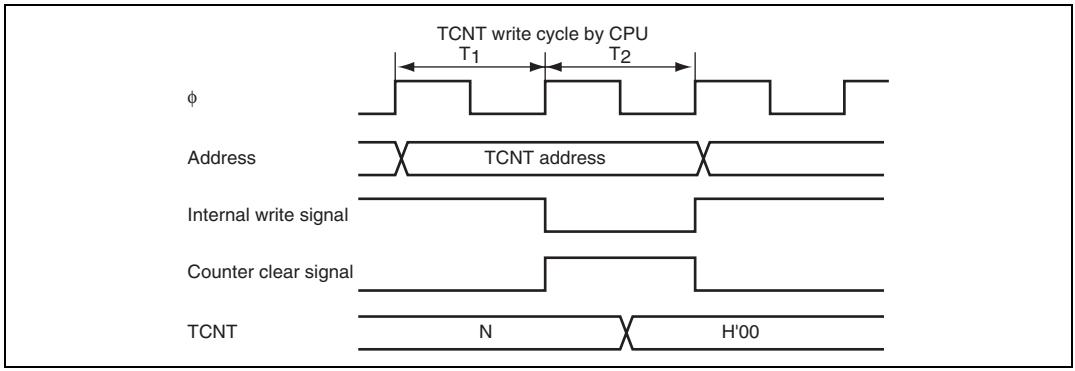

Figure 13.13 Conflict between TCNT Write and Clear

13.9.2 Conflict between TCNT Write and Count-Up

If a count-up occurs during the T_2 state of a TCNT write cycle as shown in figure 13.14, the counter write takes priority and the counter is not incremented.

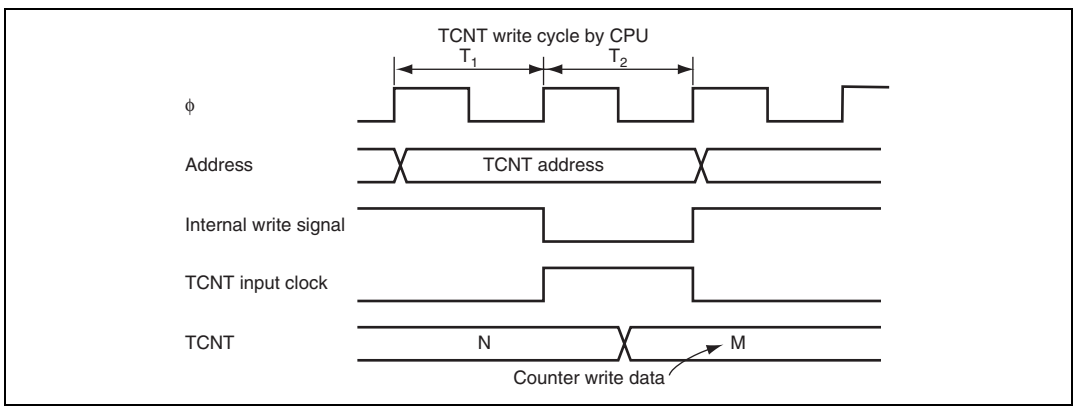

Figure 13.14 Conflict between TCNT Write and Count-Up

15.6 Operation in Clocked Synchronous Mode

Figure 15.14 shows the general format for clocked synchronous communication. In clocked synchronous mode, data is transmitted or received in synchronization with clock pulses. One character in transfer data consists of 8-bit data. In data transmission, the SCI outputs data from one falling edge of the synchronization clock to the next. In data reception, the SCI receives data in synchronization with the rising edge of the synchronization clock. After 8-bit data is output, the transmission line holds the MSB state. In clocked synchronous mode, no parity or multiprocessor bit is added. Inside the SCI, the transmitter and receiver are independent units, enabling full-duplex communication by use of a common clock. Both the transmitter and the receiver also have a double-buffered structure, so that the next transmit data can be written during transmission or the previous receive data can be read during reception, enabling continuous data transfer.

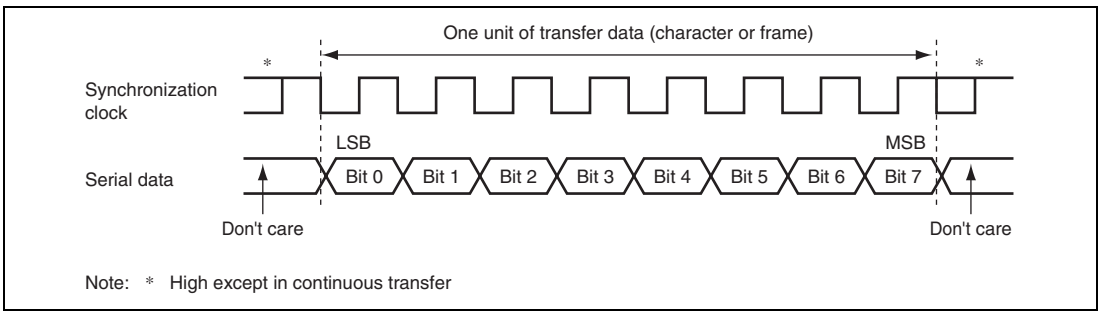

Figure 15.14 Data Format in Synchronous Communication (LSB-First)

15.6.1 Clock

Either an internal clock generated by the on-chip baud rate generator or an external synchronization clock input at the SCK pin can be selected, according to the setting of the CKE1 and CKE0 bits in SCR. When the SCI is operated on an internal clock, the synchronization clock is output from the SCK pin. Eight synchronization clock pulses are output in the transfer of one character, and when no transfer is performed the clock is fixed high.

15.7.7 Serial Data Reception (Except in Block Transfer Mode)

Data reception in smart card interface mode is identical to that in normal serial communication interface mode. Figure 15.29 shows the data re-transfer operation during reception.

1. If a parity error is detected in receive data, the PER bit in SSR is set to 1. Here, an ERI interrupt request is generated if the RIE bit in SCR is set to 1. Clear the PER bit to 0 before the next parity bit is sampled.
2. For the frame in which a parity error is detected, the RDRF bit in SSR is not set to 1.
3. If no parity error is detected, the PER bit in SSR is not set to 1. In this case, data is determined to have been received successfully, and the RDRF bit in SSR is set to 1. Here, an RXI interrupt request is generated if the RIE bit in SCR is set.

Figure 15.30 shows a sample flowchart for reception. In reception, setting the RIE bit to 1 allows an RXI interrupt request to be generated when the RDRF flag is set to 1. If an error occurs during reception, i.e., either the ORER or PER flag is set to 1, a transmit/receive error interrupt (ERI) request is generated and the error flag must be cleared. Even if a parity error occurs and PER is set to 1 in reception, receive data is transferred to RDR, thus allowing the data to be read.

Note: For operations in block transfer mode, see section 15.4, Operation in Asynchronous Mode.

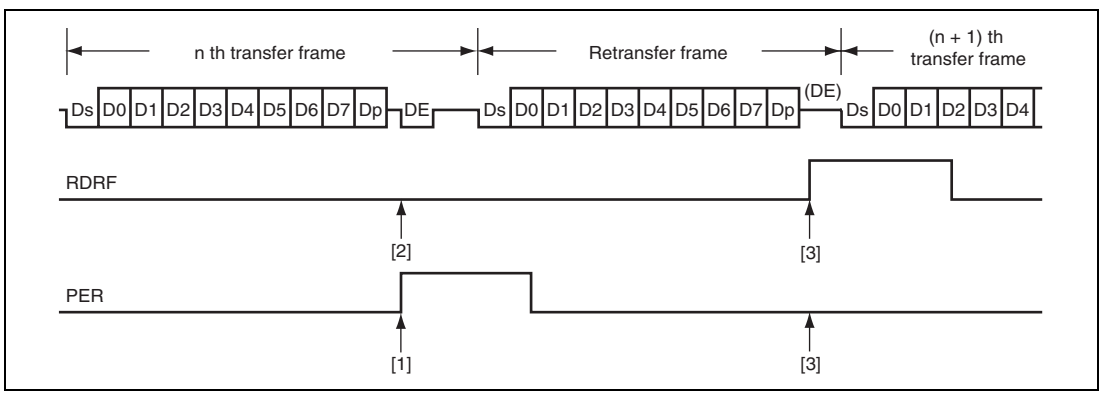

Figure 15.29 Data Re-transfer Operation in SCI Reception Mode

Table 16.8 shows the range of initialization of the registers related to data transmission/reception through the LPC interface, making a classification by each mode.

Table 16.8 Register States

Register		System Reset	SCIFRST	REGRST	LPC Reset	LPC Shutdown	LPC Abort
SCIFADRH	Bits 15 to 8	Initialized	Retained	Retained	Retained	Retained	Retained
SCIFADRL	Bits 7 to 0	Initialized	Retained	Retained	Retained	Retained	Retained
HICR5	SCIFE	Initialized	Retained	Retained	Retained	Retained	Retained
SIRQCR4	Bits 7 to 4, SCSIRQ3 to 0	Initialized	Retained	Retained	Retained	Retained	Retained
SCIFCR	SCIFOE1, SCIFOE0, OUT2LOOP, CKSEL1, CKSEL0, SCIFRST, REGRST	Initialized	Retained	Retained	Retained	Retained	Retained
FRBR	Bits 7 to 0	Initialized	Retained	Initialized	Initialized	Retained	Retained
FTHR	Bits 7 to 0	Initialized	Retained	Initialized	Initialized	Retained	Retained
FDLL	Bits 7 to 0	Initialized	Retained	Initialized	Initialized	Retained	Retained
FDLH	Bits 7 to 0	Initialized	Retained	Initialized	Initialized	Retained	Retained
FIIR	FIFOE1, FIFOE0, INTID2 to INTID0, INTPEND	Initialized	Retained	Initialized	Initialized	Retained	Retained
FFCR	RCVRTRIG1, RCVRTRIG0, XMITFRST, RCVRFRST, FIFOE	Initialized	Retained	Initialized	Initialized	Retained	Retained
FLCR	DLAB, TREAK, EPS, PEN, STOP, CLS1, CLS0	Initialized	Retained	Initialized	Initialized	Retained	Retained

6. Note on ICDR read in transmit mode and ICDR write in receive mode

   If ICDR is read in transmit mode (TRS = 1) or ICDR is written to in receive mode (TRS = 0), the SCL pin may not be held low in some cases after transmit/receive operation has been completed, thus inconveniently allowing clock pulses to be output on the SCL bus line before ICDR is accessed correctly. To access ICDR correctly, read ICDR after setting receive mode or write to ICDR after setting transmit mode.

7. Note on ACKE and TRS bits in slave mode

   In the I²C bus interface, if 1 is received as the acknowledge bit value (ACKB = 1) in transmit mode (TRS = 1) and then the address is received in slave mode without performing appropriate processing, interrupt handling may start at the rising edge of the 9th clock pulse even when the address does not match. Similarly, if the start condition or address is transmitted from the master device in slave transmit mode (TRS = 1), the IRIC flag may be set after the ICDRE flag is set and 1 received as the acknowledge bit value (ACKB = 1), thus causing an interrupt source even when the address does not match.

   To use the I²C bus interface module in slave mode, be sure to follow the procedures below.

   A. When having received 1 as the acknowledge bit value for the last transmit data at the end of a series of transmit operation, clear the ACKE bit in ICCR once to initialize the ACKB bit to 0.

   B. Set receive mode (TRS = 0) before the next start condition is input in slave mode. Complete transmit operation by the procedure shown in figure 17.16, in order to switch from slave transmit mode to slave receive mode.

17.6.1 Module Stop Mode Setting

The IIC operation can be enabled or disabled using the module stop control register. The initial setting is for the IIC operation to be halted. Register access is enabled by canceling module stop mode. For details, see section 24, Power-Down Modes.

- LADR2L

Bit	Bit Name	Initial Value	R/W Slave	R/W Host	Description
7	Bit 7	0	R/W	—	Channel 2 Address Bits 7 to 3
6	Bit 6	1	R/W	—	Set the LPC channel 2 host address.
5	Bit 5	1	R/W	—	
4	Bit 4	0	R/W	—	
3	Bit 3	0	R/W	—	
2	Bit 2	0	R/W	—	Reserved This bit is ignored when an address match is decided.
1	Bit 1	1	R/W	—	Channel 2 Address Bits 1 and 0
0	Bit 0	0	R/W	—	Set the LPC channel 2 host address.

- Host select register

I/O Address Bits 5 to 3	I/O Address Bit 2	I/O Address Bits 1 and 0	Transfer Cycle	Host Select Register
Bits 15 to 3 in LADR2	0	Bits 1 and 0 in LADR2	I/O write	IDR2 write (data)
Bits 15 to 3 in LADR2	1	Bits 1 and 0 in LADR2	I/O write	IDR2 write (command)
Bits 15 to 3 in LADR2	0	Bits 1 and 0 in LADR2	I/O read	ODR2 read
Bits 15 to 3 in LADR2	1	Bits 1 and 0 in LADR2	I/O read	STR2 read

Note: * When channel 2 is used, the content of LADR2 must be set so that the addresses for channels 1, 3, 4, and SCIF are different.

Bit	Bit Name	Initial Value	R/W Slave	R/W Host	Description
2	SMIE2	0	R/W	—	Host SMI Interrupt Enable 2 Enables or disables an SMI interrupt request when OBF2 is set by an ODR2 write. 0: Host SMI interrupt request by OBF2 and SMIE2 is disabled [Clearing conditions] • Writing 0 to SMIE2 • LPC hardware reset, LPC software reset • Clearing OBF2 to 0 (when IEDIR2 = 0) 1: [When IEDIR2 = 0] Host SMI interrupt request by setting OBF2 to 1 is enabled [When IEDIR2 = 1] Host SMI interrupt is requested [Setting condition] Writing 1 after reading SMIE2 = 0
1	IRQ12E1	0	R/W	—	Host IRQ12 Interrupt Enable 1 Enables or disables an HIRQ12 interrupt request when OBF1 is set by an ODR1 write. 0: HIRQ12 interrupt request by OBF1 and IRQ12E1 is disabled [Clearing conditions] • Writing 0 to IRQ12E1 • LPC hardware reset, LPC software reset • Clearing OBF1 to 0 1: HIRQ12 interrupt request by setting OBF1 to 1 is enabled [Setting condition] Writing 1 after reading IRQ12E1 = 0

Bit	Bit Name	Initial Value	R/W	Description
2	WD	—	R/W	Write Data Address Detect When an address not in the flash memory area is specified as the start address of the storage destination for the program data, an error occurs. 0: Setting of the start address of the storage destination for the program data is normal 1: Setting of the start address of the storage destination for the program data is abnormal
1	WA	—	R/W	Write Address Error Detect When the following items are specified as the start address of the programming destination, an error occurs. • An area other than flash memory • The specified address is not aligned with the 128-byte boundary (lower eight bits of the address are other than H'00 and H'80) 0: Setting of the start address of the programming destination is normal 1: Setting of the start address of the programming destination is abnormal
0	SF	—	R/W	Success/Fail Returns the programming result. 0: Programming has ended normally (no error) 1: Programming has ended abnormally (error occurs)

(3) Flash Program/Erase Frequency Parameter (FPEFEQ: General Register ER0 of CPU)

FPEFEQ sets the operating frequency of the CPU. The operating frequency available in this LSI ranges from 8 MHz to 20 MHz.

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	—	—	Unused These bits should be cleared to 0.
15 to 0	F15 to F0	—	R/W	Frequency Set These bits set the operating frequency of the CPU. The setting value must be calculated as follows: 1. Round off the operating frequency expressed in MHz unit at the third decimal place to make it into two decimal places. 2. Multiply the rounded number by 100 and convert the result into binary and write it to FPEFEQ (general register ER0). For example, when the operating frequency of the CPU is 20.000 MHz, the setting value is as follows: 1. Round 20.000 off at the third decimal place as 20.00. 2. Convert 20.00 × 100 = 2000 into a binary number and set B'0000 0111 1101 0000 (H'07D0) in ER0.

When the $\overline{\text{RES}}$ pin is driven low, the clock pulse generator starts oscillation. Simultaneously with the start of system clock oscillation, the system clock is supplied to the entire LSI. Note that the $\overline{\text{RES}}$ pin must be held low until clock oscillation is stabilized. If the $\overline{\text{RES}}$ pin is driven high after the clock oscillation stabilization time has elapsed, the CPU starts reset exception handling.

Figure 24.2 shows an example in which a transition is made to software standby mode at the falling edge of the NMI pin, and software standby mode is cleared at the rising edge of the NMI pin.

In this example, an NMI interrupt is accepted with the NMIEG bit in SYSCR cleared to 0 (falling edge specification), then the NMIEG bit is set to 1 (rising edge specification), the SSBY bit is set to 1, and a SLEEP instruction is executed, causing a transition to software standby mode.

Software standby mode is then cleared at the rising edge of the NMI pin.

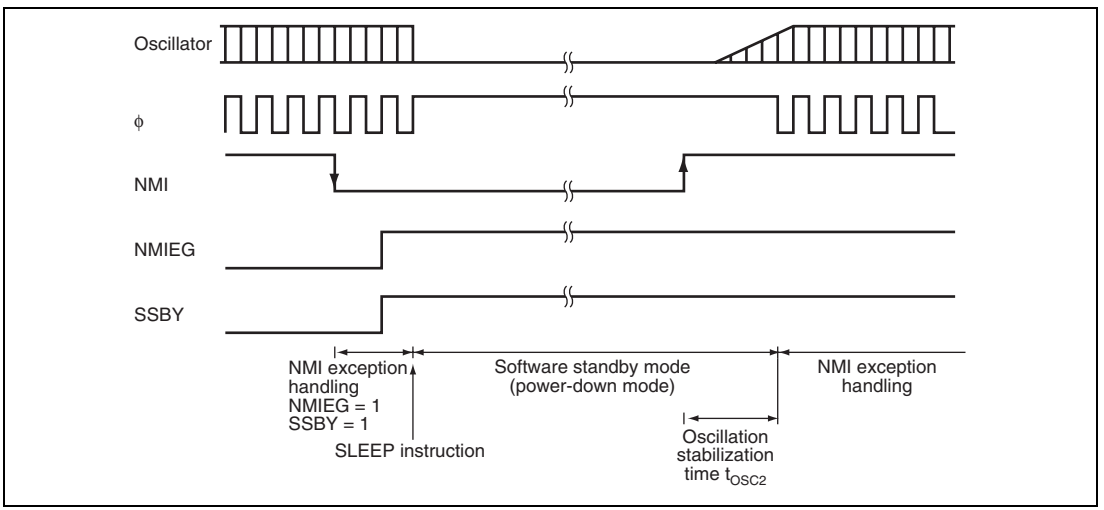

Figure 24.3 Software Standby Mode Application Example

Register Abbreviation	Reset	High-Speed/Medium speed	Watch	Sleep	Module Stop	Software Standby	Module
TCORA_0	Initialized	—	—	—	—	—	TMR_0, TMR_1
TCORA_1	Initialized	—	—	—	—	—	
TCORB_0	Initialized	—	—	—	—	—	
TCORB_1	Initialized	—	—	—	—	—	
TCNT_0	Initialized	—	—	—	—	—	
TCNT_1	Initialized	—	—	—	—	—	
ICCR_0	Initialized	—	—	—	—	—	IIC_0
ICSR_0	Initialized	—	—	—	—	—	
ICDR_0	—	—	—	—	—	—	
SARX_0	Initialized	—	—	—	—	—	
ICMR_0	Initialized	—	—	—	—	—	
SAR_0	Initialized	—	—	—	—	—	
KBCRH_3	Initialized	—	—	—	—	—	PS2_3
KBCRL_3	Initialized	—	—	—	—	—	
KBBR_3	Initialized	—	—	—	—	—	
KBCR2_3	Initialized	—	—	—	—	—	
TCSR_1	Initialized	—	—	—	—	—	WDT_1
TCNT_1	Initialized	—	—	—	—	—	
TCR_X	Initialized	—	—	—	—	—	TMR_X
TCSR_X	Initialized	—	—	—	—	—	
TICRR	Initialized	—	—	—	—	—	
TICRF	Initialized	—	—	—	—	—	
TCNT_X	Initialized	—	—	—	—	—	
TCORC	Initialized	—	—	—	—	—	
TCORA_X	Initialized	—	—	—	—	—	
TCORB_X	Initialized	—	—	—	—	—	
TCONRI	Initialized	—	—	—	—	—	
TCONRS	Initialized	—	—	—	—	—	TMR_X, TMR_Y

B. Product Lineup

Product Type		Type Code	Mark Code	Package (Code)
H8S/2117	Flash memory version	R4F2117	F2117TE20V	PTQP0144LC-A (TFP-144V)
			F2117BG20V	PLBG0176GA-A (BP-176V)
			F2117LP20V	PTLG0145JB-A (TLP-145V)