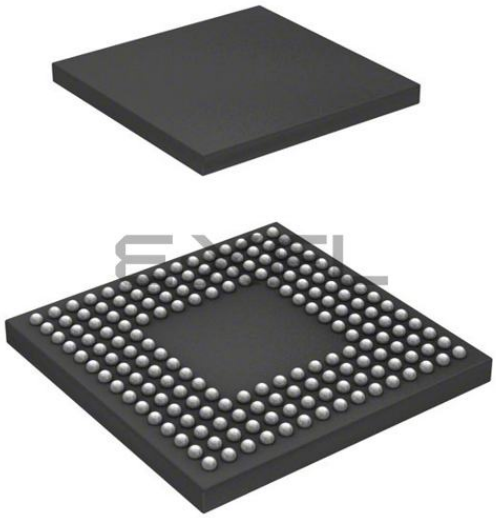

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Details	
Product Status	Not For New Designs
Core Processor	H8S/2600
Core Size	16-Bit
Speed	20MHz
Connectivity	FIFO, I²C, LPC, SCI, SmartCard
Peripherals	POR, PWM, WDT
Number of I/O	128
Program Memory Size	160KB (160K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	External
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LFBGA
Supplier Device Package	176-LFBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2117vbg20v

2.8 Processing States

The H8S/2600 CPU has four main processing states: the reset state, exception handling state, program execution state and power-down state. Figure 2.13 indicates the state transitions.

- Reset State

  In this state, the CPU and all on-chip peripheral modules are initialized and not operating. When the $\overline{\text{RES}}$ input goes low, all current processing stops and the CPU enters the reset state. All interrupts are masked in the reset state. Reset exception handling starts when the $\overline{\text{RES}}$ signal changes from low to high. For details, refer to section 4, Exception Handling.

  The reset state can also be entered by a watchdog timer overflow.

- Exception-Handling State

  The exception-handling state is a transient state that occurs when the CPU alters the normal processing flow due to an exception source, such as a reset, trace, interrupt, or trap instruction. The CPU fetches a start address (vector) from the exception vector table and branches to that address. For further details, refer to section 4, Exception Handling.

- Program Execution State

  In this state, the CPU executes program instructions in sequence.

- Program Stop State

  This is a power-down state in which the CPU stops operating. The program stop state occurs when a SLEEP instruction is executed or the CPU enters software standby mode. For further details, refer to section 24, Power-Down Modes.

Bit	Bit Name	Initial Value	R/W	Description
1	KINWUE	0	R/W	Keyboard Control Register Access Enable When the RELOCATE bit is cleared to 0, this bit enables or disables CPU access for the keyboard matrix interrupt registers (KMIMRA and KMIMR), pull-up MOS control register (KMPCR), and registers (TCR_X/TCR_Y, TCSR_X/TCSR_Y, TICRR/TCORA_Y, TICRF/TCORB_Y, TCNT_X/TCNT_Y, TCORC, TCORA_X, TCORB_X, TCONRI, and TCONRS) of 8-bit timers (TMR_X and TMR_Y) 0: Enables CPU access for registers of TMR_X and TMR_Y in areas from H'(FF)FFF0 to H'(FF)FFF7 and from H'(FF)FFFC to H'(FF)FFFF 1: Enables CPU access for the keyboard matrix interrupt registers and input pull-up MOS control register in areas from H'(FF)FFF0 to H'(FF)FFF7 and from H'(FF)FFFC to H'(FF)FFFF When the RELOCATE bit is set to 1, this bit is disabled. For details, see section 3.2.4, System Control Register 3 (SYSCR3) and section 25, List of Registers.
0	RAME	1	R/W	RAM Enable Enables or disables on-chip RAM. 0: On-chip RAM is disabled 1: On-chip RAM is enabled

Port	Description	Bit	Function			Input Pull-up MOS Function	LED Drive Capability (5 mA Sink Current)	On-Chip Noise Canceller
			I/O	Input	Output			
Port 4	General I/O port also functioning as PWMX and PWMU_B outputs, TCM input, and TMR_0, TMR_1, IIC_1, and SCI_2 inputs/outputs	7	P47	TCMCKI3/ TCMMCI3	PWX1/PWMU5B	—	—	—
		6	P46	TCMCYI3	PWX0/PWMU4B			
		5	P45	TCMCKI2/ TCMMCI2	PWMU3B			
		4	P44	TCMCYI2	TMO1/PWMU2B			
		3	P43/SCK2	TMI1/TCMCKI1/ TCMMCI1	—			
		2	P42/SDA1	TCMCYI1				
		1	P41	RxD2/TCMCKI0/ TCMMCI0	TMO0			
		0	P40	TMI0/TCMCYI0	TxD2			
Port 5	General I/O port also functioning as IIC_0 and SCIF inputs/outputs	2	P52/SCL0	—	—	—	—	—
		1	P51	FRxD	—			
		0	P50	—	FTxD			
Port 6	General I/O port also functioning as interrupt input and keyboard input	7	P67	$\overline{\text{KIN7}}$/IRQ7	—	O	—	O
		6	P66	$\overline{\text{KIN6}}$/IRQ6	—			
		5	P65	$\overline{\text{KIN5}}$	—			
		4	P64	$\overline{\text{KIN4}}$	—			
		3	P63	$\overline{\text{KIN3}}$	—			
		2	P62	$\overline{\text{KIN2}}$	—			
		1	P61	$\overline{\text{KIN1}}$	—			
		0	P60	$\overline{\text{KIN0}}$	—			

Port	Description	Bit	Function			Input Pull-up MOS Function	LED Drive Capability (5 mA Sink Current)	On-Chip Noise Canceller
			I/O	Input	Output			
Port D	General I/O port also functioning as A/D converter analog input	7	PD7	AN15	—	O	O	—
		6	PD6	AN14	—			
		5	PD5	AN13	—			
		4	PD4	AN12	—			
		3	PD3	AN11	—			
		2	PD2	AN10	—			
		1	PD1	AN9	—			
		0	PD0	AN8	—			
Port E	General input port also functioning as external sub-clock input, emulator input/output	4	—	PE4*[1]/ETMS	—	—	—	—
		3	—	PE3*[1]	ETDO			
		2	—	PE2*[1]/ETDI	—			
		1	—	PE1*[1] /ETCK	—			
		0	—	PE0/ExEXCL	—			
Port F	General I/O port also functioning as interrupt and TDP inputs, TMR_X, TMR_Y, and PWM outputs	7	PF7	—	PWMU5A	O	—	—
		6	PF6	—	PWMU4A			
		5	PF5	—	PWMU3A			
		4	PF4	—	PWMU2A			
		3	PF3	TDPCKI0/ TDPMCI0/$\overline{\text{IRQ11}}$	TMOX			
		2	PF2	TDPCYI0//$\overline{\text{IRQ10}}$	TMOY			
		1	PF1	$\overline{\text{IRQ9}}$	PWMU1A			
		0	PF0	$\overline{\text{IRQ8}}$	PWMU0A			

Port		Output Specification Signal Name	Output Signal Name	Signal Selection Register Settings	Internal Module Settings
P8	6	SCK1_OE	SCK1		SCI_1.SMR.C/$\overline{A}$ = 1 or SCI_1.SMR.C/$\overline{A}$ = 0, SCR.CKE[1:0] = 01/10/11
		SCL1_OE	SCL1	PTCNT1.IIC1AS PTCNT1.IIC1BS	ICE•$\overline{IIC1AS}$•$\overline{IIC1BS}$ = 1
	5	P85_OE	P85		
	4	TxD1_OE	TxD1		SCI_1.SCR.TE = 1
	3	P83_OE	P83		
	2	$\overline{CLKRUN}$_OE	$\overline{CLKRUN}$		LPC.HICR5.SCIFE, HICR4.LPC4E, HICR0.LPC[3E:1E] LPCENABLE = 1: SCIFE + LPC4E + LPC3E + LPC2E + LPC1E
	1	GA20_OE	GA20		LPC.HICR0.FGA20E = 1
	0	$\overline{PME}$_OE	$\overline{PME}$		LPC.HICR0.PMEE = 1
P9	7	SDA0_OE	SDA	PTCNT1.IIC0AS PTCNT1.IIC0BS	ICE•$\overline{IIC0AS}$•$\overline{IIC0BS}$ = 1
	6	ϕ_OE	ϕ		
	5	P95_OE	P95		
	4	P94_OE	P94		
	3	P93_OE	P93		
	2	P92_OE	P92		
	1	P91_OE	P91		
	0	P90_OE	P90		
PA	7	PS2CD_OE	PS2CD		PS2_2.KBCRH.KBIOE = 1
	6	PS2CC_OE	PS2CC		PS2_2.KBCRH.KBIOE = 1
	5	PS2BD_OE	PS2BD		PS2_1.KBCRH.KBIOE = 1
	4	PS2BC_OE	PS2BC		PS2_1.KBCRH.KBIOE = 1
	3	PS2AD_OE	PS2AD		PS2_0.KBCRH.KBIOE = 1
	2	PS2AC_OE	PS2AC		PS2_0.KBCRH.KBIOE = 1
	1	PS2DD_OE	PS2DD		PS2_3.KBCRH.KBIOE = 1
	0	PS2DC_OE	PS2DC		PS2_3.KBCRH.KBIOE = 1

9.4 Bus Master Interface

DACNT, DADRA, and DADRB are 16-bit registers. The data bus linking the bus master and the on-chip peripheral modules, however, is only 8 bits wide. When the bus master accesses these registers, it therefore uses an 8-bit temporary register (TEMP).

These registers are written to and read from as follows.

- Write

  When the upper byte is written to, the upper-byte write data is stored in TEMP. Next, when the lower byte is written to, the lower-byte write data and TEMP value are combined, and the combined 16-bit value is written in the register.

- Read

  When the upper byte is read from, the upper-byte value is transferred to the CPU and the lower-byte value is transferred to TEMP. Next, when the lower byte is read from, the lower-byte value in TEMP is transferred to the CPU.

These registers should always be accessed 16 bits at a time with a MOV instruction, and the upper byte should always be accessed before the lower byte. Correct data will not be transferred if only the upper byte or only the lower byte is accessed. Also note that a bit manipulation instruction cannot be used to access these registers.

Example 1: Write to DACNT

```
MOV.W R0, @DACNT      ; Write R0 contents to DACNT
```

Example 2: Read DADRA

```
MOV.W @DADRA, R0      ; Copy contents of DADRA to R0
```

Channel	Register Name	Abbreviation	R/W	Initial Value	Address	Data Bus Width
Channel 2	Timer general register A_2	TGRA_2	R/W	H'FFFF	H'FE78	16
	Timer general register B_2	TGRB_2	R/W	H'FFFF	H'FE7A	16
Common	Timer start register	TSTR	R/W	H'00	H'FEB0	8
	Timer synchro register	TSYR	R/W	H'00	H'FEB1	8

10.3.1 Timer Control Register (TCR)

The TCR registers control the TCNT operation for each channel. The TPU has a total of three TCR registers, one for each channel (channel 0 to 2). TCR register settings should be made only when TCNT operation is stopped.

Bit	Bit Name	Initial value	R/W	Description
7	CCLR2	0	R/W	Counter Clear 2 to 0
6	CCLR1	0	R/W	These bits select the TCNT counter clearing source. See tables 10.4 and 10.5 for details.
5	CCLR0	0	R/W	
4	CKEG1	0	R/W	Clock Edge 1 and 0
3	CKEG0	0	R/W	These bits select the input clock edge. When the input clock is counted using both edges, the input clock cycle is divided in 2 (φ/4 both edges = φ/2 rising edge). If phase counting mode is used on channels 1, 2, 4, and 5, this setting is ignored and the phase counting mode setting has priority. Internal clock edge selection is valid when the input clock is φ/4 or slower. This setting is ignored if the input clock is φ/1 and rising edge count is selected. 00: Count at rising edge 01: Count at falling edge 1x: Count at both edges
2	TPSC2	0	R/W	Time Prescaler 2 to 0
1	TPSC1	0	R/W	These bits select the TCNT counter clock. The clock source can be selected independently for each channel. See tables 10.6 to 10.8 for details.
0	TPSC0	0	R/W	

[Legend]

x: Don't care

(b) When TGR is an input capture register

Figure 10.20 shows an operation example in which TGRA has been designated as an input capture register, and buffer operation has been designated for TGRA and TGRC. Counter clearing by TGRA input capture has been set for TCNT, and both rising and falling edges have been selected as the TIOCA pin input capture input edge. As buffer operation has been set, when the TCNT value is stored in TGRA upon occurrence of input capture A, the value previously stored in TGRA is simultaneously transferred to TGRC.

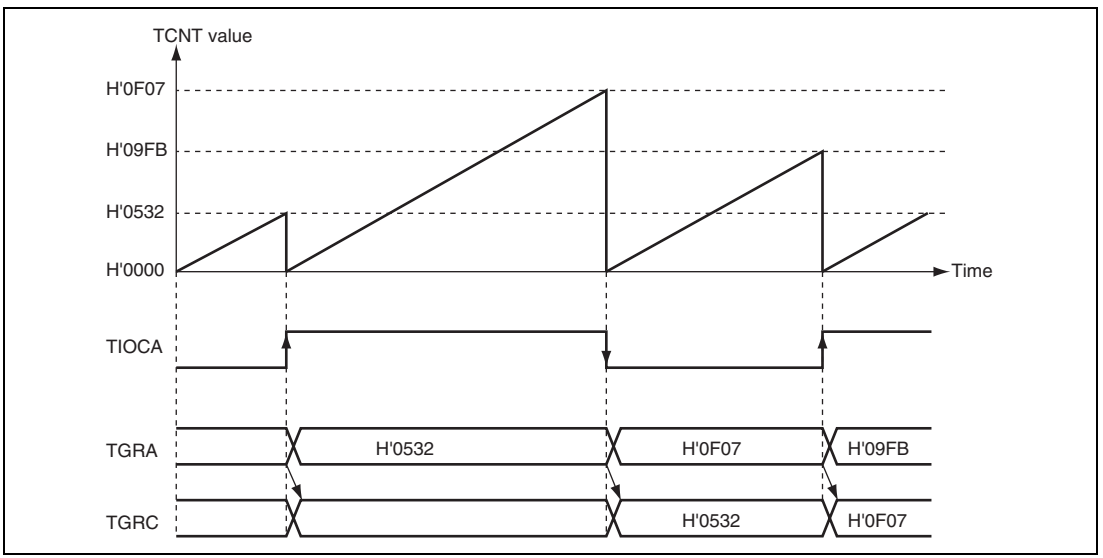

Figure 10.20 Example of Buffer Operation (2)

Table 10.19 PWM Output Registers and Output Pins

		Output Pins	
Channel	**Registers**	**PWM Mode 1**	**PWM Mode 2**
0	TGRA_0	TIOCA0	TIOCA0
	TGRB_0		TIOCB0
	TGRC_0	TIOCC0	TIOCC0
	TGRD_0		TIOCD0
1	TGRA_1	TIOCA1	TIOCA1
	TGRB_1		TIOCB1
2	TGRA_2	TIOCA2	TIOCA2
	TGRB_2		TIOCB2

Note: In PWM mode 2, PWM output is not possible for the TGR register in which the period is set.

(1) Example of PWM Mode Setting Procedure

Figure 10.21 shows an example of the PWM mode setting procedure.

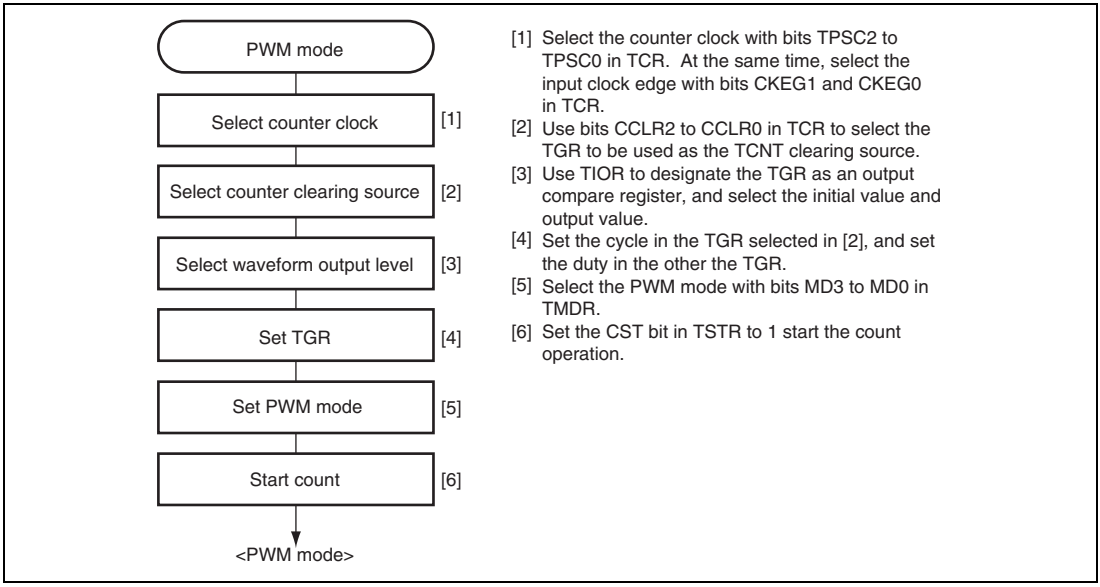

Figure 10.21 Example of PWM Mode Setting Procedure

Table 13.4 Registers Accessible by TMR_X/TMR_Y

TMRX/Y	H'FFF0	H'FFF1	H'FFF2	H'FFF3	H'FFF4	H'FFF5	H'FFF6	H'FFF7
0	TMR_X	TMR_X	TMR_X	TMR_X	TMR_X	TMR_X	TMR_X	TMR_X
	TCR_X	TCSR_X	TICRR	TICRF	TCNT	TCORC	TCORA_X	TCORB_X
1	TMR_Y	TMR_Y	TMR_Y	TMR_Y	TMR_Y	TMR_Y		
	TCR_Y	TCSR_Y	TCORA_Y	TCORB_Y	TCNT_Y			

13.3.10 Timer XY Control Register (TCRXY)

TCRXY selects the TMR_X and TMR_Y output pins and internal clock.

Bit	Bit Name	Initial Value	R/W	Description
7, 6	—	All 0	R/W	Reserved The initial value should not be changed.
5	CKSX	0	R/W	TMR_X Clock Select For details about selection, see table 13.3.
4	CKSY	0	R/W	TMR_Y Clock Select For details about selection, see table 13.3.
3 to 0	—	All 0	R/W	Reserved The initial value should not be changed.

13.9.3 Conflict between TCOR Write and Compare-Match

If a compare-match occurs during the T_2 state of a TCOR write cycle as shown in figure 13.15, the TCOR write takes priority and the compare-match signal is disabled. With TMR_X, a TICR input capture conflicts with a compare-match in the same way as with a write to TCORC. In this case also, the input capture takes priority and the compare-match signal is disabled.

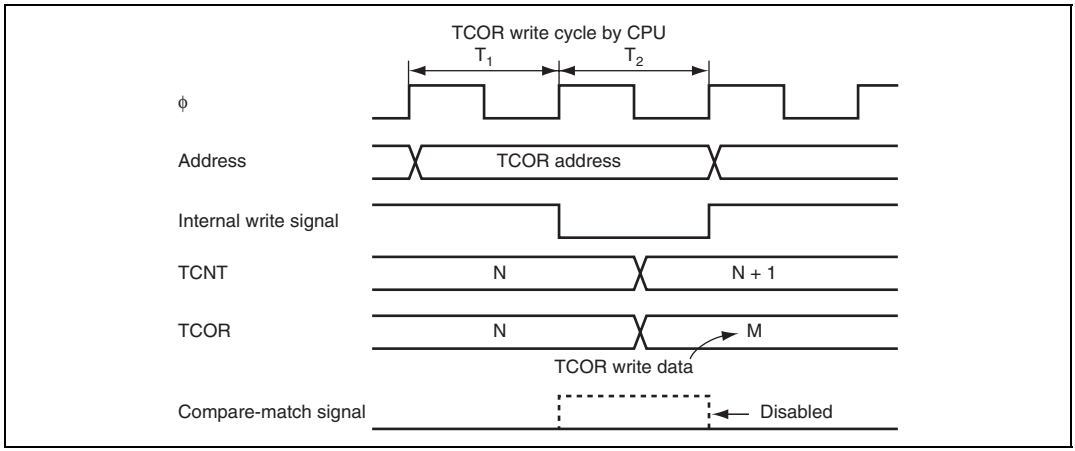

Figure 13.15 Conflict between TCOR Write and Compare-Match

13.9.4 Conflict between Compare-Matches A and B

If compare-matches A and B occur at the same time, the operation follows the output status that is defined for compare-match A or B, according to the priority of the timer output shown in table 13.7.

Table 13.7 Timer Output Priorities

Output Setting	Priority
Toggle output	High
1 output	↑
0 output	↑
No change	Low

16.3.12 Modem Status Register (FMSR)

FMSR is a read-only register that indicates the status of or a change in the modem control pins.

Bit	Bit Name	Initial Value	R/W	Description
7	DCD	Undefined	R	Data Carrier Detect Indicates the inverted state of the $\overline{\text{DCD}}$ input pin.
6	RI	Undefined	R	Ring Indicator Indicates the inverted state of the $\overline{\text{RI}}$ input pin.
5	DSR	Undefined	R	Data Set Ready Indicates the inverted state of the $\overline{\text{DSR}}$ input pin.
4	CTS	Undefined	R	Clear to Send Indicates the inverted state of the $\overline{\text{CTS}}$ input pin.
3	DDCD	0	R	Delta Data Carrier Indicator Indicates a change in the $\overline{\text{DCD}}$ input signal after the DDCD bit is read. 0: No change in the $\overline{\text{DCD}}$ input signal after FMSR read [Clearing condition] FMSR read 1: A change in the $\overline{\text{DCD}}$ input signal after FMSR read [Setting condition] A change in the $\overline{\text{DCD}}$ input signal
2	TERI	0	R	Trailing Edge Ring Indicator Indicates a rise in the $\overline{\text{RI}}$ input signal after the TERI bit is read. 0: No change in the $\overline{\text{RI}}$ input signal after FMSR read [Clearing condition] FMSR read 1: A rise in the $\overline{\text{RI}}$ input signal after FMSR read [Setting condition] A rise in the $\overline{\text{RI}}$ input pin

Bit	Bit Name	Initial Value	R/W	Description
2	AAS	0	R/(W)*	Slave Address Recognition Flag In I²C bus format slave receive mode, this flag is set to 1 if the first frame following a start condition matches bits SVA6 to SVA0 in SAR, or if the general call address (H'00) is detected. [Setting condition] When the slave address or general call address (one frame including a R/$\overline{W}$ bit is H'00) is detected in slave receive mode and FS = 0 in SAR [Clearing conditions] • When ICDR is written to (transmit mode) or read from (receive mode) • When 0 is written in AAS after reading AAS = 1 • In master mode
1	ADZ	0	R/(W)*	General Call Address Recognition Flag In I²C bus format slave receive mode, this flag is set to 1 if the first frame following a start condition is the general call address (H'00). [Setting condition] When the general call address (one frame including a R/$\overline{W}$ bit is H'00) is detected in slave receive mode and FS = 0 or FSX = 0 [Clearing conditions] • When ICDR is written to (transmit mode) or read from (receive mode) • When 0 is written in ADZ after reading ADZ = 1 • In master mode If a general call address is detected while FS=1 and FSX=0, the ADZ flag is set to 1; however, the general call address is not recognized (AAS flag is not set to 1).

18.5.2 KD Output by KDO bit (KBCRL) and by Automatic Transmission

Figure 18.20 shows the relationship between the KD output by the KDO bit (KBCRL) and by the automatic transmission. Switch to the KD output by the automatic transmission is performed when KBTS is set to 1 and TXCR is not cleared to 0. In this case, the KD output by the KDO bit (KBCRL) is masked.

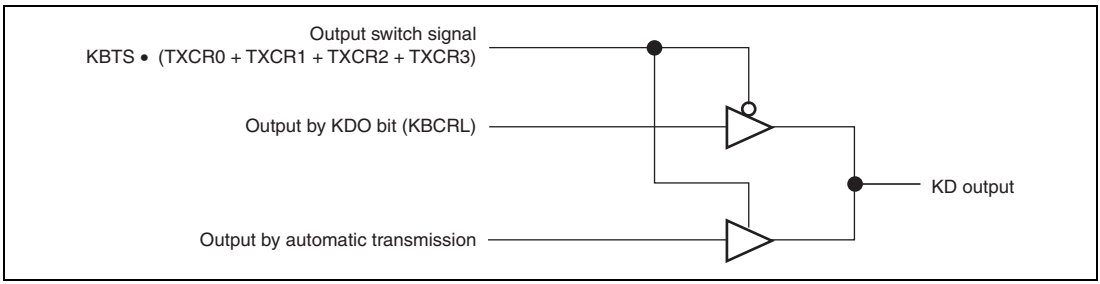

Figure 18.20 KDO Output

18.5.3 Module Stop Mode Setting

Keyboard buffer control unit operation can be enabled or disabled using the module stop control register. The initial setting is for keyboard buffer control unit operation to be halted. Register access is enabled by canceling module stop mode. For details, see section 24, Power-Down Modes.

18.5.4 Medium-Speed Mode

In medium-speed mode, the PS2 operates with the medium-speed clock. For normal operation of the PS2, set the medium-speed clock to a frequency of 300 kHz or higher.

18.5.5 Transmit Completion Flag (KBTE)

When TXCR3 to TXCR0 are 1011 (transmit completion notification) and then the TXCR3 to TXCR0 are initialized by clearing KBIOE or KBTS to 0, the transmit completion flag (KBTE) is set. In this case, KTER is invalid.

When LPC3E = 1, an I/O address received in an LPC I/O cycle is compared with the contents of LADR3. When determining an IDR3, ODR3, or STR3 address match, bit 0 in LADR3 is regarded as 0, and the value of bit 2 is ignored. When determining a TWR0 to TWR15 address match, bit 4 in LADR3 is inverted, and the values of bits 3 to 0 are ignored.

- Host select register

I/O Address					Transfer	
Bit 4	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Cycle**	**Host Select Register**
Bit 4	Bit 3	0	Bit 1	0	I/O write	IDR3 write, C/$\overline{D}$3 ← 0
Bit 4	Bit 3	1	Bit 1	0	I/O write	IDR3 write, C/$\overline{D}$3 ← 1
Bit 4	Bit 3	0	Bit 1	0	I/O read	ODR3 read
Bit 4	Bit 3	1	Bit 1	0	I/O read	STR3 read
$\overline{\text{Bit 4}}$	0	0	0	0	I/O write	TWR0MW write
$\overline{\text{Bit 4}}$	0	0	0	1	I/O write	TWR1 to TWR15 write
	:	:	:	:		
	1	1	1	1		
$\overline{\text{Bit 4}}$	0	0	0	0	I/O read	TWR0SW read
$\overline{\text{Bit 4}}$	0	0	0	1	I/O read	TWR1 to TWR15 read
	:	:	:	:		
	1	1	1	1		

Note: * When channel 3 is used, the content of LADR3 must be set so that the addresses for channels 1, 2, 4, and SCIF are different.

12. If data other than H'FF is to be written to the key code area in programmer mode, a verification error will occur unless a software countermeasure is taken for the PROM programmer and version of program.
13. The programming program that includes the initialization routine and the erasing program that includes the initialization routine are each 3 kbytes or less. Accordingly, when the CPU clock frequency is 20 MHz, the download for each program takes approximately 200 μs at the maximum.
14. A programming/erasing program for the flash memory used in a conventional F-ZTAT H8, H8S microcomputer which does not support download of the on-chip program by setting the SCO bit in FCCS to 1 cannot run in this LSI. Be sure to download the on-chip program to execute programming/erasing of the flash memory in this F-ZTAT H8/H8S microcomputer.
15. Unlike a conventional F-ZTAT H8/H8S microcomputers, measures against a program crash are not taken by WDT while programming/erasing and downloading a programming/erasing program. When needed, measures should be taken by user. A periodic interrupt generated by the WDT can be used as the measures, as an example. In this case, the interrupt generation period should take into consideration time to program/erase the flash memory.
16. When downloading the programming/erasing program, do not clear the SCO bit in FCCS to 0 after immediately setting it to 1. Otherwise, download cannot be performed normally. Immediately after executing the instruction to set the SCO bit to 1, dummy read of the FCCS must be executed twice.
17. The contents of some registers are not saved in a programming/programming end/erasing program. When needed, save registers in the procedure program.

Table 24.3 LSI Internal States in Each Operating Mode

Function		High Speed	Medium Speed	Sleep	Module Stop	Watch	Software Standby
System clock pulse generator		Functioning	Functioning	Functioning	Functioning	Stopped	Stopped
Subclock input		Functioning	Functioning	Functioning	Functioning	Functioning	Stopped
CPU	Instruction execution	Functioning	Medium-speed operation	Stopped	Functioning	Stopped	Stopped
	Registers			Retained		Retained	Retained
External interrupts	NMI	Functioning	Functioning	Functioning	Functioning	Functioning	Functioning
	IRQ0 to IRQ15						
	KIN0 to KIN15						
	WUE8 to WUE15						
On-chip peripheral modules	WDT_1	Functioning	Functioning	Functioning	Functioning	Subclock operation	Stopped (retained)
	WDT_0					Stopped (retained)	
	TMR_0, TMR_1				Functioning/ stopped (retained)		
	TPU TCM_0 to 3 TDP_0 to 2						
	TMR_X, TMR_Y						
	SCIF						
	IIC_0 to 2						
	LPC						
	PS2_0 to 3		Medium-speed operation/functioning				
	PWMU		Functioning		Functioning/ stopped (reset)	Stopped (reset)	Stopped (reset)
	PWM						
	PWMX						
	SCI_1, SCI_2						
	A/D converter						
	RAM	Functioning	Functioning	Functioning	Functioning	Retained	Retained
	I/O	Functioning	Functioning	Functioning	Functioning	Retained	Retained

Note: Stopped (retained) means that the internal register values are retained and the internal state is operation suspended. Stopped (reset) means that the internal register values and the internal state are initialized. In module stop mode, only modules for which a stop setting has been made are stopped (reset or retained).

Register Abbreviation	Reset	High-Speed/Medium speed	Watch	Sleep	Module Stop	Software Standby	Module
TCORA_0	Initialized	—	—	—	—	—	TMR_0, TMR_1
TCORA_1	Initialized	—	—	—	—	—	
TCORB_0	Initialized	—	—	—	—	—	
TCORB_1	Initialized	—	—	—	—	—	
TCNT_0	Initialized	—	—	—	—	—	
TCNT_1	Initialized	—	—	—	—	—	
ICCR_0	Initialized	—	—	—	—	—	IIC_0
ICSR_0	Initialized	—	—	—	—	—	
ICDR_0	—	—	—	—	—	—	
SARX_0	Initialized	—	—	—	—	—	
ICMR_0	Initialized	—	—	—	—	—	
SAR_0	Initialized	—	—	—	—	—	
KBCRH_3	Initialized	—	—	—	—	—	PS2_3
KBCRL_3	Initialized	—	—	—	—	—	
KBBR_3	Initialized	—	—	—	—	—	
KBCR2_3	Initialized	—	—	—	—	—	
TCSR_1	Initialized	—	—	—	—	—	WDT_1
TCNT_1	Initialized	—	—	—	—	—	
TCR_X	Initialized	—	—	—	—	—	TMR_X
TCSR_X	Initialized	—	—	—	—	—	
TICRR	Initialized	—	—	—	—	—	
TICRF	Initialized	—	—	—	—	—	
TCNT_X	Initialized	—	—	—	—	—	
TCORC	Initialized	—	—	—	—	—	
TCORA_X	Initialized	—	—	—	—	—	
TCORB_X	Initialized	—	—	—	—	—	
TCONRI	Initialized	—	—	—	—	—	
TCONRS	Initialized	—	—	—	—	—	TMR_X, TMR_Y

Module	Register Abbreviation	Number of Bits	Address	Data Bus Width	Access States
PORT	P2DR	8	H'FFB3 (PORTS = 0)	8	2
PORT	P3DDR	8	H'FFB4 (PORTS = 0)	8	2
PORT	P4DDR	8	H'FFB5 (PORTS = 0)	8	2
PORT	P3DR	8	H'FFB6 (PORTS = 0)	8	2
PORT	P4DR	8	H'FFB7 (PORTS = 0)	8	2
PORT	P5DDR	8	H'FFB8 (PORTS = 0)	8	2
PORT	P6DDR	8	H'FFB9 (PORTS = 0)	8	2
PORT	P5DR	8	H'FFBA (PORTS = 0)	8	2
PORT	P6DR	8	H'FFBB (PORTS = 0)	8	2
PORT	PBODR	8	H'FFBC (PORTS = 0)	8	2
PORT	P8DDR	8	H'FFBD (Write) (PORTS = 0)	8	2
PORT	PBPIN	8	H'FFBD (Read) (PORTS = 0)	8	2
PORT	P7PIN	8	H'FFBE (Read) (PORTS = 0)	8	2
PORT	PBDDR	8	H'FFBE (Write) (PORTS = 0)	8	2
PORT	P8DR	8	H'FFBF (PORTS = 0)	8	2
PORT	P9DDR	8	H'FFC0 (PORTS = 0)	8	2
PORT	P9DR	8	H'FFC1 (PORTS = 0)	8	2
PORT	KMPCR	8	H'FFF2 (RELOCATE = 0) (PORTS = 0)	8	2

Module	Register Abbreviation	Number of Bits	Address	Data Bus Width	Access States
TMR_0	TCORB_0	8	H'FFCE	16	2
TMR_0	TCNT_0	8	H'FFD0	16	2
TMR_1	TCR_1	8	H'FFC9	8	2
TMR_1	TCSR_1	8	H'FFCB	16	2
TMR_1	TCORA_1	8	H'FFCD	16	2
TMR_1	TCORB_1	8	H'FFCF	16	2
TMR_1	TCNT_1	8	H'FFD1	16	2
TMR_X	TCR_X	8	H'FFF0	8	2
TMR_X	TCSR_X	8	H'FFF1	8	2
TMR_X	TICRR	8	H'FFF2	8	2
TMR_X	TICRF	8	H'FFF3	8	2
TMR_X	TCNT_X	8	H'FFF4	8	2
TMR_X	TCORC	8	H'FFF5	8	2
TMR_X	TCORA_X	8	H'FFF6	8	2
TMR_X	TCORB_X	8	H'FFF7	8	2
TMR_X	TCONRI	8	H'FFFC	8	2
TMR_Y	TCR_Y	8	H'FEC8 (RELOCATE = 1)	8	2
TMR_Y	TCSR_Y	8	H'FEC9 (RELOCATE = 1)	8	2
TMR_Y	TCORA_Y	8	H'FECA (RELOCATE = 1)	8	2
TMR_Y	TCORB_Y	8	H'FECB (RELOCATE = 1)	8	2
TMR_Y	TCNT_Y	8	H'FECC (RELOCATE = 1)	8	2
TMR_Y	TCR_Y	8	H'FFF0 (RELOCATE = 0)	8	2
TMR_Y	TCSR_Y	8	H'FFF1 (RELOCATE = 0)	8	2
TMR_Y	TCORA_Y	8	H'FFF2 (RELOCATE = 0)	8	2
TMR_Y	TCORB_Y	8	H'FFF3 (RELOCATE = 0)	8	2