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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	H8S/2600
Core Size	16-Bit
Speed	20MHz
Connectivity	FIFO, I²C, LPC, SCI, SmartCard
Peripherals	POR, PWM, WDT
Number of I/O	112
Program Memory Size	160KB (160K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	External
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	144-TQFP
Supplier Device Package	144-TQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2117vt20hv

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions may occur due to the false recognition of the pin state as an input signal. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

(2) PE0/ExEXCL

The pin function is switched as shown below according to the combination of the EXCLS bit in PTCNT0 and EXCLE bit in LPWRCR. When the EXCLS bit in PTCNT0 and EXCLE bit in LPWRCR are set to 1, this pin can be used as the ExEXCL input pin.

		Setting
		I/O Port
Module Name	Pin Function	ExEXCL
I/O port	PE0 input (initial setting)	0

7.2.15 Port F

(1) PF7/PWMU5, APF6/PWMU4A, PF5/PWMU3A, PF4/PWMU2A

The pin function is switched as shown below according to the combination of the register setting of the PWMU and the PFnDDR bit.

		Setting	
		PWMU	I/O Port
Module Name	Pin Function	PWMUmA_OE	PFnDDR
PWMU	PWMUmA output	1	1
I/O port	PFn output	0	1
	PFn input (initial setting)	—	0

(n = 5 to 2, m = 7 to 4)

Table 7.4 Available Output Signals and Settings in Each Port

Port		Output Specification Signal Name	Output Signal Name	Signal Selection Register Settings	Internal Module Settings
P1	7	P17_OE	P17		
	6	P16_OE	P16		
	5	P15_OE	P15		
	4	P14_OE	P14		
	3	P13_OE	P13		
	2	P12_OE	P12		
	1	P11_OE	P11		
	0	P10_OE	P10		
P2	7	P27_OE	P27		
	6	P26_OE	P26		
	5	P25_OE	P25		
	4	P24_OE	P24		
	3	P23_OE	P23		
	2	P22_OE	P22		
	1	P21_OE	P21		
	0	P20_OE	P20		
P3	7	SERIRQ_OE	SERIRQ		LPC.HICR5.SCIFE, HICR4.LPC4E, HICR0.LPC[3E:1E] LPCENABLE = 1: SCIFE+LPC4E + LPC3E + LPC2E + LPC1E
	6	P36_OE	P36		
	5	P35_OE	P35		
	4	P34_OE	P34		
	3	LAD3_OE	LAD3		
	2	LAD2_OE	LAD2		
	1	LAD1_OE	LAD1		
	0	LAD0_OE	LAD0		

(1) Example of Setting

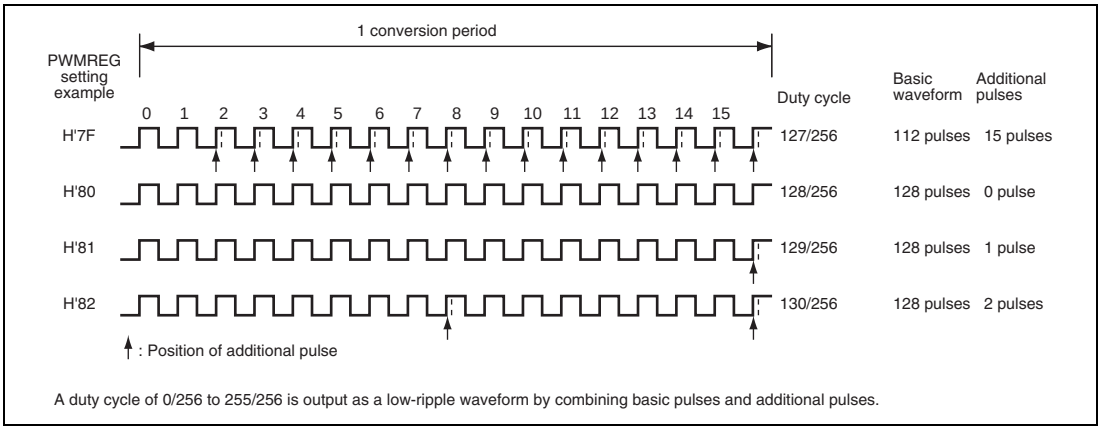

Figure 8.9 Example of WMU Setting

(2) Example of Circuit for Use as D/A Converter

The following shows an example of a circuit in which PWMU output pulses are used as a D/A converter. When a low-pass filter is connected externally to the LSI, low-ripple analog output can be generated. If pulse division mode is used, a D/A output with even less ripple is available.

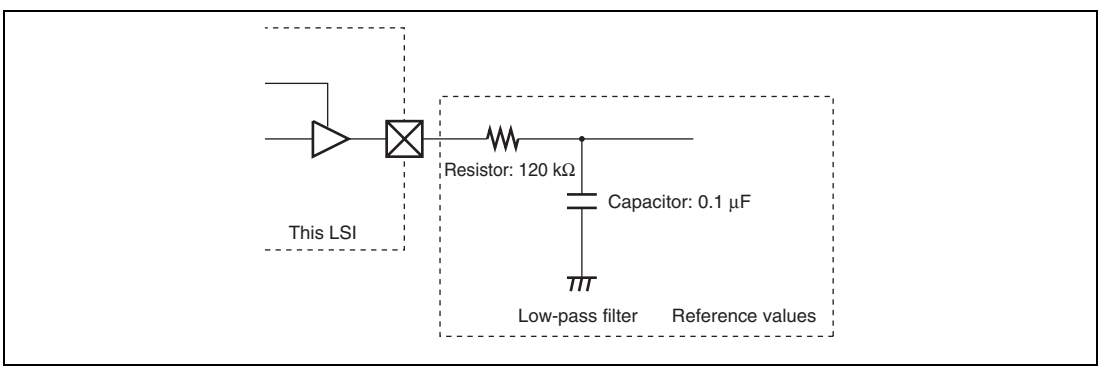

Figure 8.10 Example of Circuit for Use as a D/A Converter

9.4 Bus Master Interface

DACNT, DADRA, and DADRB are 16-bit registers. The data bus linking the bus master and the on-chip peripheral modules, however, is only 8 bits wide. When the bus master accesses these registers, it therefore uses an 8-bit temporary register (TEMP).

These registers are written to and read from as follows.

- Write

  When the upper byte is written to, the upper-byte write data is stored in TEMP. Next, when the lower byte is written to, the lower-byte write data and TEMP value are combined, and the combined 16-bit value is written in the register.

- Read

  When the upper byte is read from, the upper-byte value is transferred to the CPU and the lower-byte value is transferred to TEMP. Next, when the lower byte is read from, the lower-byte value in TEMP is transferred to the CPU.

These registers should always be accessed 16 bits at a time with a MOV instruction, and the upper byte should always be accessed before the lower byte. Correct data will not be transferred if only the upper byte or only the lower byte is accessed. Also note that a bit manipulation instruction cannot be used to access these registers.

Example 1: Write to DACNT

```
MOV.W R0, @DACNT      ; Write R0 contents to DACNT
```

Example 2: Read DADRA

```
MOV.W @DADRA, R0      ; Copy contents of DADRA to R0
```

12.2 Input/Output Pins

Table 12.1 lists the pin configuration of the TDP.

Table 12.1 Pin Configuration

Channel	Pin Name	I/O	Function
0	TDPCKI0 (TDPMCI0)	Input	External counter clock input Cycle measurement control input
	TDPCYI0	Input	External event input
1	TDPCKI1 (TDPMCI1)	Input	External counter clock input Cycle measurement control input
	TDPCYI1	Input	External event input
2	TDPCKI2 (TDPMCI2)	Input	External counter clock input Cycle measurement control input
	TDPCYI2	Input	External event input

Figures 13.1 and 13.2 show block diagrams of 8-bit timers.

An input capture function is added to TMR_X.

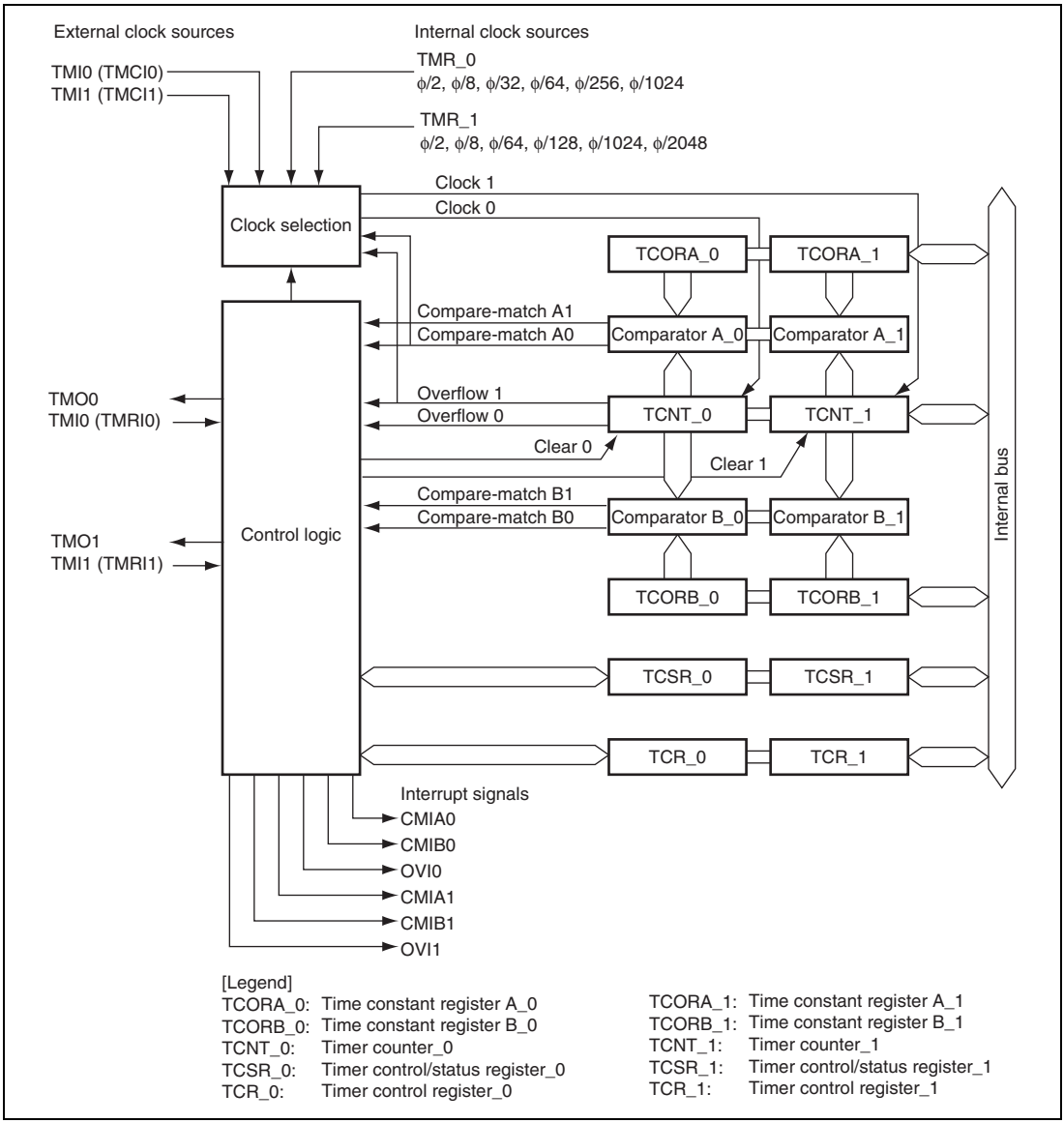

Figure 13.1 Block Diagram of 8-Bit Timer (TMR_0 and TMR_1)

13.5.6 Timing of Overflow Flag (OVF) Setting

The OVF bit in TCSR is set to 1 when the TCNT overflows (changes from H'FF to H'00). Figure 13.10 shows the timing of OVF flag setting.

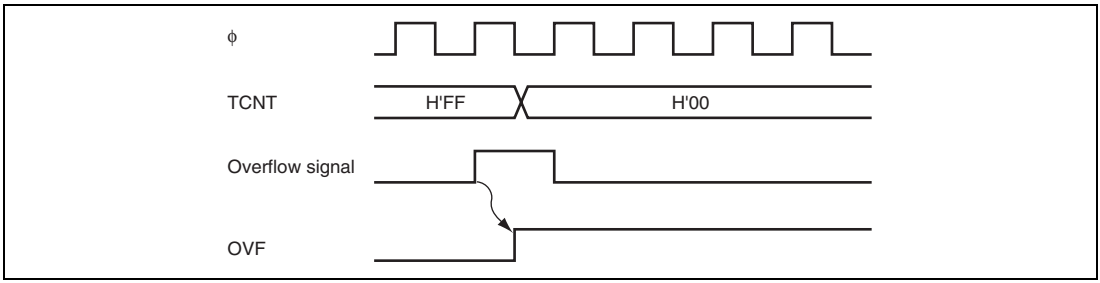

Figure 13.10 Timing of OVF Flag Setting

13.9.6 Mode Setting with Cascaded Connection

If the 16-bit count mode and compare-match count mode are set simultaneously, the input clock pulses for TCNT_0 and TCNT_1, and TCNT_X and TCNT_Y are not generated, and thus the counters will stop operating. Simultaneous setting of these two modes should therefore be avoided.

13.9.7 Module Stop Mode Setting

TMR operation can be enabled or disabled using the module stop control register. The initial setting is for TMR operation to be halted. Register access is enabled by canceling the module stop mode. For details, see section 24, Power-Down Modes.

14.3.2 Timer Control/Status Register (TCSR)

TCSR selects the clock source to be input to TCNT, and the timer mode.

- TCSR_0

Bit	Bit Name	Initial Value	R/W	Description
7	OVF	0	R/(W)*	Overflow Flag Indicates that TCNT has overflowed (changes from H'FF to H'00). [Setting condition] When TCNT overflows (changes from H'FF to H'00) When internal reset request generation is selected in watchdog timer mode, OVF is cleared automatically by the internal reset. [Clearing conditions] • When TCSR is read when OVF = 1, then 0 is written to OVF • When 0 is written to TME
6	WT/$\overline{IT}$	0	R/W	Timer Mode Select Selects whether the WDT is used as a watchdog timer or interval timer. 0: Interval timer mode 1: Watchdog timer mode
5	TME	0	R/W	Timer Enable When this bit is set to 1, TCNT starts counting. When this bit is cleared, TCNT stops counting and is initialized to H′00.
4	—	0	R/(W)	Reserved The initial value should not be changed.
3	RST/$\overline{NMI}$	0	R/W	Reset or NMI Selects to request an internal reset or an NMI interrupt when TCNT has overflowed. 0: An NMI interrupt is requested 1: An internal reset is requested

When, with the I²C bus format selected, IRIC is set to 1 and an interrupt is generated, other flags must be checked in order to identify the source that set IRIC to 1. Although each source has a corresponding flag, caution is needed at the end of a transfer.

When the ICDRE or ICDRF flag is set, the IRTR flag may or may not be set. The IRTR flag is not set at the end of a data transfer up to detection of a retransmission start condition or stop condition after a slave address (SVA) or general call address match in I²C bus format slave mode.

Tables 17.5 and 17.6 show the relationship between the flags and the transfer states.

Table 17.5 Flags and Transfer States (Master Mode)

MST	TRS	BBSY	ESTP	STOP	IRTR	AASX	AL	AAS	ADZ	ACKB	ICDRF	ICDRE	State
1	1	0	0	0	0	0↓	0	0↓	0↓	0	—	0	Idle state (flag clearing required)
1	1	1↑	0	0	1↑	0	0	0	0	0	—	1↑	Start condition detected
1	—	1	0	0	—	0	0	0	0	—	—	—	Wait state
1	1	1	0	0	—	0	0	0	0	1↑	—	—	Transmission end (ACKE=1 and ACKB=1)
1	1	1	0	0	1↑	0	0	0	0	0	—	1↑	Transmission end with ICDRE=0
1	1	1	0	0	—	0	0	0	0	0	—	0↓	ICDR write with the above state
1	1	1	0	0	—	0	0	0	0	0	—	1	Transmission end with ICDRE=1
1	1	1	0	0	—	0	0	0	0	0	—	0↓	ICDR write with the above state or after start condition detected
1	1	1	0	0	1↑	0	0	0	0	0	—	1↑	Automatic data transfer from ICDRT to ICDRS with the above state

19.3.11 Bidirectional Data Registers 0 to 15 (TWR0 to TWR15)

TWR0 to TWR15 are sixteen 8-bit readable/writable registers to both the slave (this LSI) and host. In TWR0, however, two registers (TWR0MW and TWR0SW) are allocated to the same address for both the host and the slave addresses. TWR0MW is a write-only register for the host, and a read-only register for the slave, while TWR0SW is a write-only register for the slave and a read-only register for the host. When the host and slave begin a write, after the respective registers of TWR0 have been written to, arbitration for simultaneous access is performed by checking the status flags whether or not those writes were valid.

When the host has access rights, TWR0MW is selected in TWR0 and the state of TWR0MW is returned when the host reads TWR0SW. Attempts by the slave to write to TWR0SW are invalid.

When the slave has access rights, TWR0SW is selected in TWR0 and the state of TWR0SW is returned when the slave reads TWR0MW. Attempts by the host to write to TWR0MW are invalid.

For the registers selected from the host according to the I/O address, see section 19.3.7, LPC Channel 3 Address Registers H and L (LADR3H and LADR3L).

Data transferred in an LPC I/O write cycle is written to the selected register; in an LPC I/O read cycle, the data in the selected register is transferred to the host. The initial values of TWR0 to TWR15 are H'00.

19.3.12 Status Registers 1 to 4 (STR1 to STR4)

STR1 to STR4 are 8-bit registers that indicate status information during LPC interface processing. The registers selected from the host according to the I/O address are shown in the following table. In an LPC I/O read cycle, the data in the selected register is transferred to the host.

I/O Address					Transfer	
Bits 15 to 4	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Cycle**	**Host Register Selection**
Bits 15 to 4	Bit 3	1	Bit1	Bit 0	I/O read	STRn read

n = 1 to 4

19.3.19 Host Interface Select Register (HISEL)

HISEL selects the function of bits 7 to 4 in STR3 and selects the output of the host interrupt request signal of each frame.

Bit	Bit Name	Initial Value	R/W		Description
			Slave	Host	
7	SELSTR3	0	R/W	—	Status Register 3 Selection Selects the function of bits 7 to 4 in STR3 in combination with the TWRE bit in LADR3L. For details of STR3, see section 19.3.12, Status Registers 1 to 4 (STR1 to STR4). 0: Bits 7 to 4 in STR3 indicate processing status of the LPC interface. 1: [When TWRE = 1] Bits 7 to 4 in STR3 indicate processing status of the LPC interface. [When TWRE = 0] Bits 7 to 4 in STR3 are readable/writable bits which user can use as necessary
6	SELIRQ11	0	R/W	—	Host IRQ Interrupt Select These bits select the state of the output on the SERIRQ pins. 0: [When host interrupt request is cleared] SERIRQ pin output is in the Hi-Z state [When host interrupt request is set] SERIRQ pin output is low 1: [When host interrupt request is cleared] SERIRQ pin output is low [When host interrupt request is set] SERIRQ pin output is in the Hi-Z state.
5	SELIRQ10	0	R/W	—	
4	SELIRQ9	0	R/W	—	
3	SELIRQ6	0	R/W	—	
2	SELSMI	0	R/W	—	
1	SELIRQ12	1	R/W	—	
0	SELIRQ1	1	R/W	—	

(2) Flash Pass and Fail Parameter (FPFR: General Register R0L of CPU)

FPFR indicates the return values of the initialization, programming, and erasure results. The meaning of the bits in FPFR varies depending on the processing.

(a) Initialization before programming/erasing

FPFR indicates the return value of the initialization result.

Bit	Bit Name	Initial Value	R/W	Description
7 to 2	—	—	—	Unused These bits return 0.
1	FQ	—	R/W	Frequency Error Detect Compares the specified CPU operating frequency with the operating frequencies supported by this LSI, and returns the result. 0: Setting of operating frequency is normal 1: Setting of operating frequency is abnormal
0	SF	—	R/W	Success/Fail Returns the initialization result. 0: Initialization has ended normally (no error) 1: Initialization has ended abnormally (error occurs)

22.11 Programmer Mode

Along with its on-board programming mode, this LSI also has a programmer mode as a further mode for the writing and erasing of programs and data. In programmer mode, a general-purpose PROM programmer that supports the device types shown in table 22.16 can be used to write programs to the on-chip ROM without any limitation.

Table 22.16 Device Types Supported in Programmer Mode

Target Memory MAT	Size	Device Type
User MAT	256 kbytes*	FZTAT256V3A
User boot MAT	8 kbytes	FZTATUSBTV3A

Note: * For the R4F2117 model, 160 kbytes of ROM space is available when the user MAT is selected. If programming is performed in programmer mode, H'FF data must be written to address H'28000 to H'3FFFF with 256-kbyte capacity setting.

22.12 Standard Serial Communication Interface Specifications for Boot Mode

The boot program initiated in boot mode performs serial communication using the host and on-chip SCI_1. The serial communication interface specifications are shown below.

The boot program has three states.

1. Bit-rate-adjustment state

   In this state, the boot program adjusts the bit rate to achieve serial communication with the host. Initiating boot mode enables starting of the boot program and entry to the bit-rate-adjustment state. The program receives the command from the host to adjust the bit rate. After adjusting the bit rate, the program enters the inquiry/selection state.
2. Inquiry/selection state

   In this state, the boot program responds to inquiry commands from the host. The device name, clock mode, and bit rate are selected. After selection of these settings, the program is made to enter the programming/erasing state by the command for a transition to the programming/erasing state. The program transfers the libraries required for erasure to the on-chip RAM and erases the user MATs and user boot MATs before the transition.

25.3 Register States in Each Operating Mode

Register Abbreviation	Reset	High-Speed/Medium speed	Watch	Sleep	Module Stop	Software Standby	Module
PIDDR	Initialized	—	—	—	—	—	PORT
PJDDR	Initialized	—	—	—	—	—	
PIODR	Initialized	—	—	—	—	—	
PJODR	Initialized	—	—	—	—	—	
PIPIN	—	—	—	—	—	—	
PJPIN	—	—	—	—	—	—	
PJPCR	Initialized	—	—	—	—	—	
PINOCR	Initialized	—	—	—	—	—	
PJNOCR	Initialized	—	—	—	—	—	
TDPCNT_0	Initialized	—	—	—	—	—	TDP_0
TDPPDMX_0	Initialized	—	—	—	—	—	
TDPPDMN_0	Initialized	—	—	—	—	—	
TDPWDMX_0	Initialized	—	—	—	—	—	
TDPICR_0	Initialized	—	—	—	—	—	
TDPICRF_0	Initialized	—	—	—	—	—	
TDPCSR_0	Initialized	—	—	—	—	—	
TDPCR1_0	Initialized	—	—	—	—	—	
TDPIER_0	Initialized	—	—	—	—	—	
TDPCR2_0	Initialized	—	—	—	—	—	
TDPWDMN_0	Initialized	—	—	—	—	—	
TDPCNT_1	Initialized	—	—	—	—	—	TDP_1
TDPPDMX_1	Initialized	—	—	—	—	—	
TDPPDMN_1	Initialized	—	—	—	—	—	
TDPWDMX_1	Initialized	—	—	—	—	—	
TDPICR_1	Initialized	—	—	—	—	—	
TDPICRF_1	Initialized	—	—	—	—	—	
TDPCSR_1	Initialized	—	—	—	—	—	
TDPCR1_1	Initialized	—	—	—	—	—	

26.2 DC Characteristics

Table 26.2 lists the DC characteristics. Table 26.3 lists the permissible output currents. Table 26.4 lists the bus drive characteristics.

Table 26.2 DC Characteristics (1)

Conditions: V_{CC} = 3.0 V to 3.6 V, AV_{CC}*[1] = 3.0 V to 3.6 V, AVref*[1] = 3.0 V to AV_{CC}, V_{SS} = AV_{SS}*[1] = 0 V

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	P67 to P60, $\overline{IRQ7}$ to $\overline{IRQ0}$, $\overline{IRQ15}$ to $\overline{IRQ8}$	(1)	V_T^-	$V_{CC} \times 0.2$	—	—	V	
	$\overline{KIN7}$ to $\overline{KIN0}$, $\overline{KIN15}$ to $\overline{KIN8}$, $\overline{WUE15}$ to $\overline{WUE8}$		V_T^+	—	—	$V_{CC} \times 0.7$		
	$\overline{ExIRQ7}$ to $\overline{ExIRQ6}$, and $\overline{ExIRQ15}$ to $\overline{ExIRQ8}$		$V_T^+ - V_T^-$	$V_{CC} \times 0.05$	—	—		
Input high voltage	$\overline{RES}$, NMI, MD2, MD1, and $\overline{ETRST}$	(2)	V_{IH}	$V_{CC} \times 0.9$	—	$V_{CC} + 0.3$		
	EXTAL			$V_{CC} \times 0.7$	—	$V_{CC} + 0.3$		
	Port 7			$AV_{CC} \times 0.7$	—	$AV_{CC} + 0.3$		
	Ports A, G, I, PE4, PE2 to PE0, P97, P86, P52, and P42			$V_{CC} \times 0.7$	—	5.5		
	Input pins other than (1) and (2) above			$V_{CC} \times 0.7$	—	$V_{CC} + 0.3$		
Input low voltage	$\overline{RES}$, MD2, MD1, and $\overline{ETRST}$	(3)	V_{IL}	– 0.3	—	$V_{CC} \times 0.1$		
	NMI, EXTAL, and input pins other than (1) and (3) above			–0.3	—	$V_{CC} \times 0.2$		
Output high voltage	All output pins (except for ports A, G, I, P97, P86, P52, and P42)		V_{OH}	$V_{CC} – 0.5$	—	—		I_{OH} = –200 μA
				$V_{CC} – 1.0$	—	—		I_{OH} = –1 mA
	Ports A, G, I, P97, P86, P52, and P42*[2]			0.5	—	—		I_{OH} = - 200 μA
Output low voltage	All output pins *[3]		V_{OL}	—	—	0.4		I_{OL} = 1.6 mA
	Ports 1, 2, 3, C, and D			—	—	1.0		I_{OL} = 5 mA

Item		Symbol	Min.	Max.	Unit	Test Conditions
SCI	Input clock rise time	t_{SCKr}	—	1.5	t_{cyc}	Figure 26.20
	Input clock fall time	t_{SCKf}	—	1.5		
	Transmit data delay time (synchronous)	t_{TXD}	—	50	ns	Figure 26.21
	Receive data setup time (synchronous)	t_{RXS}	50	—		
	Receive data hold time (synchronous)	t_{RXH}	50	—		

Notes: 1. Applied only for the peripheral modules that are available during subclock operation.
2. Other than P52, P97, P86, P42, port A, port G, and port I.

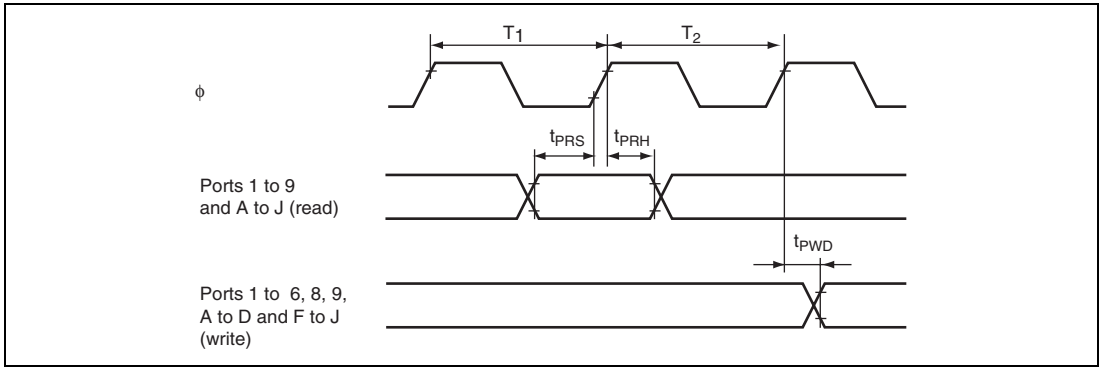

Figure 26.9 I/O Port Input/Output Timing

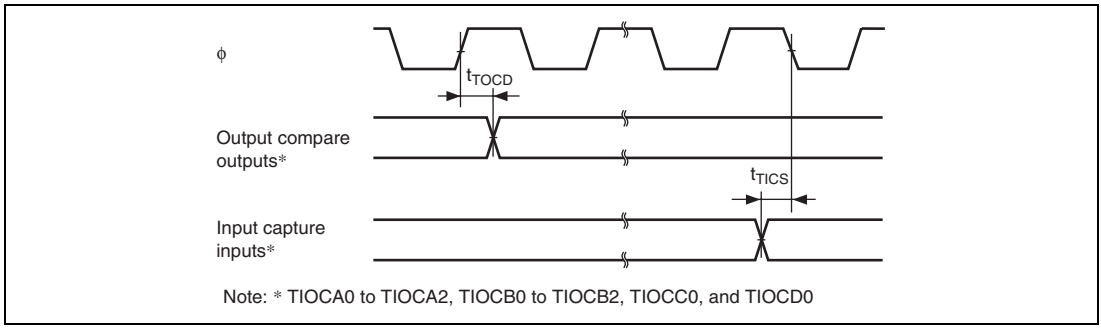

Figure 26.10 TPU Input/Output Timing

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