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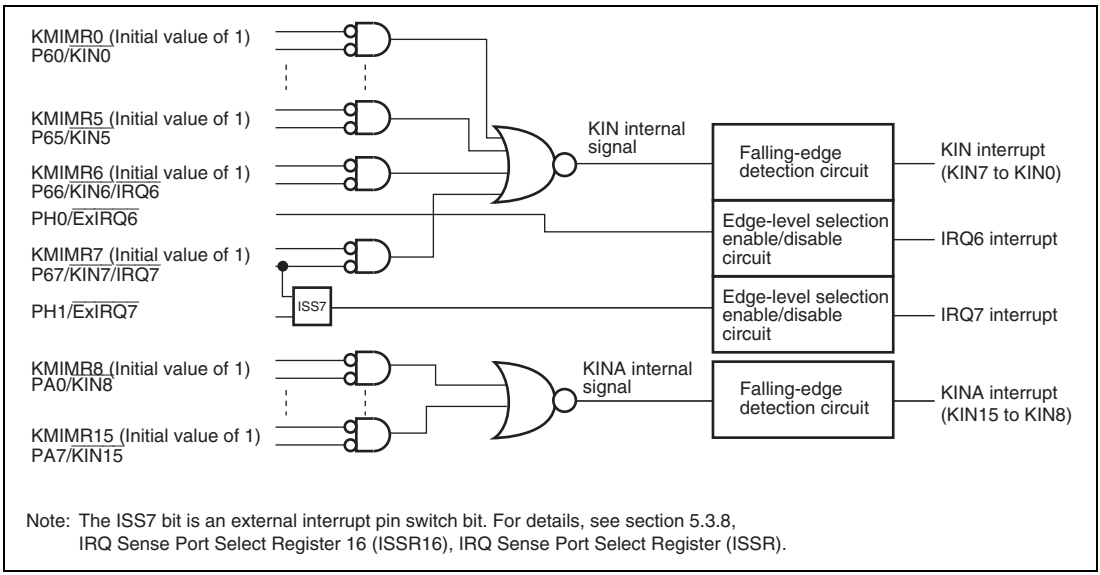
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8S/2600
Core Size	16-Bit
Speed	20MHz
Connectivity	FIFO, I²C, LPC, SCI, SmartCard
Peripherals	POR, PWM, WDT
Number of I/O	112
Program Memory Size	160KB (160K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	External
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	144-TQFP
Supplier Device Package	144-TQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2117vt20ihv

In H8S/2140B Group compatible vector mode, interrupt input from the $\overline{\text{IRQ7}}$ pin is ignored when even one of the KMIMR15 to KMIMR8 bits is cleared to 0. If the $\overline{\text{KIN7}}$ to $\overline{\text{KIN0}}$ pins or $\overline{\text{KIN15}}$ to $\overline{\text{KIN8}}$ pins are specified to be used as key-sensing interrupt input pins and wake-up event interrupt input pins, the interrupt sensing condition for the corresponding interrupt source (IRQ6 or IRQ7) must be set to low-level sensing or falling-edge sensing. Note that interrupt input cannot be made from the $\overline{\text{ExIRQ6}}$ pin.



Note: The ISS7 bit is an external interrupt pin switch bit. For details, see section 5.3.8, IRQ Sense Port Select Register 16 (ISSR16), IRQ Sense Port Select Register (ISSR).

Figure 5.3 Relation between IRQ7 and IRQ6 Interrupts, KIN15 to KIN0 Interrupts, KMIMR, and KMIMRA (Extended Vector Mode: EIVS = 1)

In extended vector mode, the initial value of the KMIMR6 bit is 1. Accordingly, it does not enable of disable the $\overline{\text{IRQ6}}$ pin interrupt. The interrupt input from the $\overline{\text{ExIRQ6}}$ pin becomes the IRQ6 interrupt request.

5.4.2 Internal Interrupt Sources

Internal interrupts issued from the on-chip peripheral modules have the following features:

- For each on-chip peripheral module there are flags that indicate the interrupt request status, and enable bits that individually select enabling or disabling of these interrupts. When the enable bit for a particular interrupt source is set to 1, an interrupt request is sent to the interrupt controller.
- The control level for each interrupt can be set by ICR.

5.5 Interrupt Exception Handling Vector Tables

Tables 5.4 and 5.5 list interrupt exception handling sources, vector addresses, and interrupt priorities. H8S/2140B Group compatible vector mode or extended vector mode can be selected for the vector addresses by the EIVS bit in system control register 3 (SYSCR3).

For default priorities, the lower the vector number, the higher the priority. Modules set at the same priority will conform to their default priorities. Priorities within a module are fixed.

An interrupt control level can be specified for a module to which an ICR bit is assigned. Interrupt requests from modules that are set to interrupt control level 1 (priority) by the interrupt control level and the I and UI bits in CCR are given priority and processed before interrupt requests from modules that are set to interrupt control level 0 (no priority).

Table 5.5 Interrupt Sources, Vector Addresses, and Interrupt Priorities (H8S/2140B Group Compatible Vector Mode)

Origin of Interrupt Source	Name	Vector Number	Vector Address	ICR	Priority
			Advanced Mode		
External pin	NMI	7	H'00001C	—	High
	IRQ0	16	H'000040	ICRA7	↑
	IRQ1	17	H'000044	ICRA6	
	IRQ2	18	H'000048	ICRA5	
	IRQ3	19	H'00004C		
	IRQ4	20	H'000050	ICRA4	
	IRQ5	21	H'000054		
	IRQ6, KIN7 to KIN0	22	H'000058	ICRA3	
	IRQ7, KIN15 to KIN8	23	H'00005C		Low

7.1 Register Descriptions

Table 7.2 lists each port registers.

Table 7.2 Register Configuration in Each Port

Port	Number of Pins	Registers									
		DDR	DR	PIN	PCR	KMPCR	ODR	NCE	NCMC	NCCS	NOCR
Port 1	8	O	O	O*[2]	O	—	—	—	—	—	—
Port 2	8	O	O	O*[2]	O	—	—	—	—	—	—
Port 3	8	O	O	O*[2]	O	—	—	—	—	—	—
Port 4	8	O	O	O*[2]	—	—	—	—	—	—	—
Port 5	3	O	O	O*[2]	—	—	—	—	—	—	—
Port 6	8	O	O	O*[2]	—	O	—	O	O	O	—
Port 7	8	—	—	O	—	—	—	—	—	—	—
Port 8	7	O	O	O*[2]	—	—	—	—	—	—	—
Port 9	8	O	O	O*[2]	O	—	—	—	—	—	—
Port A	8	O	—	O	—	—	O	—	—	—	—
Port B	8	O	—	O	O*[2]	—	O	—	—	—	—
Port C	8	O	—	O	O*[2]	—	O	O	O	O	O
Port D	8	O	—	O	O*[2]	—	O	—	—	—	O
Port E	5	—	—	O	—	—	—	—	—	—	—
Port F	8	O	—	O	O*[2]	—	O	—	—	—	O
Port G	8	O	—	O	—	—	O	O	O	O	O
Port H	6	O	—	O	O*[2]	—	O	—	—	—	O
Port I	8*[1]	O	—	O	—	—	O	—	—	—	O
Port J	8*[1]	O	—	O	O	—	O	—	—	—	O

[Legend]

O: Register exists

—: No register exists

Notes: 1. Not supported by TFP-144V and TLP-145V.

2. Valid only when the PORTS bit in the port control register 2 (PTCNT2) is 1.

9.4 Bus Master Interface

DACNT, DADRA, and DADRB are 16-bit registers. The data bus linking the bus master and the on-chip peripheral modules, however, is only 8 bits wide. When the bus master accesses these registers, it therefore uses an 8-bit temporary register (TEMP).

These registers are written to and read from as follows.

- Write

  When the upper byte is written to, the upper-byte write data is stored in TEMP. Next, when the lower byte is written to, the lower-byte write data and TEMP value are combined, and the combined 16-bit value is written in the register.

- Read

  When the upper byte is read from, the upper-byte value is transferred to the CPU and the lower-byte value is transferred to TEMP. Next, when the lower byte is read from, the lower-byte value in TEMP is transferred to the CPU.

These registers should always be accessed 16 bits at a time with a MOV instruction, and the upper byte should always be accessed before the lower byte. Correct data will not be transferred if only the upper byte or only the lower byte is accessed. Also note that a bit manipulation instruction cannot be used to access these registers.

Example 1: Write to DACNT

```
MOV.W R0, @DACNT      ; Write R0 contents to DACNT
```

Example 2: Read DADRA

```
MOV.W @DADRA, R0      ; Copy contents of DADRA to R0
```

Bit	Bit Name	Initial value	R/W	Description
3	TGFD	0	R/(W)*	Input Capture/Output Compare Flag D Status flag that indicates the occurrence of TGRD input capture or compare match in channel 0. In channels 1 and 2, bit 3 is reserved. It is always read as 0 and cannot be modified. [Setting conditions] • When TCNT = TGRD while TGRD is functioning as output compare register • When TCNT value is transferred to TGRD by input capture signal while TGRD is functioning as input capture register [Clearing condition] When 0 is written to TGFD after reading TGFD = 1
2	TGFC	0	R/(W)*	Input Capture/Output Compare Flag C Status flag that indicates the occurrence of TGRC input capture or compare match in channel 0. In channels 1 and 2, bit 2 is reserved. It is always read as 0 and cannot be modified. [Setting conditions] • When the TCNT = TGRC while TGRC is functioning as output compare register • When TCNT value is transferred to TGRC by input capture signal while TGRC is functioning as input capture register [Clearing condition] When 0 is written to TGFC after reading TGFC = 1

(b) When TGR is an input capture register

Figure 10.20 shows an operation example in which TGRA has been designated as an input capture register, and buffer operation has been designated for TGRA and TGRC. Counter clearing by TGRA input capture has been set for TCNT, and both rising and falling edges have been selected as the TIOCA pin input capture input edge. As buffer operation has been set, when the TCNT value is stored in TGRA upon occurrence of input capture A, the value previously stored in TGRA is simultaneously transferred to TGRC.

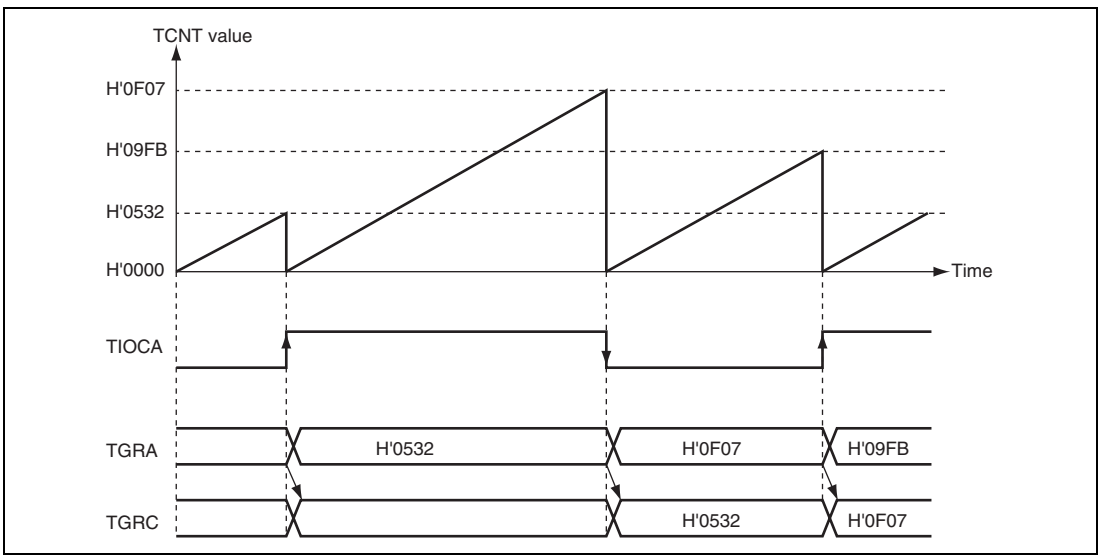


Figure 10.20 Example of Buffer Operation (2)

(1) Input Capture/Compare Match Interrupt

An interrupt is requested if the TGIE bit in TIER is set to 1 when the TGF flag in TSR is set to 1 by the occurrence of a TGR input capture/compare match on a particular channel. The interrupt request is cleared by clearing the TGF flag to 0. The TPU has 16 input capture/compare match interrupts, four each for channel 0, and two each for channels 1 and 2.

(2) Overflow Interrupt

An interrupt is requested if the TCIEV bit in TIER is set to 1 when the TCFV flag in TSR is set to 1 by the occurrence of TCNT overflow on a channel. The interrupt request is cleared by clearing the TCFV flag to 0. The TPU has three overflow interrupts, one for each channel.

(3) Underflow Interrupt

An interrupt is requested if the TCIEU bit in TIER is set to 1 when the TCFU flag in TSR is set to 1 by the occurrence of TCNT underflow on a channel. The interrupt request is cleared by clearing the TCFU flag to 0. The TPU has two underflow interrupts, one each for channels 1 and 2.

10.6.2 A/D Converter Activation

The A/D converter can be activated by the TGRA input capture/compare match for a channel. If the TTGE bit in TIER is set to 1 when the TGFA flag in TSR is set to 1 by the occurrence of a TGRA input capture/compare match on a particular channel, a request to start A/D conversion is sent to the A/D converter. If the TPU conversion start trigger has been selected on the A/D converter side at this time, A/D conversion is started. In the TPU, a total of three TGRA input capture/compare match interrupts can be used as A/D converter conversion start sources, one for each channel.

Section 11 16-Bit Cycle Measurement Timer (TCM)

This LSI has four channels on-chip 16-bit cycle measurement timers (TCM). Each TCM has a 16-bit counter that provides the basis for measuring the periods of input waveforms.

11.1 Features

- Capable of measuring the periods of input waveforms
- Sensed edge is selectable
- 16-bit compare match
- 16-bit resolution
- Selectable counter clock
  - Any of seven internal clocks or an external clock
- Five interrupt sources
  - Counter overflow
  - Cycle upper limit overflow
  - Cycle lower limit underflow
  - Compare match
  - Triggering of input capture

Table 15.8 Maximum Bit Rate with External Clock Input (Clocked Synchronous Mode)

φ (MHz)	External Input Clock (MHz)	Maximum Bit Rate (bit/s)	φ (MHz)	External Input Clock (MHz)	Maximum Bit Rate (bit/s)
8	1.3333	1333333.3	16	2.6667	2666666.7
10	1.6667	1666666.7	18	3.0000	3000000.0
12	2.0000	2000000.0	20	3.3333	3333333.3
14	2.3333	2333333.3			

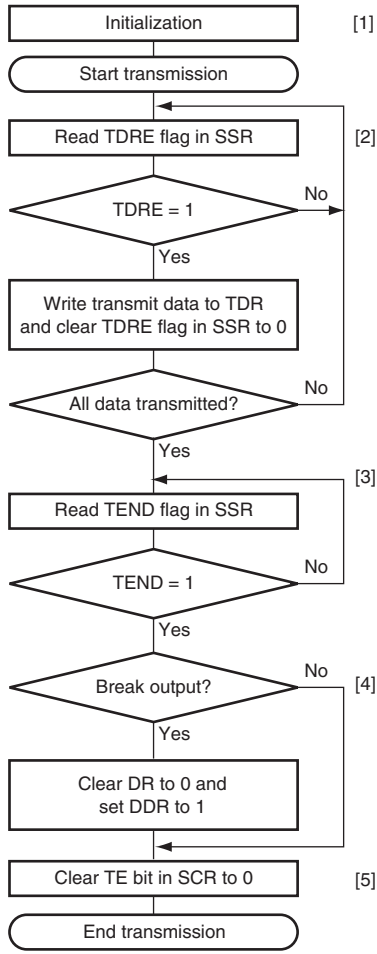
Table 15.9 BRR Settings for Various Bit Rates (Smart Card Interface Mode, n = 0, s = 372)

Bit Rate (bit/s)	Operating Frequency φ (MHz)											
	10.00			13.00			14.2848			16.00		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
9600	0	1	30	0	1	-8.99	0	1	0.00	0	1	12.01

Bit Rate (bit/s)	Operating Frequency φ (MHz)					
	18.00			20.00		
	n	N	Error (%)	n	N	Error (%)
9600	0	2	-15.99	0	2	-6.65

Table 15.10 Maximum Bit Rate for Each Frequency (Smart Card Interface Mode, S = 372)

φ (MHz)	Maximum Bit Rate (bit/s)	n	N	φ (MHz)	Maximum Bit Rate (bit/s)	n	N
10.00	13441	0	0	16.00	21505	0	0
13.00	17473	0	0	18.00	24194	0	0
14.2848	19200	0	0	20.00	26882	0	0



[1] SCI initialization:
The TxD pin is automatically designated as the transmit data output pin.
After the TE bit is set to 1, a frame of 1s is output, and transmission is enabled.

[2] SCI status check and transmit data write:
Read SSR and check that the TDRE flag is set to 1, then write transmit data to TDR and clear the TDRE flag to 0.

[3] Serial transmission continuation procedure:

To continue serial transmission, read 1 from the TDRE flag to confirm that writing is possible, then write data to TDR, and clear the TDRE flag to 0.

[4] Break output at the end of serial transmission:
To output a break in serial transmission, set DDR for the port corresponding to the TxD pin to 1, clear DR to 0, then clear the TE bit in SCR to 0.

Note: Do not write to SMR, SCR, BRR, and SDCR from the start to the end of transmission except the process of [5].

Figure 15.7 Sample Serial Transmission Flowchart

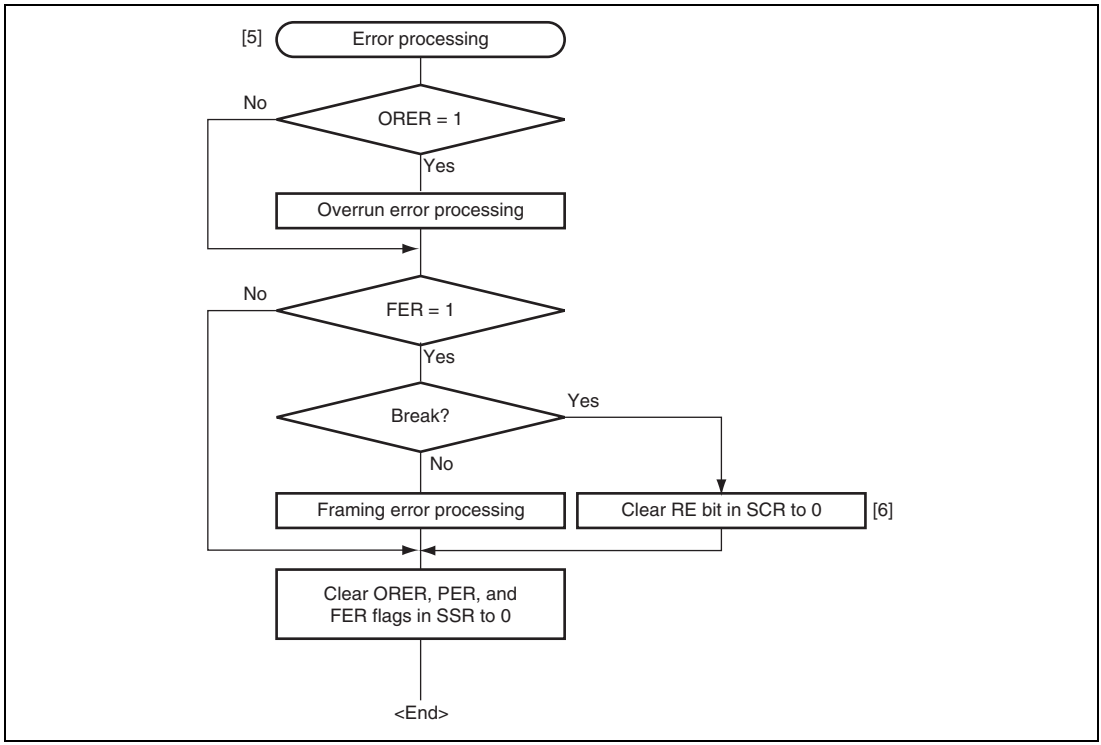


Figure 15.13 Sample Multiprocessor Serial Reception Flowchart (2)

16.3.8 FIFO Control Register (FFCR)

FFCR is a write-only register that controls transmit/receive FIFOs.

Bit	Bit Name	Initial Value	R/W	Description
7	RCVRTRIG1	0	W	Receive FIFO Interrupt Trigger Level 1, 0
6	RCVRTRIG0	0	W	These bits set the trigger level of the receive FIFO interrupt. 00: 1 byte 01: 4 bytes 10: 8 bytes 11: 14 bytes
5, 4	–	—	—	Reserved These bits cannot be modified.
3	DMAMODE	0	—	DMA Mode This bit is not supported and cannot be modified.
2	XMITFRST	0	W	Transmit FIFO Reset The transmit FIFO data is cleared when 1 is written. However, FTSR data is not cleared. This bit is automatically cleared.
1	RCVRFRST	0	W	Receive FIFO Reset The receive FIFO data is cleared when 1 is written. However, FRSR data is not cleared. This bit is automatically cleared.
0	FIFOE	0	W	FIFO Enable 0: Transmit/receive FIFOs disabled All bytes of these FIFOs are cleared. 1: Transmit/receive FIFOs enabled

(5) Data Reception

Figure 16.10 shows an example of the data reception flowchart.

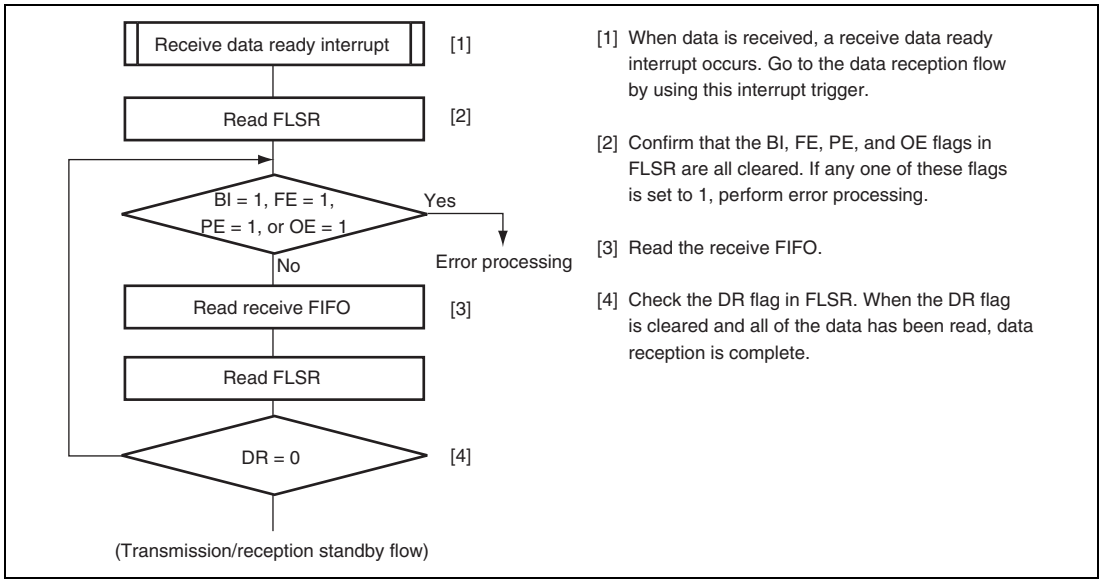


Figure 16.10 Example of Data Reception Flowchart

19.3.7 LPC Channel 3 Address Registers H and L (LADR3H and LADR3L)

LADR3 sets the LPC channel 3 host address and controls the operation of the bidirectional data registers. The contents of the address fields in LADR3 must not be changed while channel 3 is operating (while LPC3E is set to 1).

- LADR3H

			R/W		
Bit	**Bit Name**	**Initial Value**	**Slave**	**Host**	**Description**
7	Bit 15	0	R/W	—	Channel 3 Address Bits 15 to 8
6	Bit 14	0	R/W	—	Set the LPC channel 3 host address.
5	Bit 13	0	R/W	—	
4	Bit 12	0	R/W	—	
3	Bit 11	0	R/W	—	
2	Bit 10	0	R/W	—	
1	Bit 9	0	R/W	—	
0	Bit 8	0	R/W	—	

- LADR3L

			R/W		
Bit	**Bit Name**	**Initial Value**	**Slave**	**Host**	**Description**
7	Bit 7	0	R/W	—	Channel 3 Address Bits 7 to 3
6	Bit 6	0	R/W	—	Set the LPC channel 3 host address.
5	Bit 5	0	R/W	—	
4	Bit 4	0	R/W	—	
3	Bit 3	0	R/W	—	
2	—	0	R/W	—	Reserved The initial value should not be changed.
1	Bit 1	0	R/W	—	Channel 3 Address Bit 1 Sets the LPC channel 3 host address.
0	TWRE	0	R/W	—	Bidirectional Data Register Enable Enables or disables bidirectional data register operation. 0: TWR operation is disabled TWR-related I/O address match determination is halted 1: TWR operation is enabled

Bit	Bit Name	Initial Value	R/W	Description		
3	CH3	0	R/W	Channel Select 3 to 0		
2	CH2	0	R/W	Select analog input channels with the SCANE and SCANS bits in ADCRS.		
1	CH1	0	R/W			
0	CH0	0	R/W	The input channel setting must be made when conversion is halted (ADST = 0).		
				When SCANE = 0 and SCANS = X	When SCANE = 1 and SCANS = 0	When SCANE = 1 and SCANS = 1
				0000: AN0	0000: AN0	0000: AN0
				0001: AN1	0001: AN0, AN1	0001: AN0, AN1
				0010: AN2	0010: AN0 to AN2	0010: AN0 to AN2
				0011: AN3	0011: AN0 to AN3	0011: AN0 to AN3
				0100: AN4	0100: AN4	0100: AN0 to AN4
				0101: AN5	0101: AN4, AN5	0101: AN0 to AN5
				0110: AN6	0110: AN4 to AN6	0110: AN0 to AN6
				0111: AN7	0111: AN4 to AN7	0111: AN0 to AN7
				1000: AN8	1000: AN8	1000: AN8
				1001: AN9	1001: AN8, AN9	1001: AN8, AN9
				1010: AN10	1010: AN8 to AN10	1010: AN8 to AN10
				1011: AN11	1011: AN8 to AN11	1011: AN8 to AN11
				1100: AN12	1100: AN12	1100: AN8 to AN12
				1101: AN13	1101: AN12, AN13	1101: AN8 to AN13
				1110: AN14	1110: AN12 to AN14	1110: AN8 to AN14
				1111: AN15	1111: AN12 to AN15	1111: AN8 to AN15

[Legend]

X: Don't care

(1) On-Chip RAM Address Map when Programming/Erasing is Executed

Parts of the procedure program that is made by the user, like download request, programming/erasing procedure, and decision of the result, must be executed in the on-chip RAM. Since the on-chip program to be downloaded is embedded in the on-chip RAM, make sure the on-chip program and procedure program do not overlap. Figure 22.11 shows the area of the on-chip program to be downloaded.

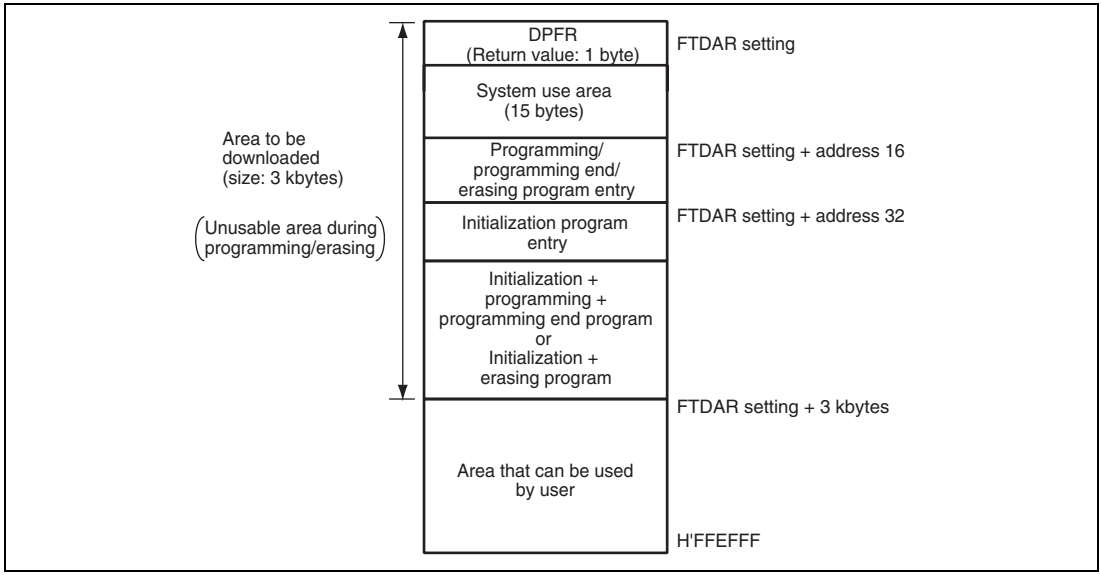


Figure 22.11 RAM Map when Programming/Erasing is Executed

8. All interrupts and the use of a bus master other than the CPU are disabled during programming/erasing. The specified voltage is applied for the specified time when programming or erasing. If interrupts occur or the bus mastership is moved to other than the CPU during programming/erasing, causing a voltage exceeding the specifications to be applied, the flash memory may be damaged. Therefore, interrupts are disabled by setting bit 7 (I bit) in the condition code register (CCR) to B'1 in interrupt control mode 0 and by setting bits 2 to 0 (I2 to I0 bits) in the extend register (EXR) to B'111 in interrupt control mode 2. Accordingly, interrupts other than NMI are held and not executed. Configure the user system so that NMI interrupts do not occur. The interrupts that are held must be executed after all programming completes.
9. FKEY must be set to H'5A and the user MAT must be prepared for programming.
10. The parameters required for programming are set. The start address of the programming destination on the user MAT (FMPAR parameter) is set in general register ER1. The start address of the program data storage area (FMPDR parameter) is set in general register ER0.
    - Example of FMPAR parameter setting: When an address other than one in the user MAT area is specified for the start address of the programming destination, even if the programming program is executed, programming is not executed and an error is returned to the FPFR parameter. Since the program data for one programming operation is 128 bytes, the lower eight bits of the address must be H'00 or H'80 to be aligned with the 128-byte boundary.
    - Example of FMPDR parameter setting: When the storage destination for the program data is flash memory, even if the programming routine is executed, programming is not executed and an error is returned to the FPFR parameter. In this case, the program data must be transferred to the on-chip RAM and then programming must be executed.
11. Programming is executed. The entry point of the programming program is at the address which is 16 bytes after #DLTOP (start address of the download destination specified by FTDAR). Call the subroutine to execute programming by using the following steps.

```
MOV.L    #DLTOP+16,ER2   ; Set entry address to ER2
JSR      @ER2            ; Call programming routine
NOP
```

    - The general registers other than R0L are held in the programming program.
    - R0L is a return value of the FPFR parameter.
    - Since the stack area is used in the programming program, a stack area of 128 bytes at the maximum must be allocated in RAM.
12. The return value in the programming program, the FPFR parameter is determined.
13. Determine whether programming of the necessary data has finished. If more than 128 bytes of data are to be programmed, update the FMPAR and FMPDR parameters in 128-byte units, and repeat steps 11 to 14. Increment the programming destination address by 128 bytes and update the programming data pointer correctly. If an address which has already been programmed is written to again, not only will a programming error occur, but also flash memory will be damaged.

22.8.3 User Boot Mode

This LSI has user boot mode that is initiated with different mode pin settings than those in boot mode or user program mode. User boot mode is a user-arbitrary boot mode, unlike boot mode that uses the on-chip SCI.

Only the user MAT can be programmed/erased in user boot mode. Programming/erasing of the user boot MAT is only enabled in boot mode or programmer mode.

(1) User Boot Mode Initiation

For the mode pin settings to start up user boot mode, see table 22.7.

When the reset start is executed in user boot mode, the built-in check routine runs. The user MAT and user boot MAT states are checked by this check routine.

While the check routine is running, NMI and all other interrupts cannot be accepted.

Next, processing starts from the execution start address of the reset vector in the user boot MAT. At this point, H'AA is set to FMATS because the execution target MAT is the user boot MAT.

(2) User MAT Programming in User Boot Mode

For programming the user MAT in user boot mode, additional processing made by setting FMATS is required: switching from user-boot-MAT selection state to user-MAT selection state, and switching back to user-boot-MAT selection state after programming completes.

Figure 22.14 shows the procedure for programming the user MAT in user boot mode.

(e) Division Ratio Inquiry

The boot program will return the supported division ratios in response to the inquiry.

Command

H'22

- Command, H'22, (one byte): Inquiry regarding division ratio

Response

H'32	Size	Number of types					
Number of division ratios	Division ratio	…					
…							
SUM							

- Response, H'32, (one byte): Response to the division ratio inquiry
- Size (one byte): The total amount of data that represents the number of types, the number of division ratios, and the division ratios
- Number of types (one byte): The number of supported divided clock types
  (e.g. when there are two divided clock types, which are the main and peripheral clocks, the number of types will be H'02.)
- Number of division ratios (one byte): The number of division ratios for each type
  (e.g. the number of division ratios to which the main clock can be set and the peripheral clock can be set.)
- Division ratio (one byte)

  Division ratio: The inverse of the division ratio, i.e. a negative number (e.g. when the clock is divided by two, the value of division ratio will be H'FE. H'FE = D'-2)

  The number of division ratios returned is the same as the number of division ratios and as many groups of data are returned as there are types.
- SUM (one byte): Checksum

Register Name	Abbreviation	Number of bits	Address	Module	Data Width	Access States
Flash key code register	FKEY	8	H'FEAC	ROM	8	2
Flash MAT select register	FMATS	8	H'FEAD	ROM	8	2
Flash transfer destination address register	FTDAR	8	H'FEAE	ROM	8	2
Timer start register	TSTR	8	H'FEB0	TPU common	8	2
Timer synchro register	TSYR	8	H'FEB1	TPU common	8	2
Keyboard control register 1_0	KBCR1_0	8	H'FEC0	PS2_0	8	2
Keyboard data buffer transmit data register_0	KBTR_0	8	H'FEC1	PS2_0	8	2
Keyboard control register 1_1	KBCR1_1	8	H'FEC2	PS2_1	8	2
Keyboard data buffer transmit data register_1	KBTR_1	8	H'FEC3	PS2_1	8	2
Keyboard control register 1_2	KBCR1_2	8	H'FEC4	PS2_2	8	2
Keyboard data buffer transmit data register_2	KBTR_2	8	H'FEC5	PS2_2	8	2
Timer XY control register	TCRXY	8	H'FEC6	TMR_XY	8	2
Timer control register_Y	TCR_Y	8	H'FEC8 (RELOCATE = 1)	TMR_Y	8	2
Timer control/status register_Y	TCSR_Y	8	H'FEC9 (RELOCATE = 1)	TMR_Y	8	2
Time constant register A_Y	TCORA_Y	8	H'FECA (RELOCATE = 1)	TMR_Y	8	2
Time constant register B_Y	TCORB_Y	8	H'FECB (RELOCATE = 1)	TMR_Y	8	2
Timer counter _Y	TCNT_Y	8	H'FECC (RELOCATE = 1)	TMR_Y	8	2
I^2C bus data register_1	ICDR_1	8	H'FECE (RELOCATE = 1)	IIC_1	8	2
Second slave address register_1	SARX_1	8	H'FECE (RELOCATE = 1)	IIC_1	8	2
I^2C bus mode register_1	ICMR_1	8	H'FECF (RELOCATE = 1)	IIC_1	8	2
Slave address register_1	SAR_1	8	H'FECF (RELOCATE = 1)	IIC_1	8	2