Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	H8S/2600
Core Size	16-Bit
Speed	20MHz
Connectivity	FIFO, I²C, LPC, SCI, SmartCard
Peripherals	POR, PWM, WDT
Number of I/O	112
Program Memory Size	160KB (160K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	External
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	144-TQFP
Supplier Device Package	144-TQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2117vt20v

Classification	Module/ Function	Description
Timer	8-bit PWM timer (PWMU)	• 8-bit timers A/B × six channels • Selectable from four clock sources • Cycle selectable for each channel • Supports 8-bit single pulse mode, 16-bit single pulse mode, and 8-bit pulse division mode.
	14-bit PWM timer (PWMX)	• 14 bits × two channels • Pulse division method • Selectable from sixteen operation clocks by combination of eight system clock cycles and two base cycles
	16-bit timer pulse unit (TPU)	• 16 bits × three channels • Selectable from eight counter input clocks for each channel • Maximum 8-pulse inputs/outputs • The following operations can be set. — Counter clear operation — Multiple timer counters (TCNT) can be written to simultaneously. — Simultaneous clearing by compare match and input capture possible — Register simultaneous input/output possible by counter synchronous operation — Maximum of 7-phase PWM output possible by combination with synchronous operation • Supports buffer operation and phase counting mode (two-phase encoder input) for some channels • Supports input capture function • Supports output compare function (waveform output at compare match)
	16-bit cycle measurement timer (TCM)	• 16 bits × four channels • Selectable from seven clocks: six internal clocks and one external clock • Capable of measuring the periods of input waveforms
	16-bit duty period measurement timer (TDP)	• 16 bits × three channels • Selectable from seven clocks: six internal clocks and one external clock • Capable of measuring the periods and pulse width of input waveforms

(7) PC1/$\overline{\text{WUE9}}$/TIOCB0

The pin function is switched as shown below according to the combination of the register setting of the TPU and the PC1DDR bit. When the WUEMR9 bit in WUEMR of the interrupt controller is cleared to 0, this pin can be used as the $\overline{\text{WUE9}}$ input pin.

This pin functions as TIOCB0 input when TPU channel 0 timer operating mode is set to normal operation or phase counting mode and IOB3 to IOB0 in TIORH_0 are set to B'10xx. (x: Don't care.)

		Setting	
		TPU	I/O Port
Module Name	Pin Function	TIOCB0_OE	PC1DDR
TPU	TIOCB0 output	1	—
I/O port	PC1 output	0	1
	PC1 input (initial setting)	0	0

(8) PC0/$\overline{\text{WUE8}}$/TIOCA0

The pin function is switched as shown below according to the combination of the register setting of the TPU and the PC0DDR bit. When the WUEMR8 bit in WUEMR of the interrupt controller is cleared to 0, this pin can be used as the $\overline{\text{WUE8}}$ input pin.

This pin functions as TIOCA0 input when TPU channel 0 timer operating mode is set to normal operation or phase counting mode and IOA3 to IOA0 in TIORH_0 are set to B'10xx. (x: Don't care.)

		Setting	
		TPU	I/O Port
Module Name	Pin Function	TIOCA0_OE	PC0DDR
TPU	TIOCA0 output	1	—
I/O port	PC0 output	0	1
	PC0 input (initial setting)	0	0

Section 10 16-Bit Timer Pulse Unit (TPU)

This LSI has an on-chip 16-bit timer pulse unit (TPU) that comprises three 16-bit timer channels. The function list of the 16-bit timer unit and its block diagram are shown in table 10.1 and figure 10.1, respectively.

10.1 Features

- Maximum 8-pulse input/output
- Selection of eight counter input clocks for channels 0 and 2, seven counter input clocks for channel 1
- The following operations can be set for each channel:
  - Waveform output at compare match
  - Input capture function
  - Counter clear operation
  - Multiple timer counters (TCNT) can be written to simultaneously
  - Simultaneous clearing by compare match and input capture possible
  - Register simultaneous input/output possible by counter synchronous operation
  - Maximum of 7-phase PWM output possible by combination with synchronous operation
- Buffer operation settable for channel 0
- Phase counting mode settable independently for each of channels 1 and 2
- Fast access via internal 16-bit bus
- 13 interrupt sources
- Automatic transfer of register data
- A/D converter conversion start trigger can be generated

Bit	Bit Name	Initial value	R/W	Description
3	TGFD	0	R/(W)*	Input Capture/Output Compare Flag D Status flag that indicates the occurrence of TGRD input capture or compare match in channel 0. In channels 1 and 2, bit 3 is reserved. It is always read as 0 and cannot be modified. [Setting conditions] • When TCNT = TGRD while TGRD is functioning as output compare register • When TCNT value is transferred to TGRD by input capture signal while TGRD is functioning as input capture register [Clearing condition] When 0 is written to TGFD after reading TGFD = 1
2	TGFC	0	R/(W)*	Input Capture/Output Compare Flag C Status flag that indicates the occurrence of TGRC input capture or compare match in channel 0. In channels 1 and 2, bit 2 is reserved. It is always read as 0 and cannot be modified. [Setting conditions] • When the TCNT = TGRC while TGRC is functioning as output compare register • When TCNT value is transferred to TGRC by input capture signal while TGRC is functioning as input capture register [Clearing condition] When 0 is written to TGFC after reading TGFC = 1

(b) Example of input capture operation

Figure 10.13 shows an example of input capture operation. In this example both rising and falling edges have been selected as the TIOCA pin input capture input edge, falling edge has been selected as the TIOCB pin input capture input edge, and counter clearing by TGRB input capture has been designated for TCNT.

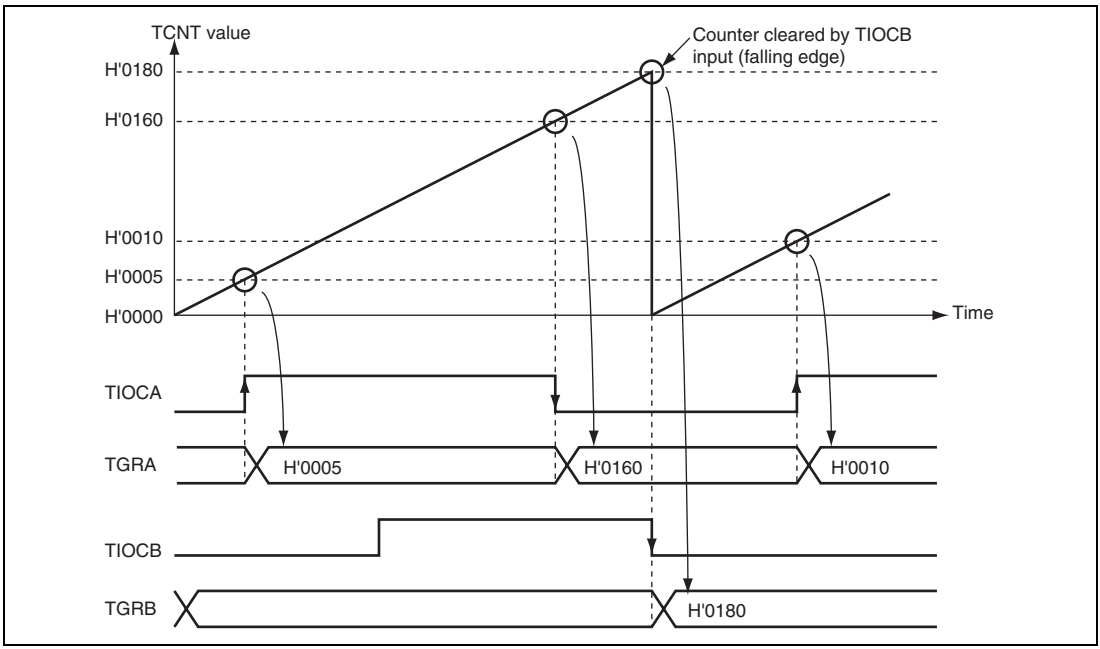

Figure 10.13 Example of Input Capture Operation

(3) TCFV Flag/TCFU Flag Setting Timing

Figure 10.40 shows the timing for setting of the TCFV flag in TSR by overflow occurrence, and TCIV interrupt request signal timing. Figure 10.41 shows the timing for setting of the TCFU flag in TSR by underflow occurrence, and TCIU interrupt request signal timing.

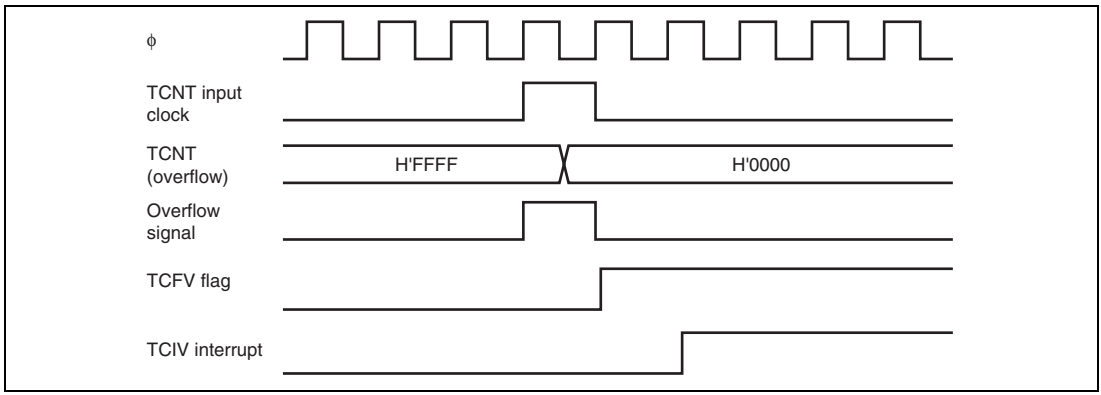

Figure 10.40 TCIV Interrupt Setting Timing

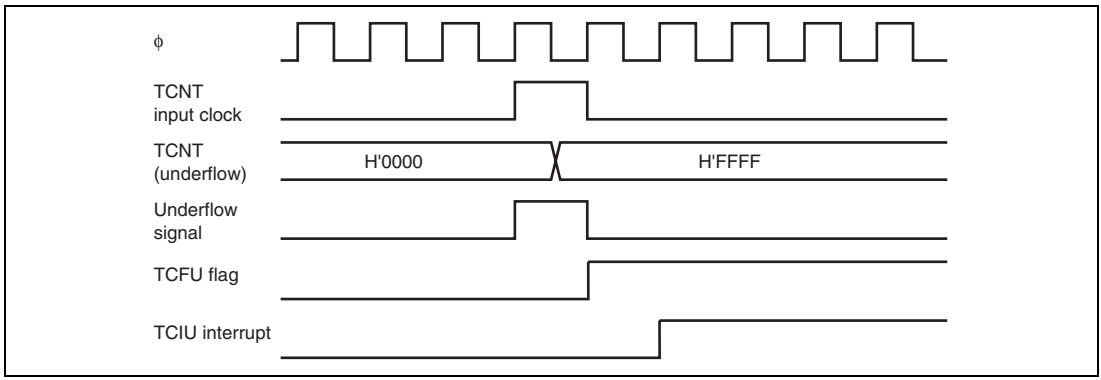

Figure 10.41 TCIU Interrupt Setting Timing

Bit	Bit Name	Initial Value	R/W	Description
4	IEDG	0	R/W	Input Edge Select In timer mode, selects the falling or rising edge of the TCMCYI input for use in input capture, in combination with the value of the POCTL bit. In cycle measurement mode, selects the falling or rising edge of the TCMCYI input for use in measurement, in combination with the value of the POCTL bit. POCTL = 0 0: Selects the rising edge of the TCMCYI input 1: Selects the falling edge of the TCMCYI input POCTL = 1 0: Selects the falling edge of the TCMCYI input 1: Selects the rising edge of the TCMCYI input
3	TCMMDS	0	R/W	TCM Mode Select Selects the TCM operating mode. 0: Timer mode The TCM provides compare match and input capture facilities. 1: Cycle measurement mode Setting this bit to 1 starts counting by TCMCNT. TCMCNT should be initialized to H'0000. Clear the CST in TCMCR to 0 before setting to cycle measurement mode.
2	CKS2	0	R/W	Clock Select 2, 1, 0
1	CKS1	0	R/W	Selects the clock signal for input to TCMCNT.
0	CKS0	0	R/W	Note: Modify this bit when CST = 0 and TCMMDS = 0 000: Count ϕ/2 internal clock 001: Count ϕ/8 internal clock 010: Count ϕ/16 internal clock 011: Count ϕ/32 internal clock 100: Count ϕ/64 internal clock 101: Count ϕ/128 internal clock 110: Count ϕ/256 internal clock 111: Count external clock (select the external clock edge with CKSEG in TCMCSR.)

12.3.10 TDP Control Register 2 (TDPCR2)

TDPCR2 selects cycle measurement mode and controls the TDPMCI input polarity.

Bit	Bit Name	Initial Value	R/W	Description
7	PMMS	0	R/W	Cycle Measurement Mode Select Selects whether to use the TDPMCI signal in cycle measurement mode. 0: The TDPMCI signal is not used (cycle measurement is always performed). 1: The TDPMCI signal is used (cycle measurement is performed only while the TDPMCI signal is high). Note: Change this bit when CST = 0 and TDPMDS = 0.
6	MCICTL	0	R/W	TDPMCI Input Polarity Inversion 0: TDPMCI input is used directly 1: TDPMCI input is inverted for use Note: Change this bit when CST = 0 and TDPMDS = 0.
5 to 1	—	All 0	R/W	Reserved The initial value should not be changed.
0	—	0	R	Reserved This bit is always read as 0 and cannot be modified.

15.4.3 Clock

Either an internal clock generated by the on-chip baud rate generator or an external clock input at the SCK pin can be selected as the SCI's transfer clock, according to the setting of the C/$\overline{A}$ bit in SMR and the CKE1 and CKE0 bits in SCR. When an external clock is input at the SCK pin, the clock frequency should be 16 times the bit rate used.

When the SCI is operated on an internal clock, the clock can be output from the SCK pin. The frequency of the clock output in this case is equal to the bit rate, and the phase is such that the rising edge of the clock is in the middle of the transmit data, as shown in figure 15.4.

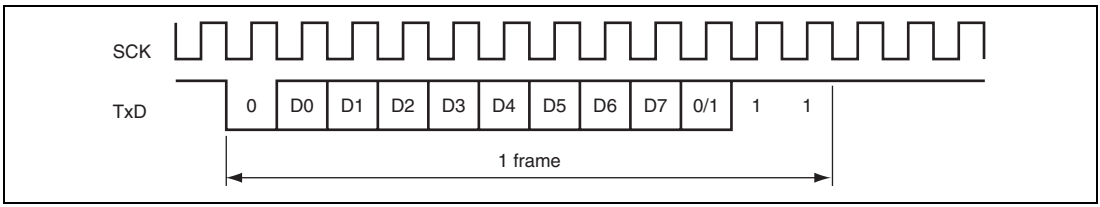

Figure 15.4 Relation between Output Clock and Transmit Data Phase (Asynchronous Mode)

Bit	Bit Name	Initial Value	R/W	Description
2	BC2	0	R/W	Bit Counter 2 to 0
1	BC1	0	R/W	These bits specify the number of bits to be transferred next. Bit BC2 to BC0 settings should be made during an interval between transfer frames. If bits BC2 to BC0 are set to a value other than 000, the setting should be made while the SCL line is low.
0	BC0	0	R/W	The bit counter is initialized to B'000 when a start condition is detected. The value returns to B'000 at the end of a data transfer.
				I²C Bus Format / Clocked Synchronous Serial Mode
				000: 9 bits / 000: 8 bits
				001: 2 bits / 001: 1 bit
				010: 3 bits / 010: 2 bits
				011: 4 bits / 011: 3 bits
				100: 5 bits / 100: 4 bits
				101: 6 bits / 101: 5 bits
				110: 7 bits / 110: 6 bits
				111: 8 bits / 111: 7 bits

19.3.19 Host Interface Select Register (HISEL)

HISEL selects the function of bits 7 to 4 in STR3 and selects the output of the host interrupt request signal of each frame.

Bit	Bit Name	Initial Value	R/W		Description
			Slave	Host	
7	SELSTR3	0	R/W	—	Status Register 3 Selection Selects the function of bits 7 to 4 in STR3 in combination with the TWRE bit in LADR3L. For details of STR3, see section 19.3.12, Status Registers 1 to 4 (STR1 to STR4). 0: Bits 7 to 4 in STR3 indicate processing status of the LPC interface. 1: [When TWRE = 1] Bits 7 to 4 in STR3 indicate processing status of the LPC interface. [When TWRE = 0] Bits 7 to 4 in STR3 are readable/writable bits which user can use as necessary
6	SELIRQ11	0	R/W	—	Host IRQ Interrupt Select These bits select the state of the output on the SERIRQ pins. 0: [When host interrupt request is cleared] SERIRQ pin output is in the Hi-Z state [When host interrupt request is set] SERIRQ pin output is low 1: [When host interrupt request is cleared] SERIRQ pin output is low [When host interrupt request is set] SERIRQ pin output is in the Hi-Z state.
5	SELIRQ10	0	R/W	—	
4	SELIRQ9	0	R/W	—	
3	SELIRQ6	0	R/W	—	
2	SELSMI	0	R/W	—	
1	SELIRQ12	1	R/W	—	
0	SELIRQ1	1	R/W	—	

Section 20 A/D Converter

This LSI includes one unit (unit 0) of successive-approximation-type 10-bit A/D converter that allows up to sixteen analog input channels to be selected. Figure 20.1 shows a block diagram for unit 0.

20.1 Features

- 10-bit resolution
- Input channels: Sixteen channels
- Conversion cycle: 40 cycles (A/D conversion clock)
- Two kinds of operating modes
  Single mode: Single-channel A/D conversion
  Scan mode: Continuous A/D conversion on one to four channels or continuous A/D conversion on one to eight channels
- A/D conversion clocks specifiable (ϕ, ϕ/2, ϕ/4, or ϕ/8)
- Eight data registers
  Conversion results are held in a 16-bit data register for each channel
- Sample and hold function
- Three kinds of A/D conversion start
  Software
  Conversion start trigger from 16-bit timer pulse unit (TPU) or 8-bit timer (TMR)
- Interrupt source
  A/D conversion end interrupt (ADI) request can be generated

20.2 Input/Output Pins

Table 20.1 summarizes the pins used by the A/D converter.

The AVCC and AVSS pins are the power supply pins for the analog block in the A/D converter. The AVref pin is a reference voltage pin for the A/D converter. The sixteen analog input pins are divided into two channel sets: analog input pins 0 to 7 (AN0 to AN7) comprising channel set 0 and analog input pins 8 to 15 (AN8 to AN15) comprising channel set 1.

Table 20.1 Pin Configuration

Pin Name	Symbol	I/O	Function
Analog power supply pin	AVCC	Input	Analog block power supply
Analog ground pin	AVSS	Input	Analog block ground
Reference power supply pin	AVref	Input	Reference voltage for A/D converter
Analog input pin 0	AN0	Input	Channel set 0 analog input
Analog input pin 1	AN1	Input	
Analog input pin 2	AN2	Input	
Analog input pin 3	AN3	Input	
Analog input pin 4	AN4	Input	
Analog input pin 5	AN5	Input	
Analog input pin 6	AN6	Input	
Analog input pin 7	AN7	Input	
Analog input pin 8	AN8	Input	Channel set 1 analog input
Analog input pin 9	AN9	Input	
Analog input pin 10	AN10	Input	
Analog input pin 11	AN11	Input	
Analog input pin 12	AN12	Input	
Analog input pin 13	AN13	Input	
Analog input pin 14	AN14	Input	
Analog input pin 15	AN15	Input	

22.7 Register Descriptions

The flash memory has the following registers and parameters.

Table 22.3 Register Configuration

Register Name	Abbreviation	R/W	Initial Value	Address	Data Bus Width
Flash code control status register	FCCS	R/W*	H'80	H'FEA8	8
Flash program code select register	FPCS	R/W	H'00	H'FEA9	8
Flash erase code select register	FECS	R/W	H'00	H'FEAA	8
Flash key code register	FKEY	R/W	H'00	H'FEAC	8
Flash MAT select register	FMATS	R/W	H'00	H'FEAD	8
Flash transfer destination address register	FTDAR	R/W	H'00	H'FEAE	8

Note: * Bits other than the SCO bit are read-only bits. The SCO bit is a write-only bit and is always read as 0.

Table 22.4 Parameter Configuration

Register Name	Abbreviation	R/W	Initial Value	Address	Data Bus Width
Download path fail result parameter	DPFR	R/W*	Undefined	On-chip RAM*	8, 16, 32
Flash path/fail parameter	FPFR	R/W	Undefined	R0L of CPU	8, 16, 32
Flash program/erase frequency parameter	FPEFEQ	R/W	Undefined	ER0 of CPU	8, 16, 32
Flash multipurpose address area parameter	FMPAR	R/W	Undefined	ER1 of CPU	8, 16, 32
Flash multipurpose data destination parameter	FMPDR	R/W	Undefined	ER0 of CPU	8, 16, 32
Flash erase block select parameter	FEBS	R/W	Undefined	ER0 of CPU	8, 16, 32

Note: * One byte of the start address on the on-chip RAM specified by FTDAR

(1) Download Pass and Fail Result Parameter (DPFR: Single Byte of Start Address in On-Chip RAM Specified by FTDAR)

DPFR indicates the return value of the download result. The DPFR value is used to determine the download result.

Bit	Bit Name	Initial Value	R/W	Description
7 to 3	—	—	—	Unused These bits return 0.
2	SS	—	R/W	Source Select Error Detect Only one type can be specified for the on-chip program which can be downloaded. When the program to be downloaded is not selected, more than two types of programs are selected, or a program which is not mapped is selected, an error occurs. 0: Download program selection is normal 1: Download program selection is abnormal
1	FK	—	R/W	Flash Key Register Error Detect Checks the FKEY value (H'A5) and returns the result. 0: FKEY setting is normal (H'A5) 1: FKEY setting is abnormal (value other than H'A5)
0	SF	—	R/W	Success/Fail Returns the download result. Reads back the program downloaded to the on-chip RAM and determines whether it has been transferred to the on-chip RAM. 0: Download of the program has ended normally (no error) 1: Download of the program has ended abnormally (error occurs)

(1) On-Chip RAM Address Map when Programming/Erasing is Executed

Parts of the procedure program that is made by the user, like download request, programming/erasing procedure, and decision of the result, must be executed in the on-chip RAM. Since the on-chip program to be downloaded is embedded in the on-chip RAM, make sure the on-chip program and procedure program do not overlap. Figure 22.11 shows the area of the on-chip program to be downloaded.

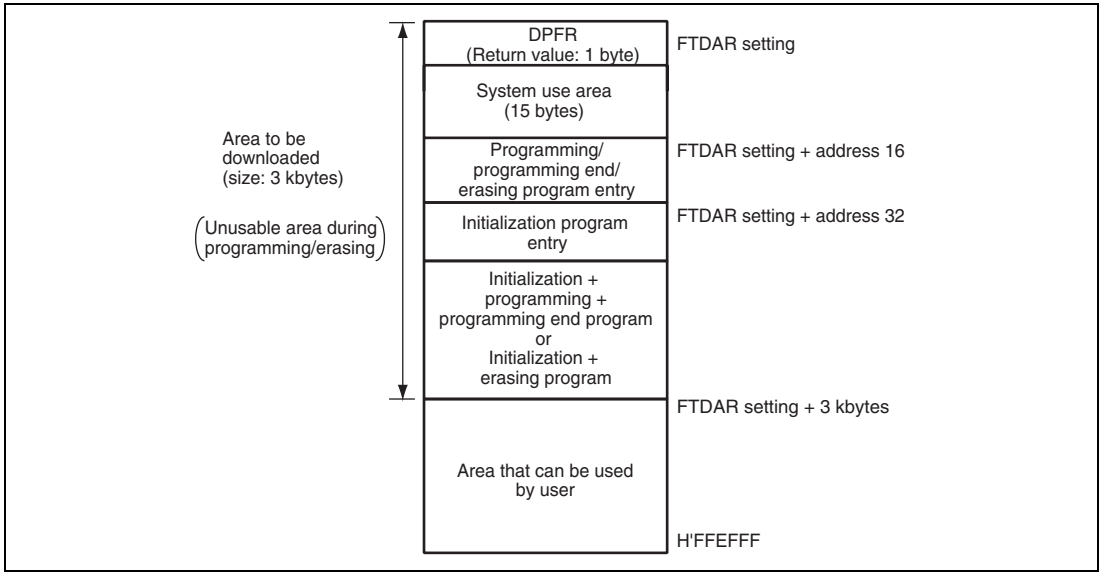

Figure 22.11 RAM Map when Programming/Erasing is Executed

Table 22.20 Error Codes

Code	Description
H'00	No error
H'11	Sum check error
H'12	Program size error
H'21	Device code mismatch error
H'22	Clock mode mismatch error
H'24	Bit rate selection error
H'25	Input frequency error
H'26	Division ratio error
H'27	Operating frequency error
H'29	Block number error
H'2A	Address error
H'2B	Data length error
H'51	Erasure error
H'52	Erasure incomplete error
H'53	Programming error
H'54	Selection processing error
H'80	Command error
H'FF	Bit-rate-adjustment confirmation error

24.1.2 Low-Power Control Register (LPWRCR)

LPWRCR controls power-down modes.

Bit	Bit Name	Initial Value	R/W	Description
7	DTON	0	R/W	Direct Transfer On Flag The initial value should not be changed.
6	LSON	0	R/W	Low-Speed On Flag The initial value should not be changed.
5	NESEL	0	R/W	Noise Elimination Sampling Frequency Select Selects the frequency by which the subclock (ϕSUB) input from the EXCL or ExEXCL pin is sampled using the clock (ϕ) generated by the system clock pulse generator. Clear this bit to 0 when ϕ is 5 MHz or more. The initial value should not be changed. 0: Sampling using ϕ/32 clock 1: Sampling using ϕ/4 clock (not allowed)
4	EXCLE	0	R/W	Subclock Input Enable Enables or disables subclock input from the EXCL or ExEXCL pin. 0: Disables subclock input from the EXCL or ExEXCL pin 1: Enables subclock input from the EXCL or ExEXCL pin
3 to 0	—	All 0	R/W	Reserved The initial value should not be changed.

Register Abbreviation	Reset	High-Speed/Medium speed	Watch	Sleep	Module Stop	Software Standby	Module
TCMCNT_2	Initialized	—	—	—	—	—	TCM_2
TCMMLCM_2	Initialized	—	—	—	—	—	
TCMICR_2	Initialized	—	—	—	—	—	
TCMICRF_2	Initialized	—	—	—	—	—	
TCMCSR_2	Initialized	—	—	—	—	—	
TCMCR_2	Initialized	—	—	—	—	—	
TCMIER_2	Initialized	—	—	—	—	—	
TCMMINCM_2	Initialized	—	—	—	—	—	
TCMCNT_3	Initialized	—	—	—	—	—	TCM_3
TCMMLCM_3	Initialized	—	—	—	—	—	
TCMICR_3	Initialized	—	—	—	—	—	
TCMICRF_3	Initialized	—	—	—	—	—	
TCMCSR_3	Initialized	—	—	—	—	—	
TCMCR_3	Initialized	—	—	—	—	—	
TCMIER_3	Initialized	—	—	—	—	—	
TCMMINCM_3	Initialized	—	—	—	—	—	
ADDRA	Initialized	—	Initialized	—	Initialized	Initialized	A/D converter
ADDRB	Initialized	—	Initialized	—	Initialized	Initialized	
ADDRC	Initialized	—	Initialized	—	Initialized	Initialized	
ADDRD	Initialized	—	Initialized	—	Initialized	Initialized	
ADDRE	Initialized	—	Initialized	—	Initialized	Initialized	
ADDRF	Initialized	—	Initialized	—	Initialized	Initialized	
ADDRG	Initialized	—	Initialized	—	Initialized	Initialized	
ADDRH	Initialized	—	Initialized	—	Initialized	Initialized	
ADCSR	Initialized	—	Initialized	—	Initialized	Initialized	
ADCR	Initialized	—	Initialized	—	Initialized	Initialized	

Table 26.3 Permissible Output Currents

Conditions: V_{CC} = 3.0 V to 3.6 V, V_{SS} = 0V

Item		Symbol	Min.	Typ.	Max.	Unit
Permissible output low current (per pin)	SCL0, SDA0, SCL1, SDA1, SCL2, SDA2, ExSCLA, ExSDAA, ExSCLB, ExSDAB, PS2AC to PS2DC, PS2AD to PS2DD, and PA7 to PA4 (bus drive function selected)	I_{OL}	—	—	8	mA
	Ports 1, 2, 3, C, and D		—	—	5	
	Other output pins		—	—	2	
Permissible output low current (total)	Total of ports 1, 2, 3, C, and D	ΣI_{OL}	—	—	40	
	Total of all output pins, including the above		—	—	60	
Permissible output high current (per pin)	All output pins	$-I_{OH}$	—	—	2	
Permissible output high current (total)	Total of all output pins	$\Sigma - I_{OH}$	—	—	30	

Notes: 1. To protect LSI reliability, do not exceed the output current values in table 26.3.
2. When driving a Darlington transistor or LED, always insert a current-limiting resistor in the output line, as show in figures 26.1 and 26.2.