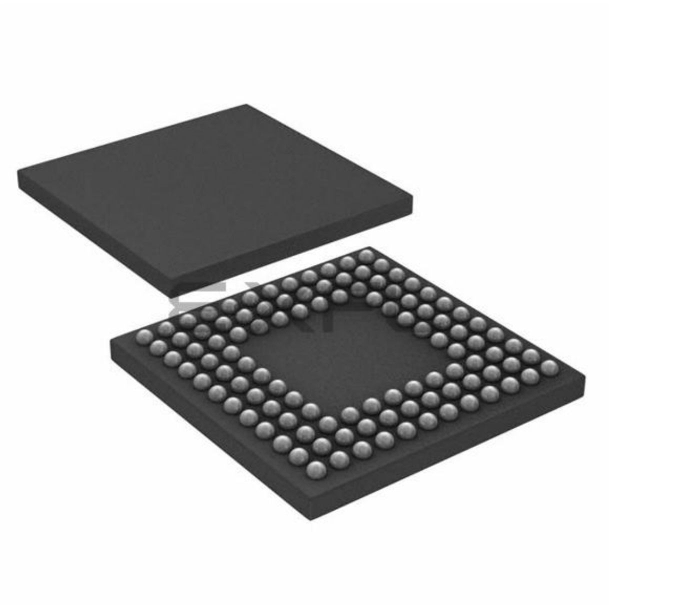

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	41.78MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	32
Program Memory Size	126KB (63K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 32
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 7x12b; D/A 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	108-LFBGA, CSPBGA
Supplier Device Package	108-CSPBGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aduc7121bbcz

ADUC7121* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

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- ADuC7121 QuickStart Plus Development System

DOCUMENTATION

Data Sheet

- ADuC7121: Precision Analog Microcontroller, 12-Bit Analog I/O, ARM7TDMI MCU Data Sheet

REFERENCE DESIGNS

- CN0153

REFERENCE MATERIALS

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- Integrated Route Taken to Pulse Oximetry
- Low Power, Low Cost, Wireless ECG Holter Monitor
- Part 1: Simplifying Design of Industrial Process-Control Systems with PLC Evaluation Boards
- Part 2: Simplifying Design of Industrial Process-Control Systems with PLC Evaluation Boards
- Precision Analog Microcontroller Simplifies Optical Transceiver Design

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Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Digital Power Supply Current					
IOV_{DD} Current in Normal Mode					Code executing from Flash/EE
		7		mA	CD = 7
		11		mA	CD = 3
		30	40	mA	CD = 0 (41.78 MHz clock)
IOV_{DD} Current in Pause Mode[4]		25		mA	CD = 0 (41.78 MHz clock)
IOV_{DD} Current in Sleep Mode[4]		100		µA	T_A = 25°C
Additional Power Supply Currents					
ADC		2.7		mA	@1 MSPS
IDAC		21		mA	All current DACs (IDACs) on
DAC		250		µA	per VDAC
ESD TESTS					2.5 V reference, T_A = 25°C
HBM Passed Up to			4	kV	
FICDM Passed Up to			0.5	kV	

[1] All ADC channel specifications are guaranteed during normal MicroConverter core operation.
[2] Apply to all ADC input channels.
[3] Measured using the factory set default values in the ADC offset register (ADCOF) and gain coefficient register (ADCGN).
[4] Not production tested but supported by design and/or characterization data on production release.
[5] Measured using the factory set default values in ADCOF and ADCGN with an external AD845 op amp as an input buffer stage as shown in Figure 24. Based on external ADC system components, the user may need to execute a system calibration to remove external endpoint errors and achieve these specifications (see the ADC section).
[6] The input signal can be centered on any dc common-mode voltage (V_{CM}) provided that this value is within the ADC voltage input range specified.
[7] V_{REF} calibration and trimming are performed under the following conditions: the core is operating in normal mode CD = 0, the ADC is on, the current DACs are on, and all VDACs are on. V_{REF} accuracy may vary under other operating conditions.
[8] The PVDD_IDAC0 pad voltage must be at least 300 mV greater than the IDAC0 pad voltage. These voltages are measured via the PVDD0 and IDAC0 channels of the ADC. This allows the IDAC0 pin to be pulled up to 1.7 V provided that this 300 mV differential voltage is maintained between the pads. This may require the PVDD_IDAC0 being supplied with a voltage greater than 2.0 V. The 2.1 V maximum PVDD_IDACx rating must not be exceeded.
[9] DAC linearity is calculated using a reduced code range of 100 to 3995.
[10] DAC gain error is calculated using a reduced code range of 100 to internal 2.5 V V_{REF}.
[11] Die temperature.
[12] Endurance is qualified as per JEDEC Standard 22 Method A117 and measured at −40°C, +25°C, +85°C, and +125°C.
[13] Retention lifetime equivalent at junction temperature (T_J) = 85°C as per JEDEC Standard 22 Method A117. Retention lifetime derates with junction temperature.
[14] Test carried out with a maximum of eight I/Os set to a low output level.
[15] Power supply current consumption is measured in normal, pause, and sleep modes under the following conditions: normal mode using a 3.6 V supply, pause mode using a 3.6 V supply, and sleep mode using 3.6 V supply.
[16] IOV_{DD} power supply current increases typically by 2 mA during a Flash/EE erase cycle.

ABSOLUTE MAXIMUM RATINGS

AGND = 0 V, T_A = 25°C, unless otherwise noted.

Table 8.

Parameter	Rating
AV_{DD} to IOV_{DD}	−0.3 V to +0.3 V
AGND to DGND	−0.3 V to +0.3 V
IOV_{DD} to IOGND, AV_{DD} to AGND	−0.3 V to +6 V
Digital Input Voltage to IOGND	−0.3 V to +5.3 V
Digital Output Voltage to IOGND	−0.3 V to IOV_{DD} + 0.3 V
V_{REF}_2.5 and V_{REF}_1.2 to AGND	−0.3 V to AV_{DD} + 0.3 V
Analog Inputs to AGND	−0.3 V to AV_{DD} + 0.3 V
Analog Outputs to AGND	−0.3 V to AV_{DD} + 0.3 V
Operating Temperature Range, Industrial	−10°C to +95°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
θ_{JA} Thermal Impedance	
108-Ball CSP_BGA	40°C/W
Peak Solder Reflow Temperature	
SnPb Assemblies (10 sec to 30 sec)	240°C
RoHS-Compliant Assemblies (20 sec to 40 sec)	260°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating can be applied at any one time.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Pin No.	Mnemonic	Type[1]	Description
A8	IDAC2	AO	IDAC2 Output. The output for this pin is 45 mA.
A7	PVDD_IDAC2	S	2.0 V Power for IDAC2.
C8	C_{DAMP}_IDAC2	AI	Damping Capacitor Pin for IDAC2.
A5	IDAC3	AO	IDAC3 Output. The output for this pin is 80 mA.
C5	PVDD_IDAC3	S	2.0 V Power for the IDAC3.
B4	C_{DAMP}_IDAC3	AI	Damping Capacitor for IDAC3.
A4	IDAC1	AO	IDAC1 Output. The output for this pin is 200 mA.
A1	IDAC1	AO	IDAC1 Output. The output for this pin is 200 mA.
A3	PVDD_IDAC1	S	Power for IDAC1.
A2	PVDD_IDAC1	S	Power for IDAC1.
B1	C_{DAMP}_IDAC1	AI	Damping Capacitor for IDAC1.
A12	IDAC0	AO	IDAC0 Output. The output for this pin is 250 mA.
A9	IDAC0	AO	IDAC0 Output. The output for this pin is 250 mA.
A11	PVDD_IDAC0	S	Power for IDAC0.
A10	PVDD_IDAC0	S	Power for IDAC0.
B12	C_{DAMP}_IDAC0	AI	Damping Capacitor Pin for IDAC0.
B11	IDAC_TST	AI/O	IDAC Test Purposes.
B10	PGND	S	Power Ground.
B9	PGND	S	Power Ground.
M1	AGND	S	Analog Ground.
M6	AGND	S	Analog Ground.
L1	AVDD	S	Analog Supply (3.3 V).
M7	AVDD	S	Analog Supply (3.3 V).
M12	AGND	S	Analog Ground.
B6	AGND	S	Analog Ground.
L12	AVDD	S	Analog Supply (3.3 V).
C7	AVDD	S	Analog Supply (3.3 V).
B7	AVDD_IDAC	S	Output of 2.5 V LDO regulator for internal IDACs. A 470 nF capacitor to AGND must be connected to this pin.
G1	DVDD	S	Output of 2.6 V On-Chip LDO Regulator. A 470 nF capacitor to DGND must be connected to this pin.
G12	DVDD	S	Output of 2.6 V On-Chip LDO Regulator. A 470 nF capacitor to DGND must be connected to this pin.
F1	DGND	S	Digital Ground.
F12	DGND	S	Digital Ground.
H1	IOVDD	S	3.3 V GPIO Supply.
J1	IOGND	S	3.3 V GPIO Ground.
H12	IOVDD	S	3.3 V GPIO Supply.
J12	IOGND	S	3.3 V GPIO Ground.
G2	XTALO	DO	Crystal Oscillator Inverter Output. If an external crystal is not being used, this pin can remain unconnected.
H2	XTALI	DI	Crystal Oscillator Inverter Input and Internal Clock Generator Circuits Input. If an external crystal is not being used, connect this pin to the DGND system ground.
F10	TCK	DI	JTAG Test Port Input, Test Clock. Debug and download access.
E10	TMS	DI	JTAG Test Port Input, Test Mode Select. Debug and download access.

[1] A is analog, D is digital, I is input, O is output, and S is supply, NC is no connect.

TERMINOLOGY

ADC SPECIFICATIONS

Integral Nonlinearity

Integral nonlinearity (INL) is the maximum deviation of any code from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, a point ½ LSB below the first code transition, and full scale, a point ½ LSB above the last code transition.

Differential Nonlinearity

Differential nonlinearity (DNL) is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error

Offset error is the deviation of the first code transition (0000 . . . 000) to (0000 . . . 001) from the ideal, that is, +½ LSB.

Gain Error

Gain error is the deviation of the last code transition from the ideal AIN voltage (full scale − 1.5 LSB) after the offset error has been adjusted out.

Signal to (Noise + Distortion) Ratio

Signal to (noise + distortion) ratio, or SINAD, is the measured ratio of signal to (noise + distortion) at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the rms sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc.

The ratio is dependent on the number of quantization levels in the digitization process: the more levels there are, the smaller the quantization noise becomes.

The theoretical SINAD ratio for an ideal N-bit converter with a sine wave input is given by

$$\textit{Signal to (Noise + Distortion)} = (6.02\,N + 1.76)\text{ dB}$$

Thus, for a 12-bit converter, this is 74 dB.

Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the rms sum of the harmonics to the fundamental.

DAC SPECIFICATIONS

Relative Accuracy

Otherwise known as endpoint linearity, relative accuracy is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero error and full-scale error.

Voltage Output Settling Time

This is the amount of time it takes the output to settle to within a one LSB level for a full-scale input change.

ADC CIRCUIT OVERVIEW

The analog-to-digital converter (ADC) incorporates a fast, multichannel, 12-bit ADC. It can operate from a 3.0 V to 3.6 V supply and is capable of providing a throughput of up to 1 MSPS when the clock source is 41.78 MHz. This block provides the user with a multichannel multiplexer, a differential track-and-hold, an on-chip reference, and an ADC.

The ADC consists of a 12-bit successive approximation converter based around two capacitor DACs. Depending on the input signal configuration, the ADC can operate in one of the following three modes:

- Fully differential mode, for small and balanced signals.
- Single-ended mode, for any single-ended signals.
- Pseudo differential mode, for any single-ended signals, taking advantage of the common-mode rejection offered by the pseudo differential input.

The converter accepts an analog input range of 0 V to V_{REF} when operating in single-ended mode or pseudo differential mode. In fully differential mode, the input signal must be balanced around a common-mode voltage (V_{CM}) in the range of 0 V to AV_{DD} and with a maximum amplitude of 2 V_{REF} (see Figure 12).

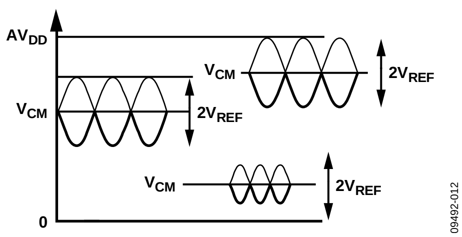

Figure 12. Examples of Balanced Signals for Fully Differential Mode

A high precision, low drift, and factory calibrated 2.5 V reference is provided on chip. An external reference can also be connected as described in the Band Gap Reference section.

Single or continuous conversion modes can be initiated in the software. An external $ADC\overline{\text{CONVST}}$ pin, an output generated from the on-chip PLA, a Timer0, or a Timer1 overflow can also be used to generate a repetitive trigger for ADC conversions.

If the signal has not been deasserted by the time the ADC conversion is complete, a second conversion begins automatically. A voltage output from an on-chip band gap reference proportional to absolute temperature can also be routed through the front-end ADC multiplexer, effectively creating an additional ADC channel input. This facilitates an internal temperature sensor channel, measuring die temperature to an accuracy of ±3°C.

The ADuC7121 is modified in a way that differentiates its ADC structure from other devices in the ADuC702x family.

The PADC0x and PADC1x inputs connect to a PGA and allow for a gain from 1 to 5 with 32 steps. The remaining channels can be configured as single ended or differential. A buffer is provided before the ADC for measuring internal channels.

ADC TRANSFER FUNCTION

Pseudo Differential and Single-Ended Modes

For both pseudo differential and single-ended modes, the input range is 0 to V_{REF}. In addition, the output coding is straight binary in both pseudo differential and single-ended modes with

1 LSB = *FS*/4096, or 2.5 V/4096 = 0.61 mV, or 610 µV when V_{REF} = 2.5 V

The ideal code transitions occur midway between successive integer LSB values (that is, 1/2 LSB, 3/2 LSBs, 5/2 LSBs, …, FS – 3/2 LSBs). The ideal input/output transfer characteristic is shown in Figure 13.

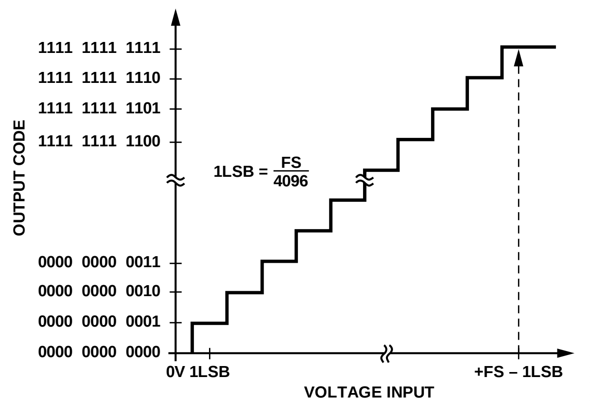

Figure 13. ADC Transfer Function in Pseudo Differential Mode or Single-Ended Mode

Fully Differential Mode

The amplitude of the differential signal is the difference between the signals applied to the V_{IN+} and V_{IN-} inputs (that is, $V_{IN+} - V_{IN-}$). Therefore, the maximum amplitude of the differential signal is $-V_{REF}$ to $+V_{REF}$ p-p (2 × V_{REF}). This is regardless of the common mode (CM). The common mode is the average of the two signals ($V_{IN+} + V_{IN-}$)/2, and is, therefore, the voltage that the two inputs are centered on, which results in the span of each input being CM ± V_{REF}/2. This voltage must be set up externally, and its range varies with V_{REF} (see the Driving the Analog Inputs section).

The output coding is twos complement in fully differential mode with

1 LSB = 2 V_{REF}/4096 or 2 × 2.5 V/4096 = 1.22 mV when V_{REF} = 2.5 V

The output result is ±11 bits, but this is shifted by one bit to the right. This allows the result in ADCDAT to be declared as a signed integer when writing C code. The designed code transitions occur midway between successive integer LSB values (that is,

POWER SUPPLY MONITOR

The power supply monitor on the ADuC7121 indicates when the IOVDD supply pin drops below one of two supply trip points. The monitor function is controlled via the PSMCON register. If enabled in the IRQEN or FIQEN register, the monitor interrupts the core using the PSMI bit in the PSMCON MMR. This bit is cleared immediately after CMP goes high. Note that if the interrupt generated is exited before CMP goes high (IOVDD supply voltage is above the trip point), no further interrupts are generated until CMP returns high. The user needs to ensure that the code execution remains within the ISR until CMP returns high.

This monitor function allows the user to save working registers to avoid possible data loss due to low supply or brownout conditions. It also ensures that normal code execution does not resume until a safe supply level has been established.

The PSM does not operate correctly when using JTAG debug; therefore, disable PSM while in JTAG debug mode.

Table 40. PSMCON MMR Bit Designations (Address = 0xFFFF0440, Default Value = 0x0008)

Bit	Name	Description
15:4	Reserved	These bits are reserved.
3	CMP	Comparator bit. This is a read-only bit that directly reflects the state of the comparator. Read 1 indicates that the IOVDD supply is above its selected trip point or the PSM is in power-down mode. Read 0 indicates the IOVDD supply is below its selected trip point. Set this bit before leaving the interrupt service routine.
2	TP	Trip point selection bit. 0 = 2.79 V. 1 = 3.07 V.
1	PSMEN	Power supply monitor enable bit. Set to 1 by the user to enable the power supply monitor circuit. Cleared to 0 by the user to disable the power supply monitor circuit.
0	PSMI	Power supply monitor interrupt bit. This bit is set high by the MicroConverter if CMP is low, indicating low I/O supply. The PSMI bit can be used to interrupt the processor. When CMP returns high, the PSMI bit can be cleared by writing a 1 to this location. A write of 0 has no effect. There is no timeout delay. PSMI can be cleared immediately after CMP goes high.

Table 41. FEE0PRO and FEE0HID MMR Bit Designations

Bit	Description
31	Read protection. Cleared by the user to protect Block 0. Set by the user to allow reading Block 0.
30:0	Write protection for Page 123 to Page 0. Each bit protects a group of 4 pages. Cleared by the user to protect the pages when writing to flash. Thus preventing an accidental write to specific pages in flash. Set by the user to allow writing the pages.

Command Sequence for Executing a Mass Erase

```
FEE0DAT = 0x3CFF;
FEE0ADR = 0xFFC3;
FEE0MOD = FEE0MOD|0x8;  //Erase key enable
FEE0CON = 0x06;         //Mass erase command
```

FEE1DAT Register

FEE1DAT is a 16-bit data register.

Name: FEE1DAT

Address: 0xFFFF0E8C

Default value: 0xXXXX

Access: Read and write

FEE1ADR Register

FEE1ADR is a 16-bit address register.

Name: FEE1ADR

Address: 0xFFFF0E90

Default value: 0x0000

Access: Read and write

FEE1SGN Register

FEE1SGN is a 24-bit code signature.

Name: FEE1SGN

Address: 0xFFFF0E98

Default value: 0xFFFFFF

Access: Read only

FEE1PRO Register

FEE1PRO provides protection following subsequent reset MMR. It requires a software key (see Table 42).

Name: FEE1PRO

Address: 0xFFFF0E9C

Default value: 0x00000000

Access: Read and write

FEE1HID Register

FEE1HID provides immediate protection MMR. It does not require any software keys (see Table 42).

Name: FEEHID

Address: 0xFFFF0EA0

Default value: 0xFFFFFFFF

Access: Read and write

Table 42. FEE1PRO and FEE1HID MMR Bit Designations

Bit	Description
31	Read protection. Cleared by the user to protect Block 1. Set by the user to allow reading Block 1.
30	Write protection for Page 127 to Page 120. Cleared by the user to protect the pages when writing to flash. Thus preventing an accidental write to specific pages in flash. Set by the user to allow writing the pages.
29:0	Write protection for Page 119 to Page 0. Each bit protects a group of 4 pages. Cleared by the user to protect the pages when writing to flash. Thus preventing an accidental write to specific pages in flash. Set by the user to allow writing the pages.

FEE0STA Register

Name: FEE0STA

Address: 0xFFFF0E00

Default value: 0x0001

Access: Read and write

FEE1STA Register

Name: FEE1STA

Address: 0xFFFF0E80

Default value: 0x0000

Access: Read and write

Table 43. FEExSTA MMR Bit Designations

Bit	Description
15:6	Reserved.
5	Reserved.
4	Reserved.
3	Flash/EE interrupt status bit. Set automatically when an interrupt occurs, that is, when a command is complete and the Flash/EE interrupt enable bit in the FEExMOD register is set. Cleared when reading FEExSTA register.
2	Flash/EE controller busy. Set automatically when the controller is busy. Cleared automatically when the controller is not busy.

Reset Operation

There are four types of reset: external reset, power-on reset, watchdog expiration, and software force. The RSTSTA register indicates the source of the last reset and RSTCLR clears the RSTSTA register. These registers can be used during a reset exception service routine to identify the source of the reset. If RSTSTA is null, the reset was external. Note that when clearing RSTSTA, all bits that are currently set to 1 must be cleared. Otherwise, a reset event occurs.

The RSTCFG register allows different peripherals to retain their state after a watchdog or software reset.

Table 47. Remap MMR Bit Designations (Address = 0xFFFF0220, Default Value = 0x00)

Bit	Name	Description
0	Remap	Remap bit. Set by the user to remap the SRAM to Address 0x00000000. Cleared automatically after reset to remap the Flash/EE memory to Address 0x00000000.

Table 48. RSTSTA MMR Bit Designations (Address = 0xFFFF0230, Default Value = 0x0X)

Bit	Description
7:3	Reserved.
2	Software reset. Set by the user to force a software reset. Cleared by setting the corresponding bit in RSTCLR.
1	Watchdog timeout. Set automatically when a watchdog timeout occurs. Cleared by setting the corresponding bit in RSTCLR.
0	Power-on reset. Set automatically when a power-on reset occurs. Cleared by setting the corresponding bit in RSTCLR.

RSTCFGKEY0 Register

Name: RSTCFGKEY0

Address: 0xFFFF0248

Default value: 0xXX

Access Write

RSTCFGKEY1 Register

Name: RSTCFGKEY1

Address: 0xFFFF0250

Default value: 0xXX

Access: Write

Table 49. RSTCFG Write Sequence

Name	Code
RSTCFGKEY0	0x76
RSTCFG	User value
RSTCFGKEY1	0xB1

Table 50. RSTCFG MMR Bit Designations (Address = 0xFFFF024C, Default Value = 0x00)

Bit	Description
7:4	Reserved. Always set to 0.
3	This bit is set to 1 to configure the IDAC outputs to retain their state after a watchdog or software reset. This bit is cleared for the IDAC output pins and registers to return to their default state.
2	This bit is set to 1 to configure the DAC outputs to retain their state after a watchdog or software reset. This bit is cleared for the DAC output pins and registers to return to their default state.
1	Reserved. Always set to 0.
0	This bit is set to 1 to configure the GPIO pins to retain their state after a watchdog or software reset. This bit is cleared for the GPIO pins and registers to return to their default state.

Table 75. GPIO Pin Function Designations

Port	Pin	Configuration (See GPxCON Table 76)			
		00	01	10	11
0	P0.0	GPIO	SCL0		PLAI[5]
	P0.1	GPIO	SDA0	JTAG disabled	PLAI[4]
	P0.2	GPIO	SPICLK	JTAG disabled ADC_{BUSY}	PLAO[13]
	P0.3	GPIO	MISO	SYNC (PWM)	PLAO[12]
	P0.4	GPIO	MOSI	TRIP (PWM)	PLAI[11]
	P0.5	GPIO	$\overline{CS}$	$ADC_{\overline{CONVST}}$	PLAI[10]
	P0.6	GPIO	$\overline{MRST}$		PLAI[2]
	P0.7	GPIO	$\overline{TRST}$		PLAI[3]
1	P1.0	GPIO	SIN	SCL1	PLAI[7]
	P1.1	GPIO	SOUT	SDA1	PLAI[6]
	P1.2[1]	TDI (JTAG)			PLAO[15]
	P1.3[1]	TDO (JTAG)			PLAO[14]
	P1.4	GPIO	PWM1	ECLK/XCLK	PLAI[8]
	P1.5	GPIO	PWM2		PLAI[9]
	P1.6	GPIO			PLAO[5]
	P1.7	GPIO			PLAO[4]
2	P2.0	GPIO/IRQ0			PLAI[13]
	P2.1	GPIO/IRQ1			PLAI[12]
	P2.2	GPIO			PLAI[1]
	P2.3	GPIO/IRQ2			PLAI[14]
	P2.4	GPIO	PWM5		PLAO[7]
	P2.5	GPIO	PWM6		PLAO[6]
	P2.6	GPIO/IRQ3			PLAI[15]
	P2.7	GPIO			PLAI[0]
3	P3.0	GPIO			PLAO[0]
	P3.1	GPIO			PLAO[1]
	P3.2	GPIO/IRQ4	PWM3		PLAO[2]
	P3.3	GPIO/IRQ5	PWM4		PLAO[3]
	P3.4	GPIO			PLAO[8]
	P3.5	GPIO			PLAO[9]
	P3.6	GPIO			PLAO[10]
	P3.7	GPIO/$\overline{BM}$			PLAO[11]

[1] Reconfiguring these pins disables JTAG mode. Erase part to reenable JTAG access after changing default value.

Bit	Name	Description
4	I2CSRxFO	Slave Rx FIFO overflow. This bit is set to 1 when a byte is written to the Rx FIFO when it is already full. This bit is cleared in all other conditions.
3	I2CSRXQ	I^2C slave receive request bit. This bit is set to 1 when the Rx FIFO of the slave is not empty. This bit causes an interrupt to occur if the I2CSRXENI bit in I2CxSCTL is set. The Rx FIFO must be read or flushed to clear this bit.
2	I2CSTXQ	I^2C slave transmit request bit. This bit is set to 1 when the slave receives a matching address followed by a read. If the I2CSETEN bit in I2CxSCTL is = 0, this bit goes high just after the negative edge of SCL during the read bit transmission. If the I2CSETEN bit in I2CxSCTL is = 1, this bit goes high just after the positive edge of SCL during the read bit transmission. This bit causes an interrupt to occur if the I2CSTXENI bit in I2CxSCTL is set. This bit is cleared in all other conditions.
1	I2CSTFE	I^2C slave FIFO underflow status bit. This bit is high if the Tx FIFO is empty when a master requests data from the slave. This bit asserts at the rising edge of SCL during the read bit. This bit clears in all other conditions.
0	I2CETSTA	I^2C slave early transmit FIFO status bit. If the I2CSETEN bit in I2CxSCTL is = 0, this bit goes high if the slave Tx FIFO is empty. If the I2CSETEN bit in I2CxSCTL is = 1, this bit goes high just after the positive edge of SCL during the write bit transmission. This bit asserts once only for a transfer. This bit is cleared after being read.

I²C COMMON REGISTERS

I²C FIFO Status Registers

These 16-bit MMRs contain the status of the Rx/Tx FIFOs in both master and slave modes.

Name: I2C0FSTA

Address: 0xFFFF08CC

Default value: 0x0000

Access: Read and write

Name: I2C1FSTA

Address: 0xFFFF094C

Default value: 0x0000

Access: Read and write

Table 98. I2CxFSTA MMR Bit Designations

Bit	Name	Description
15:10		Reserved bits.
9	I2CFMTX	Set this bit to 1 to flush the master Tx FIFO.
8	I2CFSTX	Set this bit to 1 to flush the slave Tx FIFO.
7:6	I2CMRXSTA	I²C master receive FIFO status bits. [00] = FIFO empty. [01] = byte written to FIFO. [10] = one byte in FIFO. [11] = FIFO full.
5:4	I2CMTXSTA	I²C master transmit FIFO status bits. [00] = FIFO empty. [01] = byte written to FIFO. [10] = one byte in FIFO. [11] = FIFO full.
3:2	I2CSRXSTA	I²C slave receive FIFO status bits. [00] = FIFO empty. [01] = byte written to FIFO. [10] = one byte in FIFO. [11] = FIFO full.
1:0	I2CSTXSTA	I²C slave transmit FIFO status bits. [00] = FIFO empty. [01] = byte written to FIFO. [10] = one byte in FIFO. [11] = FIFO full.

PROGRAMMABLE LOGIC ARRAY (PLA)

The ADuC7121 integrates a fully programmable logic array (PLA) that consists of two independent but interconnected PLA blocks. Each block consists of eight PLA elements, giving each part a total of 16 PLA elements.

Each PLA element contains a dual input lookup table that can be configured to generate any logic output function based on two inputs and a flip-flop. This is represented in Figure 37.

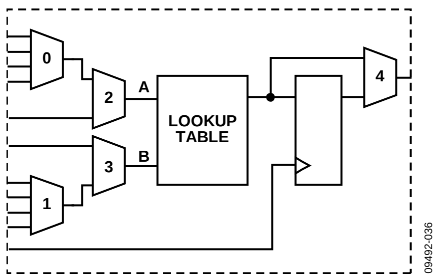

Figure 37. PLA Element

In total, 32 GPIO pins are available on each ADuC7121 for the PLA. These include 16 input pins and 16 output pins, which need to be configured in the GPxCON register as PLA pins before using the PLA. Note that the comparator output is also included as one of the 16 input pins, and that the JTAG TDI and TDO pins are included as PLA outputs. If you want to use JTAG programming or debugging, then you cannot use the JTAG TDI and TDO pins as PLA outputs.

The PLA is configured via a set of user MMRs. The output(s) of the PLA can be routed to the internal interrupt system, to the $ADC_{\overline{CONVST}}$ signal of the ADC, to an MMR, or to any of the 16 PLA output pins.

The two blocks can be interconnected as follows:

- Output of Element 15 (Block 1) can be fed to Input 0 of Mux 0 of Element 0 (Block 0).
- Output of Element 7 (Block 0) can be fed to the Input 0 of Mux 0 of Element 8 (Block 1).

Table 101. Element Input/Output

PLA Block 0			PLA Block 1		
Element	**Input**	**Output**	**Element**	**Input**	**Output**
0	P2.7	P3.0	8	P1.4	P3.4
1	P2.2	P3.1	9	P1.5	P3.5
2	P0.6	P3.2	10	P0.5	P3.6
3	P0.7	P3.3	11	P0.4	P3.7
4	P0.1	P1.7	12	P2.1	P0.3
5	P0.0	P1.6	13	P2.0	P0.2
6	P1.1	P2.5	14	P2.3	P1.3
7	P1.0	P2.4	15	P2.6	P1.2

PLADOUT Register

PLADOUT is a data output MMR for PLA. This register is always updated.

Name: PLADOUT

Address: 0xFFFF0B50

Default value: 0x00000000

Access: Read only

Table 109. PLADOUT MMR Bit Descriptions

Bit	Description
31:16	Reserved.
15:0	Output bit from Element 15 to Element 0.

PLALCK Register

PLALCK is a PLA lock option. Bit 0 is written only once. When set, it does not allow modifying any of the PLA MMRs, except PLADIN. A PLA tool is provided in the development system to easily configure the PLA.

Name: PLALCK

Address: 0xFFFF0B54

Default value: 0x00

Access: Write only

Bit	Value	Name	Description
5:4	11	IRQ2SRC[1:0]	External IRQ2 triggers on falling edge.
	10		External IRQ2 triggers on rising edge.
	01		External IRQ2 triggers on low level.
	00		External IRQ2 triggers on high level.
3:2	11	IRQ1SRC[1:0]	External IRQ1 triggers on falling edge.
	10		External IRQ1 triggers on rising edge.
	01		External IRQ1 triggers on low level.
	00		External IRQ1 triggers on high level.
1:0	11	IRQ0SRC[1:0]	External IRQ0 triggers on falling edge.
	10		External IRQ0 triggers on rising edge.
	01		External IRQ0 triggers on low level.
	00		External IRQ0 triggers on high level.

IRQCLRE Register

Name: IRQCLRE

Address: 0xFFFF0038

Default value: 0x00000000

Access: Read and write

Table 122. IRQCLRE MMR Bit Designations

Bit	Name	Description
31:25	Reserved	These bits are reserved and should not be written to.
24	IRQ5CLRI	A 1 must be written to this bit in the IRQ5 interrupt service routine to clear an edge triggered IRQ5 interrupt.
24	IRQ4CLRI	A 1 must be written to this bit in the IRQ4 interrupt service routine to clear an edge triggered IRQ4 interrupt.
23	Reserved	This bit is reserved.
22	IRQ3CLRI	A 1 must be written to this bit in the IRQ3 interrupt service routine to clear an edge triggered IRQ3 interrupt.
21	IRQ2CLRI	A 1 must be written to this bit in the IRQ2 interrupt service routine to clear an edge triggered IRQ2 interrupt.
20	IRQ1CLRI	A 1 must be written to this bit in the IRQ1 interrupt service routine to clear an edge triggered IRQ1 interrupt.
19	IRQ0CLRI	A 1 must be written to this bit in the IRQO interrupt service routine to clear an edge triggered IRQ0 interrupt.
18:0	Reserved	These bits are reserved and should not be written to.

Table 125. Timer0 Interface MMRs

Name	Description
T0LD	16-bit register that holds the 16-bit value loaded into the counter. Available only in 16-bit mode.
T0CAP	16-bit register that holds the 16-bit value captured by an enabled IRQ event. Available only in 16-bit mode.
T0VAL0/T0VAL1	T0VAL0 is a 16-bit register that holds the 16 least significant bits (LSBs). T0VAL1 is a 32-bit register that holds the 32 most significant bits (MSBs). T0VAL0 and T0VAL1 are read only. In 16-bit mode, 16-bit T0VAL0 is used. In 48-bit mode, both 16-bit T0VAL0 and 32-bit T0VAL1 are used.
T0ICLR	8-bit register. Writing any value to this register clears the interrupt. Available only in 16-bit mode.
T0CON	Configuration MMR.

Timer0 Value Registers

T0VAL0 and T0VAL1 are 16-bit and 32-bit registers that hold the 16 least significant bits and 32 most significant bits, respectively. T0VAL0 and T0VAL1 are read-only registers. In 16-bit mode, 16-bit T0VAL0 is used. In 48-bit mode, both 16-bit T0VAL0 and 32-bit T0VAL1 are used.

Name: T0VAL0

Address: 0xFFFF0304

Default value: 0x0000

Access: Read only

Name: T0VAL1

Address: 0xFFFF0308

Default value: 0x00000000

Access: Read only

Timer0 Capture Register

This is a 16-bit register that holds the 16-bit value captured by an enabled IRQ event; available in 16-bit mode only.

Name: T0CAP

Address: 0xFFFF0314

Default value: 0x0000

Access: Read only

Timer0 Control Register

This 17-bit MMR configures the mode of operation of Timer0.

Name: T0CON

Address: 0xFFFF030C

Default value: 0x00000000

Access: Read and write

Table 126. T0CON MMR Bit Designations

Bit	Value	Description
31:18		Reserved.
17		Event select bit. Set by the user to enable time capture of an event. Cleared by the user to disable time capture of an event.
16:12		Event select range, 0 to 16. The events are described in the introduction to the Timers section.
11		Reserved.
10:9		Clock select.
	00	Internal 32 kHz oscillator.
	01	UCLK.
	10	External 32 kHz crystal.
	11	HCLK.
8		Count up. Available in 16-bit mode only. Set by the user for Timer0 to count up. Cleared by the user for Timer0 to count down (default).
7		Timer0 enable bit. Set by the user to enable Timer0. Cleared by the user to disable Timer0 (default).
6		Timer0 mode. Set by the user to operate in periodic mode. Cleared by the user to operate in free-running mode (default).
5		Reserved.
4		Timer0 mode of operation.
	0	16-bit operation (default).
	1	48-bit operation.
3:0		Prescaler.
	0000	Source clock divide-by-1 (default).
	0100	Source clock divide-by-16.
	1000	Source clock divide-by-256.
	1111	Source clock divide-by-32,768.

Table 128. T1CON MMR Bit Designations

Bit	Value	Description
31:24		8-bit postscaler.
23		Enable write to postscaler.
22:20		Reserved.
19		Postscaler compare flag.
18		T1 interrupt generation selection flag.
17		Event select bit. Set by the user to enable time capture of an event. Cleared by the user to disable time capture of an event.
16:12		Event select range, 0 to 16. The events are as described in the introduction to the Timers section.
11:9		Clock select.
	000	Internal 32 kHz oscillator (default).
	001	Core clock.
	010	UCLK.
	011	P0.6. of the P0.6/$\overline{\text{MRST}}$/PLAI[2] pin.
8		Count up. Set by the user for Timer1 to count up. Cleared by the user for Timer1 to count down (default).
7		Timer1 enable bit. Set by the user to enable Timer1. Cleared by the user to disable Timer1 (default).
6		Timer1 mode. Set by the user to operate in periodic mode. Cleared by the user to operate in free-running mode (default).
5:4		Format.
	00	Binary (default).
	01	Reserved.
	10	Hr:Min:Sec:Hundredths: 23 hours to 0 hour.
	11	Hr:Min:Sec:Hundredths: 255 hours to 0 hour.
3:0		Prescaler.
	0000	Source clock divide-by-1 (default).
	0100	Source clock divide-by-16.
	1000	Source clock divide-by-256.
	1111	Source clock divide-by-32,768.

TIMER4—GENERAL-PURPOSE TIMER

Timer4 is a 32-bit general-purpose timer, count down or count up, with a programmable prescaler. The prescaler source can be the 32 kHz oscillator, the core clock, or PLL undivided output. This source can be scaled by a factor of 1, 16, 256, or 32,768. This gives a minimum resolution of 42 ns when operating at CD zero, the core is operating at 41.78 MHz, and with a prescaler of 1 (ignoring external GPIO).

The counter can be formatted as a standard 32-bit value or as hours:minutes:seconds:hundredths.

Timer4 has a capture register (T4CAP), which can be triggered by a selected IRQ's source initial assertion. Once triggered, the current timer value is copied to T4CAP, and the timer keeps running. This feature can be used to determine the assertion of an event with increased accuracy.

Timer4 interface consists of five MMRS.

- T4LD, T4VAL and T4CAP are 32-bit registers and hold 32-bit unsigned integers. T4VAL and T4CAP are read only.
- T4ICLR is an 8-bit register. Writing any value to this register clears the Timer1 interrupt.
- T4CON is the configuration MMR.
- Note that if the part is in a low power mode, and Timer4 is clocked from the GPIO or oscillator source then, Timer4 continues to operate.

Timer4 reloads the value from T4LD either when Timer4 overflows, or immediately when T4ICLR is written.

Timer4 Load Registers

T4LD is a 32-bit register, which holds the 32-bit value that is loaded into the counter.

Name: T4LD

Address: 0xFFFF0380

Default value: 0x00000000

Access: Read and write

Timer4 Clear Register

This 8-bit, write-only MMR is written (with any value) by user code to refresh (reload) Timer4.

Name: T4CLRI

Address: 0xFFFF038C

Default value: 0x00

Access: Write only

Timer4 Value Register

T4VAL is a 32-bit register that holds the current value of Timer4.

Name: T4VAL

Address: 0xFFFF0384

Default value: 0x00000000

Access: Read only

Timer4 Capture Register

This is a 32-bit register that holds the 32-bit value captured by an enabled IRQ event.

Name: T4CAP

Address: 0xFFFF0390

Default value: 0x00000000

Access: Read only

Timer4 Control Register

This 32-bit MMR configures the mode of operation of Timer4.

Name: T4CON

Address: 0xFFFF0388

Default value: 0x0000

Access: Read and write

CLOCK OSCILLATOR

The clock source for the ADuC7121 can be generated by the internal PLL or by an external clock input. To use the internal PLL, connect a 32.768 kHz parallel resonant crystal between XTALI and XTALO, and connect a capacitor from each pin to ground as shown Figure 46. This crystal allows the PLL to lock correctly to give a frequency of 41.78 MHz. If no external crystal is present, the internal oscillator is used to give a frequency of 41.78 MHz ± 3% typically.

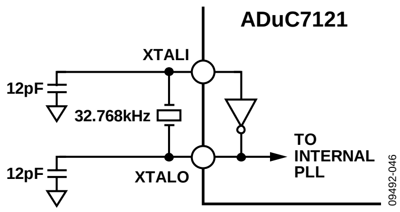

Figure 46. External Parallel Resonant Crystal Connections

To use an external source clock input instead of the PLL (see Figure 47), Bit 1 and Bit 0 of PLLCON must be modified. The external clock uses P1.4 and XCLK.

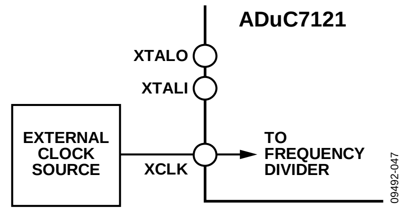

Figure 47. Connecting an External Clock Source

Using an external clock source, the ADuC7121 specified operational clock speed range is 50 kHz to 41.78 MHz ± 1% to ensure correct operation of the analog peripherals and Flash/EE.

NOTES