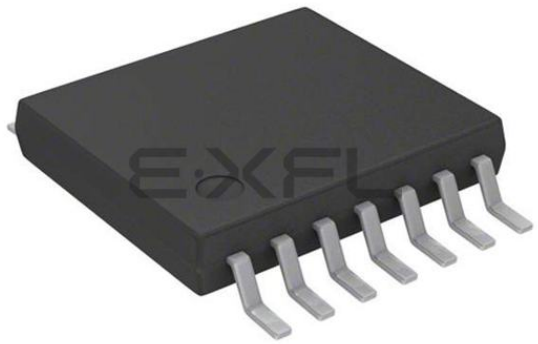

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Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	12
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 11x10b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	14-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	14-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f18326-i-st

Pin Allocation Tables

TABLE 2: 14/16-PIN ALLOCATION TABLE (PIC16(L)F18326)

I/O(2)	14-Pin PDIP/SOIC/TSSOP	16-Pin UQFN	ADC	Reference	Comparator	NCO	DAC	DSM	Timers	CCP	PWM	CWG	MSSP	EUSART	CLC	CLKR	Interrupt	Pull-up	Basic
RA0	13	12	ANA0	—	C1IN0+	—	DAC1OUT	—	—	—	—	—	$\overline{SS2}$(1)	—	—	—	IOC	Y	ICDDAT/ ICSPDAT
RA1	12	11	ANA1	VREF+	C1IN0- C2IN0-	—	DAC1REF+	—	—	—	—	—	—	—	—	—	IOC	Y	ICDCLK/ ICSPCLK
RA2	11	10	ANA2	VREF-	—	—	DAC1REF-	—	T0CKI(1)	CCP3(1)	—	CWG1IN(1) CWG2IN(1)	—	—	—	—	INT(1) IOC	Y	—
RA3	4	3	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IOC	Y	$\overline{MCLR}$ VPP
RA4	3	2	ANA4	—	—	—	—	—	T1G(1) SOSCO	—	—	—	—	—	—	—	IOC	Y	CLKOUT OSC2
RA5	2	1	ANA5	—	—	—	—	—	T1CKI(1) SOSCIN SOSCI	—	—	—	—	—	CLCIN3(1)	—	IOC	Y	CLKIN OSC1
RC0	10	9	ANC0	—	C2IN0+	—	—	—	T5CKI(1)	—	—	—	SCK1(1) SCL1(1,3,4)	—	—	—	IOC	Y	—
RC1	9	8	ANC1	—	C1IN1- C2IN1-	—	—	—	—	CCP4(1)	—	—	SDI1(1) SDA1(1,3,4)	—	CLCIN2(1)	—	IOC	Y	—
RC2	8	7	ANC2	—	C1IN2- C2IN2-	—	—	MDCIN1(1)	—	—	—	—	—	—	—	—	IOC	Y	—
RC3	7	6	ANC3	—	C1IN3- C2IN3-	—	—	MDMIN(1)	T5G(1)	CCP2(1)	—	—	$\overline{SS1}$(1)	—	CLCIN0(1)	—	IOC	Y	—
RC4	6	5	ANC4	—	—	—	—	—	T3G(1)	—	—	—	SCK2(1) SCL2(1,3,4)	—	CLCIN1(1)	—	IOC	Y	—
RC5	5	4	ANC5	—	—	—	—	MDCIN2(1)	T3CKI(1)	CCP1(1)	—	—	SDI2(1) SDA2(1,3,4)	RX(1)	—	—	IOC	Y	—
VDD	1	16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VDD

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.
2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.
3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.
4: These pins are configured for I^2C logic levels; clock and data signals may be assigned to any of these pins. Assignments to the other pins (e.g., RA5) will operate, but logic levels will be standard TTL/ ST as selected by the INLVL register.

TABLE 1-2: PIC16(L)F18326 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
RA0/ANA0/C1IN0+/DAC1OUT/ $\overline{SS2}$(1)/ ICDDAT/ICSPDAT	RA0	TTL/ST	CMOS	General purpose I/O.
	ANA0	AN	—	ADC Channel A0 input.
	C1IN0+	AN	—	Comparator C1 positive input.
	DAC1OUT	—	AN	Digital-to-Analog Converter output.
	$\overline{SS2}$	TTL/ST	—	Slave Select 2 input.
	ICDDAT	TTL/ST	CMOS	In-Circuit Debug Data I/O.
	ICSPDAT	TTL/ST	CMOS	ICSP™ Data I/O.
RA1/ANA1/VREF+/C1IN0-/ C2IN0-/DAC1REF+/ ICDCLK/ ICSPCLK	RA1	TTL/ST	CMOS	General purpose I/O.
	ANA1	AN	—	ADC Channel A1 input.
	VREF+	AN	—	ADC positive voltage reference input.
	C1IN0-	AN	—	Comparator C1 negative input.
	C2IN0-	AN	—	Comparator C2 negative input.
	DAC1REF+	—	AN	Digital-to-Analog Converter positive reference input.
	ICDCLK	TTL/ST	CMOS	In-Circuit Debug Clock I/O.
	ICSPCLK	TTL/ST	CMOS	ICSP Clock I/O.
RA2/ANA2/VREF-/ DAC1REF-/ T0CKI(1)/ CCP3(1)/CWG1IN(1)/ CWG2IN(1)/INT(1)	RA2	TTL/ST	CMOS	General purpose I/O.
	ANA2	AN	—	ADC Channel A2 input.
	VREF-	AN	—	ADC negative voltage reference input.
	DAC1REF-	—	AN	Digital-to-Analog Converter negative reference input.
	T0CKI	TTL/ST	—	TMR0 Clock input.
	CCP3	TTL/ST	CMOS	Capture/Compare/PWM 3 input.
	CWG1IN	TTL/ST	—	Complementary Waveform Generator 1 input.
	CWG2IN	TTL/ST	—	Complementary Waveform Generator 2 input.
	INT	TTL/ST	—	External interrupt input.
RA3/$\overline{MCLR}$/VPP	RA3	TTL/ST	CMOS	General purpose I/O.
	$\overline{MCLR}$	TTL/ST	—	Master Clear with internal pull-up.
	VPP	HV	—	Programming voltage.
RA4/ANA4/T1G(1)/ SOSCO/ CLKOUT/OSC2	RA4	TTL/ST	CMOS	General purpose I/O.
	ANA4	AN	—	ADC Channel A4 input.
	T1G	ST	—	TMR1 gate input.
	SOSCO	—	XTAL	Secondary Oscillator connection.
	CLKOUT	—	CMOS	FOSC/4 output.
	OSC2	—	XTAL	Crystal/Resonator (LP, XT, HS modes).

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open-Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C = Schmitt Trigger input with I^2C
HV = High Voltage XTAL = Crystal levels

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers. See Register 13-1.

2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers. See Register 13-2.

3: These I^2C functions are bidirectional. The output pin selections must be the same as the input pin selections.

TABLE 1-2: PIC16(L)F18326 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
OUT(2)	C1	—	CMOS	Comparator C1 output.
	C2	—	CMOS	Comparator C2 output.
	NCO1	—	CMOS	Numerically Controlled Oscillator output.
	DSM	—	CMOS	Digital Signal Modulator output.
	TMR0	—	CMOS	TMR0 clock output.
	CCP1	—	CMOS	Capture/Compare/PWM 1 output.
	CCP2	—	CMOS	Capture/Compare/PWM 2 output.
	CCP3	—	CMOS	Capture/Compare/PWM 3 output.
	CCP4	—	CMOS	Capture/Compare/PWM 4 output.
	PWM5	—	CMOS	Pulse-Width Modulator 5 output.
	PWM6	—	CMOS	Pulse-Width Modulator 6 output.
	CWG1A	—	CMOS	Complementary Waveform Generator 1 output A.
	CWG2A	—	CMOS	Complementary Waveform Generator 2 output A.
	CWG1B	—	CMOS	Complementary Waveform Generator 1 output B.
	CWG2B	—	CMOS	Complementary Waveform Generator 2 output B.
	CWG1C	—	CMOS	Complementary Waveform Generator 1 output C.
	CWG2C	—	CMOS	Complementary Waveform Generator 2 output C.
	CWG1D	—	CMOS	Complementary Waveform Generator 1 output D.
	CWG2D	—	CMOS	Complementary Waveform Generator 2 output D.
	SDA1(3)	I^2C	OD	I^2C data output.
	SDA2(3)	I^2C	OD	I^2C data output.
	SCL1(3)	I^2C	OD	I^2C clock output.
	SCL2(3)	I^2C	OD	I^2C clock output.
	SDO1	—	CMOS	SPI1 data output.
	SD02	—	CMOS	SPI2 data output.
	SCK1	—	CMOS	SPI1 clock output.
	SCK2	—	CMOS	SPI2 clock output.
	TX/CK	—	CMOS	Asynchronous TX data/synchronous clock output.
	DT	—	CMOS	EUSART synchronous data output.
	CLC1OUT	—	CMOS	Configurable Logic Cell 1 source output.
	CLC2OUT	—	CMOS	Configurable Logic Cell 2 source output.
	CLC3OUT	—	CMOS	Configurable Logic Cell 3 source output.
	CLC4OUT	—	CMOS	Configurable Logic Cell 4 source output.
	CLKR	—	CMOS	Clock Reference output.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open-Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C = Schmitt Trigger input with I^2C
HV = High Voltage XTAL = Crystal levels

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers. See Register 13-1.

2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers. See Register 13-2.

3: These I^2C functions are bidirectional. The output pin selections must be the same as the input pin selections.

TABLE 4-4: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-31 (CONTINUED)

Address	Name	PIC16(L)F18326	PIC16(L)F18346	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
Bank 28													
CPU CORE REGISTERS; see Table 4-2 for specifics													
E0Ch	—	—		Unimplemented								—	—
E0Dh	—	—		Unimplemented								—	—
E0Eh	—	—		Unimplemented								—	—
E0Fh	PPSLOCK			—	—	—	—	—	—	—	PPSLOCKED	---- ---0	---- ---0
E10h	INTPPS			—	—	—	INTPPS<4:0>					---0 0010	---u uuuu
E11h	T0CKIPPS			—	—	—	T0CKIPPS<4:0>					---0 0010	---u uuuu
E12h	T1CKIPPS			—	—	—	T1CKIPPS<4:0>					---0 0101	---u uuuu
E13h	T1GPPS			—	—	—	T1GPPS<4:0>					---0 0100	---u uuuu
E14h	CCP1PPS			—	—	—	CCP1PPS<4:0>					---1 0011	---u uuuu
E15h	CCP2PPS			—	—	—	CCP2PPS<4:0>					---1 0101	---u uuuu
E16h	CCP3PPS			—	—	—	CCP3PPS<4:0>					---0 0010	---u uuuu
E17h	CCP4PPS	X	—	—	—	—	CCP4PPS<4:0>					---1 0001	---u uuuu
		—	X	—	—	—	CCP4PPS<4:0>					---0 0100	---u uuuu
E18h	CWG1PPS			—	—	—	CWG1PPS<4:0>					---0 0010	---u uuuu
E19h	CWG2PPS			—	—	—	CWG2PPS<4:0>					---0 0010	---u uuuu
E1Ah	MDCIN1PPS			—	—	—	MDCIN1PPS<4:0>					---1 0010	---u uuuu
E1Bh	MDCIN2PPS			—	—	—	MDCIN2PPS<4:0>					---1 0101	---u uuuu
E1Ch	MDMINPPS			—	—	—	MDMINPPS<4:0>					---1 0011	---u uuuu
E1Dh	SSP2CLKPPS	X	—	—	—	—	SSP2CLKPPS<4:0>					---1 0100	---u uuuu
		—	X	—	—	—	SSP2CLKPPS<4:0>					---0 1111	---u uuuu
E1Eh	SSP2DATPPS	X	—	—	—	—	SSP2DATPPS<4:0>					---1 0101	---u uuuu
		—	X	—	—	—	SSP2DATPPS<4:0>					---0 1101	---u uuuu
E1Fh	SSP2SSPPS	X	—	—	—	—	SSP2SSPPS<4:0>					---0 0000	---u uuuu
		—	X	—	—	—	SSP2SSPPS<4:0>					---0 0001	---u uuuu
E20h	SSP1CLKPPS	X	—	—	—	—	SSP1CLKPPS<4:0>					---1 0000	---u uuuu
		—	X	—	—	—	SSP1CLKPPS<4:0>					---0 1110	---u uuuu

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

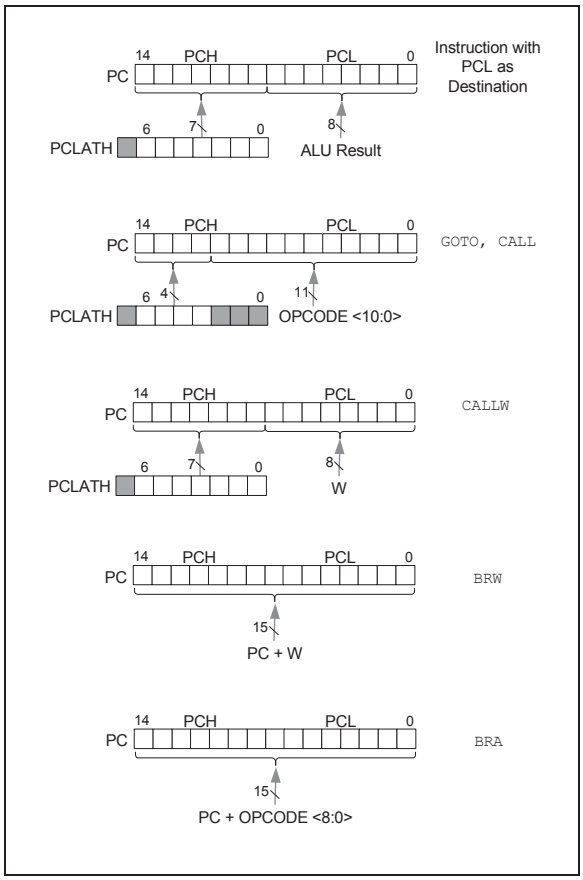
Note 1: Only on PIC16F18326/18346.

2: Register accessible from both User and ICD Debugger.

4.3 PCL and PCLATH

The Program Counter (PC) is 15 bits wide. The low byte comes from the PCL register, which is a readable and writable register. The high byte (PC<14:8>) is not directly readable or writable and comes from PCLATH. On any Reset, the PC is cleared. Figure 4-3 shows the five situations for the loading of the PC.

FIGURE 4-3: LOADING OF PC IN DIFFERENT SITUATIONS



4.3.1 MODIFYING PCL

Executing any instruction with the PCL register as the destination simultaneously causes the Program Counter PC<14:8> bits (PCH) to be replaced by the contents of the PCLATH register. This allows the entire contents of the program counter to be changed by writing the desired upper seven bits to the PCLATH register. When the lower eight bits are written to the PCL register, all 15 bits of the program counter will change to the values contained in the PCLATH register and those being written to the PCL register.

4.3.2 COMPUTED GOTO

A computed GOTO is accomplished by adding an offset to the program counter (ADDWF PCL). When performing a table read using a computed GOTO method, care should be exercised if the table location crosses a PCL memory boundary (each 256-byte block). Refer to Application Note AN556, *Implementing a Table Read* (DS00556).

4.3.3 COMPUTED FUNCTION CALLS

A computed function CALL allows programs to maintain tables of functions and provide another way to execute state machines or look-up tables. When performing a table read using a computed function CALL, care should be exercised if the table location crosses a PCL memory boundary (each 256-byte block).

If using the CALL instruction, the PCH<2:0> and PCL registers are loaded with the operand of the CALL instruction. PCH<6:3> is loaded with PCLATH<6:3>.

The CALLW instruction enables computed calls by combining PCLATH and $\overline{W}$ to form the destination address. A computed CALLW is accomplished by loading the $\overline{W}$ register with the desired address and executing CALLW. The PCL register is loaded with the value of $\overline{W}$ and PCH is loaded with PCLATH.

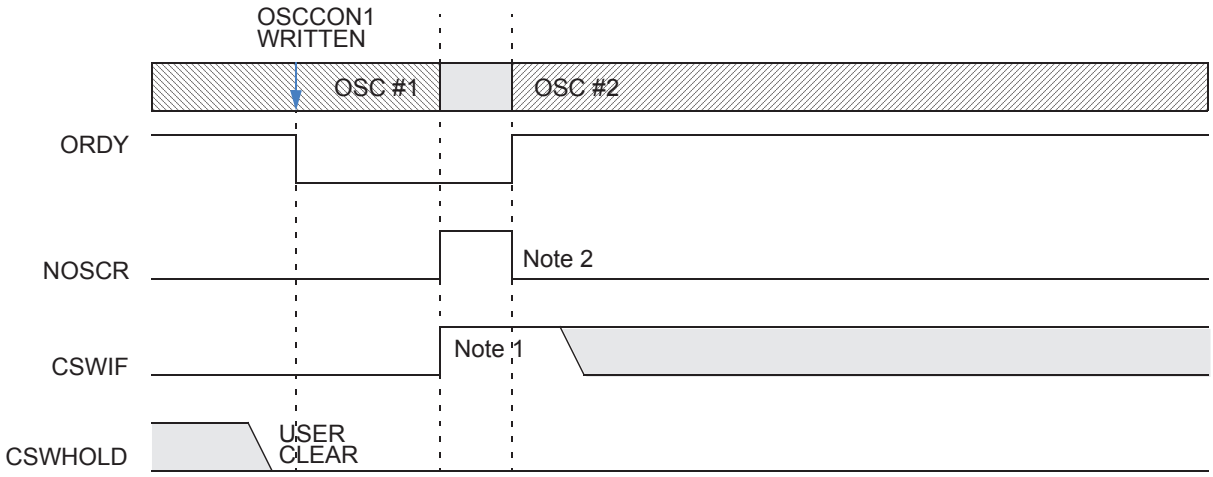
4.3.4 BRANCHING

The branching instructions add an offset to the PC. This allows relocatable code and code that crosses page boundaries. There are two forms of branching, BRW and BRA. The PC will have incremented to fetch the next instruction in both cases. When using either branching instruction, a PCL memory boundary may be crossed.

If using BRW, load the $\overline{W}$ register with the desired unsigned address and execute BRW. The entire PC will be loaded with the address PC + 1 + $\overline{W}$.

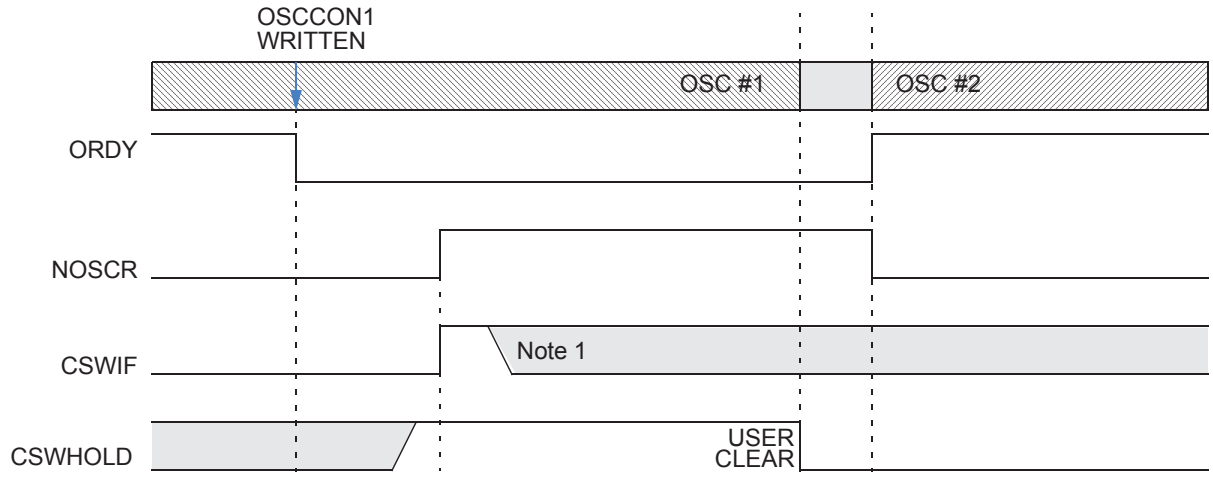
If using BRA, the entire PC will be loaded with PC + 1 + the signed value of the operand of the BRA instruction.

FIGURE 7-6: CLOCK SWITCH (CSWHOLD = 0)



Note 1: CSWIF is asserted coincident with NOSCR; interrupt is serviced at OSC#2 speed.
2: The assertion of NOSCR is hidden from the user because it appears only for the duration of the switch.

FIGURE 7-7: CLOCK SWITCH (CSWHOLD = 1)



Note 1: CSWIF is asserted coincident with NOSCR, and may be cleared before or after clearing CSWHOLD = 0.

11.4.2 NVM UNLOCK SEQUENCE

The unlock sequence is a mechanism that protects the NVM from unintended self-write programming or erasing. The sequence must be executed and completed without interruption to successfully complete any of the following operations:

- Program Flash Memory Row Erase
- Load of Program Flash Memory write latches
- Write of Program Flash Memory write latches to Program Flash Memory memory
- Write of Program Flash Memory write latches to User IDs
- Write to EEPROM

The unlock sequence consists of the following steps and must be completed in order:

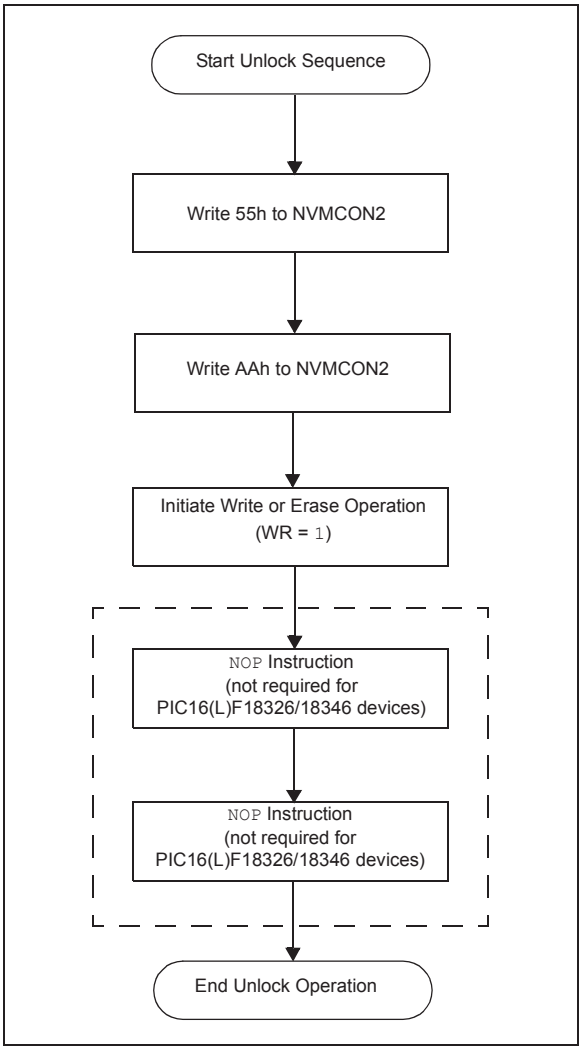
- Write 55h to NVMCON2
- Write AAh to NMVCON2
- Set the WR bit of NVMCON1

Once the WR bit is set, the processor will stall internal operations until the operation is complete and then resume with the next instruction.

Note:	The two NOP instructions after setting the WR bit, which were required in previous devices, are not required for PIC16(L)F18326/18346 devices. See Figure 11-2.

Since the unlock sequence must not be interrupted, global interrupts should be disabled prior to the unlock sequence and re-enabled after the unlock sequence is completed.

FIGURE 11-2: NVM UNLOCK SEQUENCE FLOWCHART



EXAMPLE 11-2: NVM UNLOCK SEQUENCE

```
BANKSEL                 NVMCON1
BSF                     NVMCON1,WREN      ; Enable write/erase
MOVLW                   55h               ; Load 55h
BCF                     INTCON,GIE        ; Recommended so sequence is not interrupted

MOVWF                   NVMCON2           ; Step 1: Load 55h into NVMCON2
MOVLW                   AAh               ; Step 2: Load W with AAh
MOVWF                   NVMCON2           ; Step 3: Load AAh into NVMCON2
BSF                     NVMCON1,WR        ; Step 4: Set WR bit to begin write/erase

BSF                     INTCON,GIE        ; Re-enable interrupts
```

Note 1: Sequence begins when NVMCON2 is written; steps 1-4 must occur in the cycle-accurate order shown.

2: Opcodes shown are illustrative; any instruction that has the indicated effect may be used.

REGISTER 20-7: CWGxAS1: CWG AUTO-SHUTDOWN CONTROL REGISTER 1

U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	—	AS4E	AS3E	AS2E	AS1E	AS0E
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **AS4E:** CWG Auto-Shutdown Source 4 (CLC4) Enable bit
1 = Auto-shutdown for CLC4 is enabled
0 = Auto-shutdown for CLC4 is disabled

bit 3 **AS3E:** CWG Auto-Shutdown Source 3 (CLC2) Enable bit
1 = Auto-shutdown from CLC2 is enabled
0 = Auto-shutdown from CLC2 is disabled

bit 2 **AS2E:** CWG Auto-Shutdown Source 2 (C2) Enable bit
1 = Auto-shutdown from Comparator 2 is enabled
0 = Auto-shutdown from Comparator 2 is disabled

bit 1 **AS1E:** CWG Auto-Shutdown Source 1 (C1) Enable bit
1 = Auto-shutdown from Comparator 1 is enabled
0 = Auto-shutdown from Comparator 1 is disabled

bit 0 **AS0E:** CWG Auto-Shutdown Source 0 (CWGxPPS) Enable bit
1 = Auto-shutdown from CWGxPPS is enabled
0 = Auto-shutdown from CWGxPPS is disabled

REGISTER 20-8: CWGxDBR: CWGx RISING DEAD-BAND COUNT REGISTER

U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	DBR<5:0>					
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **DBR<5:0>:** CWG Rising Edge Triggered Dead-Band Count bits
11 1111 = 63-64 CWG clock periods
11 1110 = 62-63 CWG clock periods
.
.
.
00 0010 = 2-3 CWG clock periods
00 0001 = 1-2 CWG clock periods
00 0000 = 0 CWG clock periods. Dead-band generation is bypassed.

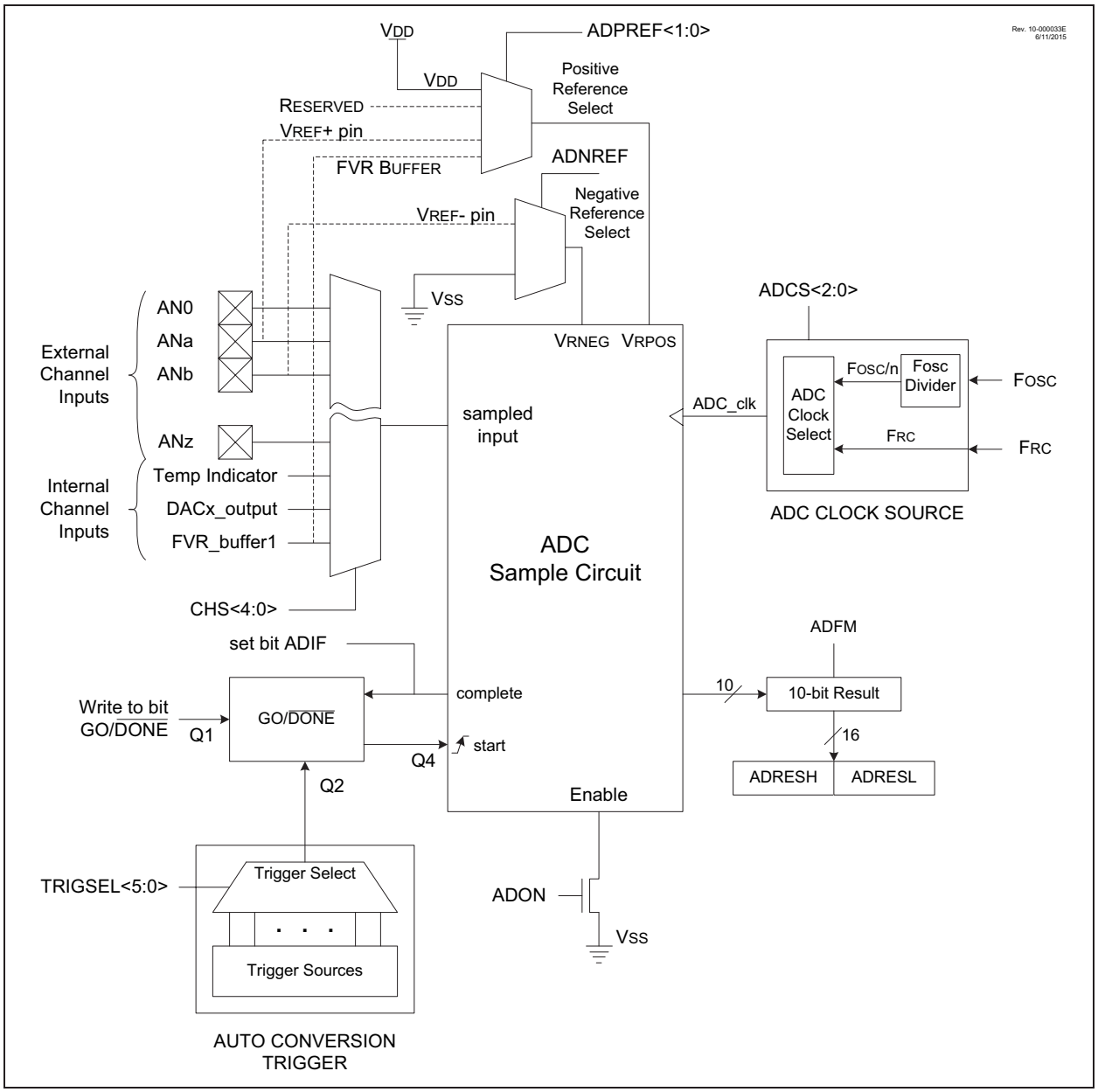
22.0 ANALOG-TO-DIGITAL CONVERTER (ADC) MODULE

The Analog-to-Digital Converter (ADC) allows conversion of an analog input signal to a 10-bit binary representation of that signal. This device uses analog inputs, which are multiplexed into a single sample and hold circuit. The output of the sample and hold is connected to the input of the converter. The converter generates a 10-bit binary result via successive approximation and stores the conversion result into the ADC result registers (ADRESH:ADRESL register pair). Figure 22-1 shows the block diagram of the ADC.

The ADC voltage reference is software selectable to be either internally generated or externally supplied.

The ADC can generate an interrupt upon completion of a conversion. This interrupt can be used to wake-up the device from Sleep.

FIGURE 22-1: ADC BLOCK DIAGRAM



29.0 CAPTURE/COMPARE/PWM MODULES

The Capture/Compare/PWM module is a peripheral that allows the user to time and control different events and to generate Pulse-Width Modulation (PWM) signals. In Capture mode, the peripheral allows the timing of the duration of an event. The Compare mode allows the user to trigger an external event when a predetermined amount of time has expired. The PWM mode can generate Pulse-Width Modulated signals of varying frequency and duty cycle.

This family of devices contains four standard Capture/Compare/PWM modules (CCP1, CCP2, CCP3 and CCP4).

The Capture and Compare functions are identical for all CCP modules.

29.1 CCP/PWM Clock Selection

The PIC16(L)F18326/18346 devices allow each individual CCP and PWM module to select the timer source that controls the module. Each module has an independent selection.

As there are up to three 8-bit timers with auto-reload (Timer2, Timer4, and Timer6), PWM mode on the CCP and PWM modules can use any of these timers.

The CCPTMRS register is used to select which timer is used.

Note 1:	In devices with more than one CCP module, it is very important to pay close attention to the register names used. A number placed after the module acronym is used to distinguish between separate modules. For example, the CCP1CON and CCP2CON control the same operational aspects of two completely different CCP modules.
2:	Throughout this section, generic references to a CCP module in any of its operating modes may be interpreted as being equally applicable to CCPx module. Register names, module signals, I/O pins, and bit names may use the generic designator ‘x’ to indicate the use of a numeral to distinguish a particular module, when required.

29.2 Capture Mode

Capture mode makes use of either the 16-bit Timer0 or Timer1 resource. When an event occurs on the capture source, the 16-bit CCPRxH:CCPRxL register pair captures and stores the 16-bit value of the TMR0H:TMR0L or TMR1H:TMR1L register pair, respectively. An event is defined as one of the following and is configured by the CCPxMODE<3:0> bits of the CCPxCON register:

- Every falling edge
- Every rising edge
- Every 4th rising edge
- Every 16th rising edge

When a capture is made, the Interrupt Request Flag bit CCPxIF of the PIR4 register is set. The interrupt flag must be cleared in software. If another capture occurs before the value in the CCPRxH, CCPRxL register pair is read, the old captured value is overwritten by the new captured value.

Figure 29-1 shows a simplified diagram of the capture operation.

29.2.1 CAPTURE SOURCES

In Capture mode, the CCPx pin should be configured as an input by setting the associated TRIS control bit.

Note:	If the CCPx pin is configured as an output, a write to the port can cause a Capture condition.

The capture source is selected by configuring the CCPxCTS<3:0> bits of the CCPxCAP register. The following sources can be selected:

- CCPxPPS input
- C1_output
- C2_output
- NCO_output
- IOC_interrupt
- LC1_output
- LC2_output
- LC3_output
- LC4_output

29.2.2 TIMER1/3/5 MODE RESOURCE

Timer1/3/5 must be running in Timer mode or Synchronized Counter mode for the CCP module to use the capture feature. In Asynchronous Counter mode, the capture operation may not work.

See **Section 27.0 "Timer1/3/5 Module with Gate Control"** for more information on configuring Timer1/3/5.

Note:	Clocking Timer1/3/5 from the system clock (FOSC) should not be used in Capture mode. In order for Capture mode to recognize the trigger event on the CCPx pin, Timer1/3/5 must be clocked from the instruction clock (FOSC/4) or from an external clock source.

29.2.3 SOFTWARE INTERRUPT MODE

When the Capture mode is changed, a false capture interrupt may be generated. The user should keep the CCPxIE interrupt enable bit of the PIE4 register clear to avoid false interrupts. Additionally, the user should clear the CCPxIF interrupt flag bit of the PIR4 register following any change in Operating mode.

29.2.4 CCP PRESCALER

There are four prescaler settings specified by the CCPxMODE<3:0> bits of the CCPxCON register. Whenever the CCP module is turned off, or the CCP module is not in Capture mode, the prescaler counter is cleared. Any Reset will clear the prescaler counter.

Switching from one capture prescaler to another does not clear the prescaler and may generate a false interrupt. To avoid this unexpected operation, turn the module off by clearing the CCPxCON register before changing the prescaler. Example 29-1 demonstrates the code to perform this function.

EXAMPLE 29-1: CHANGING BETWEEN CAPTURE PRESCALERS

```
BANKSEL CCPxCON     ;Set Bank bits to point
                    ;to CCPxCON
CLRF    CCPxCON     ;Turn CCP module off
MOVLW   NEW_CAPT_PS ;Load the W reg with
                    ;the new prescaler
                    ;move value and CCP ON
MOVWF   CCPxCON     ;Load CCPxCON with this
                    ;value
```

29.2.5 CAPTURE DURING SLEEP

Capture mode depends upon the Timer1/3/5 module for proper operation. There are two options for driving the Timer1/3/5 module in Capture mode. It can be driven by the instruction clock (FOSC/4), or by an external clock source.

When Timer1/3/5 is clocked by FOSC/4, Timer1/3/5 will not increment during Sleep. When the device wakes from Sleep, Timer1/3/5 will continue from its previous state.

Capture mode will operate during Sleep when Timer1/3/5 is clocked by an external clock source.

29.3 Compare Mode

Compare mode makes use of the 16-bit Timer1/3/5 resource. The 16-bit value of the CCPRxH:CCPRxL register pair is constantly compared against the 16-bit value of the TMR1/3/5H:TMR1/3/5L register pair. When a match occurs, one of the following events can occur:

- Toggle the CCPx output
- Set the CCPx output
- Clear the CCPx output
- Generate an Auto-conversion Trigger
- Generate a Software Interrupt

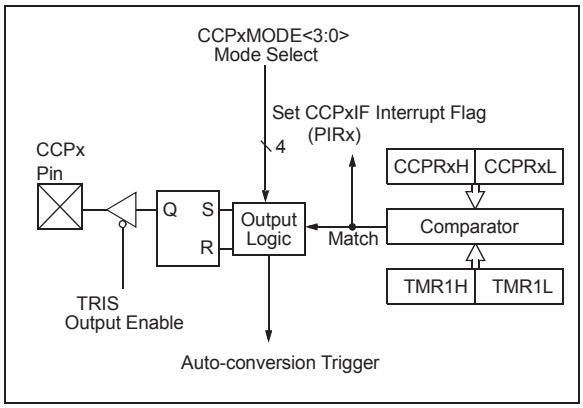
The action on the pin is based on the value of the CCPxMODE<3:0> control bits of the CCPxCON register. At the same time, the interrupt flag CCPxIF bit is set, and an ADC conversion can be triggered, if selected.

All Compare modes can generate an interrupt and trigger an ADC conversion.

Figure 29-2 shows a simplified diagram of the compare operation.

Note:	When the CCP is configured in Compare mode using the 'toggle output on match' setting (CCPxMODE<3:0> bits = 0010) and the reference timer is set for an input clock prescale other than 1:1, the output of the CCP will toggle multiple times until finally settling a '0' logic level. To avoid this, the timer input clock prescale select bits must be set to a 1:1 ratio (TxCKPS = 00).

FIGURE 29-2: COMPARE MODE OPERATION BLOCK DIAGRAM



29.3.1 CCPX PIN CONFIGURATION

The user must configure the CCPx pin as an output by clearing the associated TRIS bit and defining the appropriate output pin through the RxyPPS registers. See **Section 13.0 "Peripheral Pin Select (PPS) Module"** for more details.

Note:	Clearing the CCPxCON register will force the CCPx compare output latch to the default low level. This is not the PORT I/O data latch.

29.3.2 TIMER1/3/5 MODE RESOURCE

In Compare mode, Timer1/3/5 must be running in either Timer mode or Synchronized Counter mode. The compare operation may not work in Asynchronous Counter mode.

See **Section 27.0 "Timer1/3/5 Module with Gate Control"** for more information on configuring Timer1/3/5.

Note:	Clocking Timer1/3/5 from the system clock (FOSC) should not be used in Compare mode. In order for Compare mode to recognize the trigger event on the CCPx pin, Timer1/3/5 must be clocked from the instruction clock (FOSC/4) or from an external clock source.

29.3.3 AUTO-CONVERSION TRIGGER

All CCPx modes set the CCP interrupt flag (CCPxIF). When this flag is set as a match occurs, an auto-conversion trigger can occur if the CCP module is selected as the conversion trigger source.

Refer to **Section 22.2.4 "Auto-Conversion Trigger"** for more information.

Note:	Removing the Match condition by changing the contents of the CCPRxH and CCPRxL register pair, between the clock edge that generates the Auto-conversion Trigger and the clock edge that generates the Timer Reset, will preclude the Reset from occurring.

29.3.4 COMPARE DURING SLEEP

Since FOSC is shut down during Sleep mode, the Compare mode will not function properly during Sleep, unless the timer is running. The device will wake on interrupt (if enabled).

29.3.5 COMPARE INTERRUPTS

The CCPxIF interrupt flag will be set when a match between the CCPRxH:CCPRxL register pair and the TMR1/3/5H:TMR1/3/5L register pair occurs. If the device is in Sleep and interrupts are enabled (CCPxIE = 1), the device will wake up, assuming Timer1 is operating during Sleep.

FIGURE 30-18: I²C SLAVE, 7-BIT ADDRESS, TRANSMISSION (AHEN = 0)

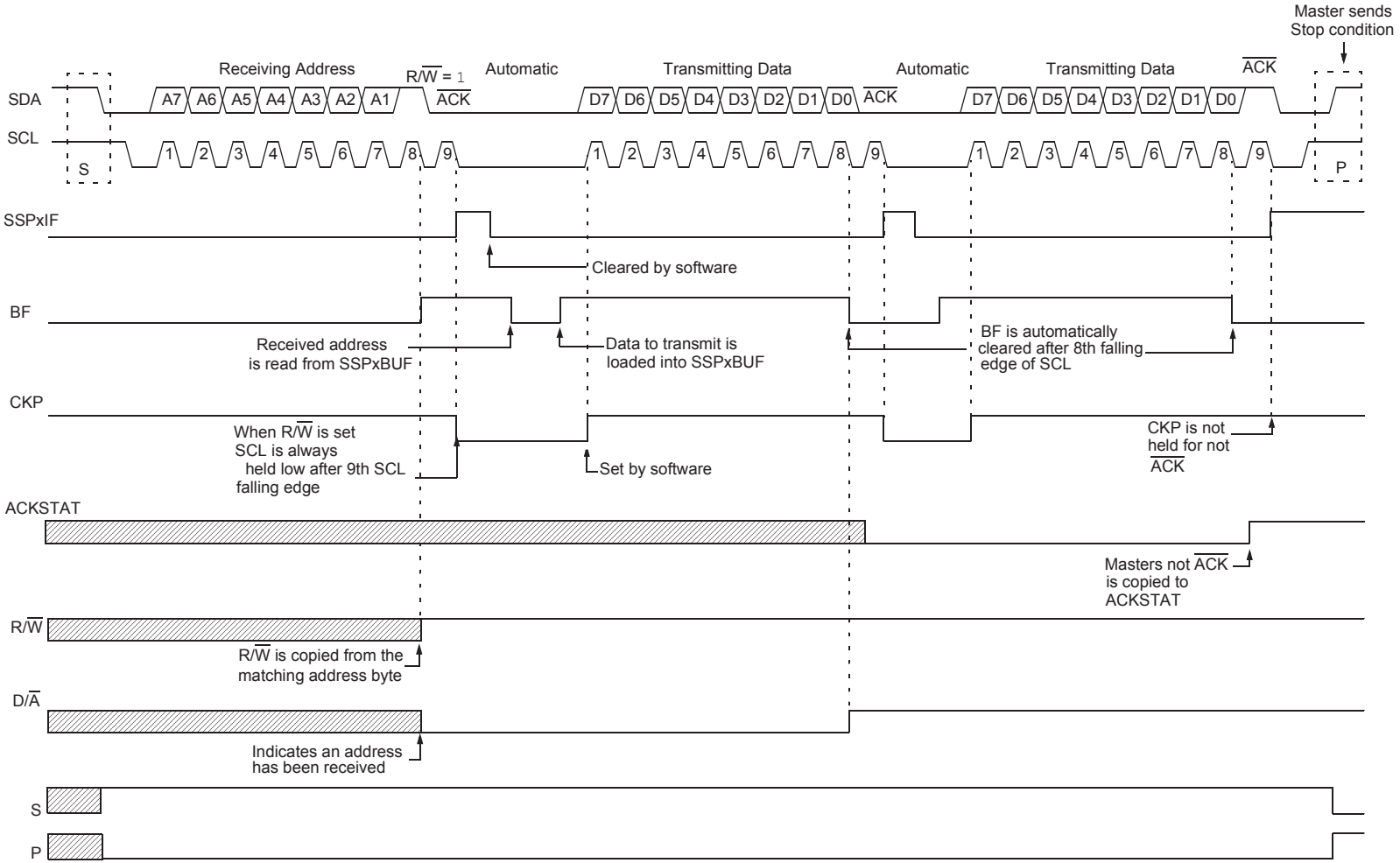
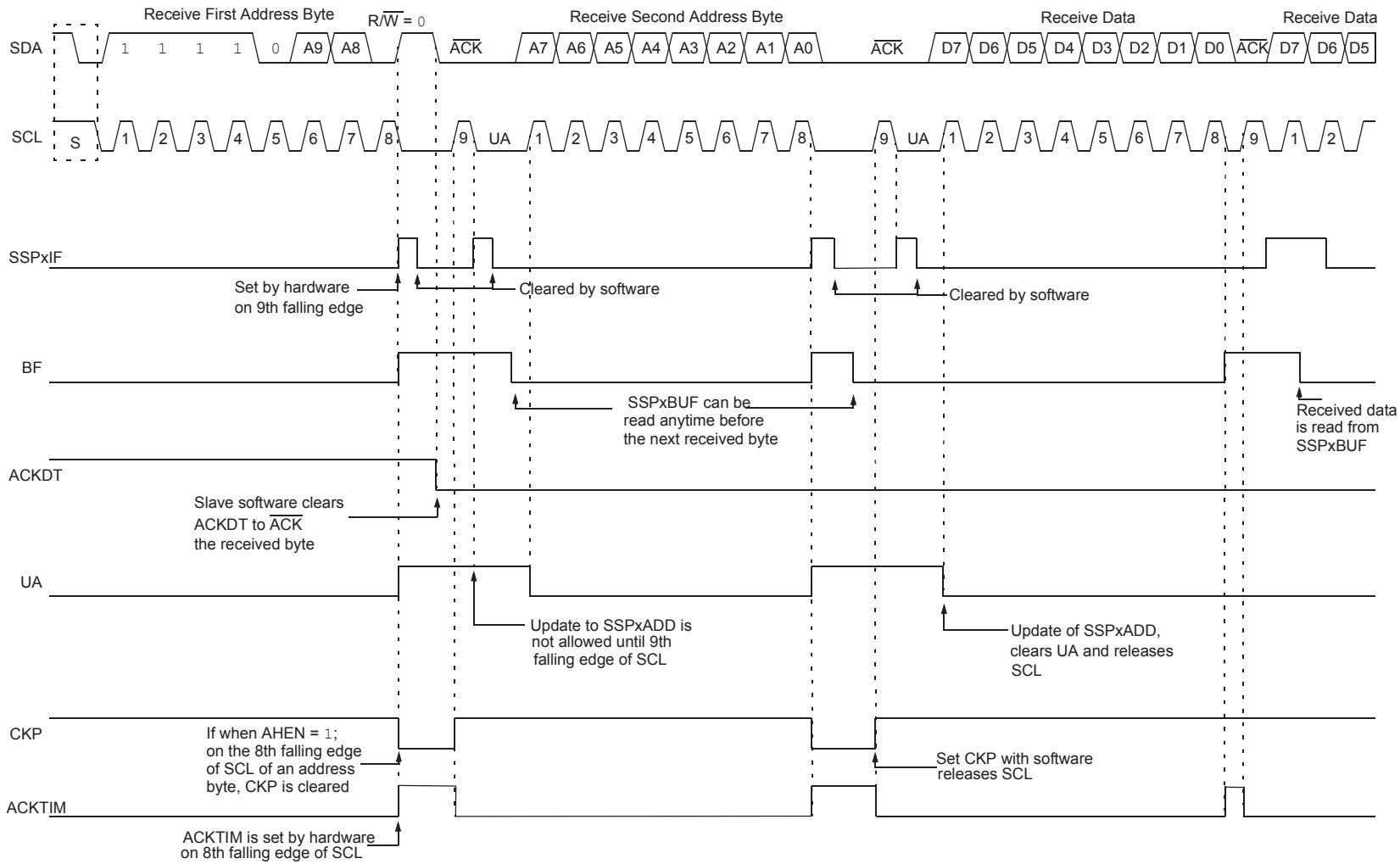


FIGURE 30-21: I²C SLAVE, 10-BIT ADDRESS, RECEPTION (SEN = 0, AHEN = 1, DHEN = 0)



30.6.5 I²C MASTER MODE REPEATED START CONDITION TIMING

A Repeated Start condition (Figure 30-27) occurs when the RSEN bit of the SSPxCON2 register is programmed high and the master state machine is no longer active. When the RSEN bit is set, the SCL pin is asserted low. When the SCL pin is sampled low, the Baud Rate Generator is loaded and begins counting. The SDA pin is released (brought high) for one Baud Rate Generator count (TBRG). When the Baud Rate Generator times out, if SDA is sampled high, the SCL pin will be deasserted (brought high). When SCL is sampled high, the Baud Rate Generator is reloaded and begins counting. SDA and SCL must be sampled high for one TBRG. This action is then followed by assertion of the SDA pin (SDA = 0) for one TBRG while SCL is high. SCL is asserted low. Following this, the RSEN bit of the SSPxCON2 register will be automatically cleared and the Baud Rate Generator will not be reloaded, leaving the SDA pin held low. As soon as a Start condition is detected on the SDA and SCL pins, the S bit of the SSPxSTAT register will be set. The SSPxIF bit will not be set until the Baud Rate Generator has timed out.

Note 1: If RSEN is programmed while any other event is in progress, it will not take effect.

2: A bus collision during the Repeated Start condition occurs if:

- SDA is sampled low when SCL goes from low-to-high.
- SCL goes low before SDA is asserted low. This may indicate that another master is attempting to transmit a data '1'.

FIGURE 30-27: REPEATED START CONDITION WAVEFORM

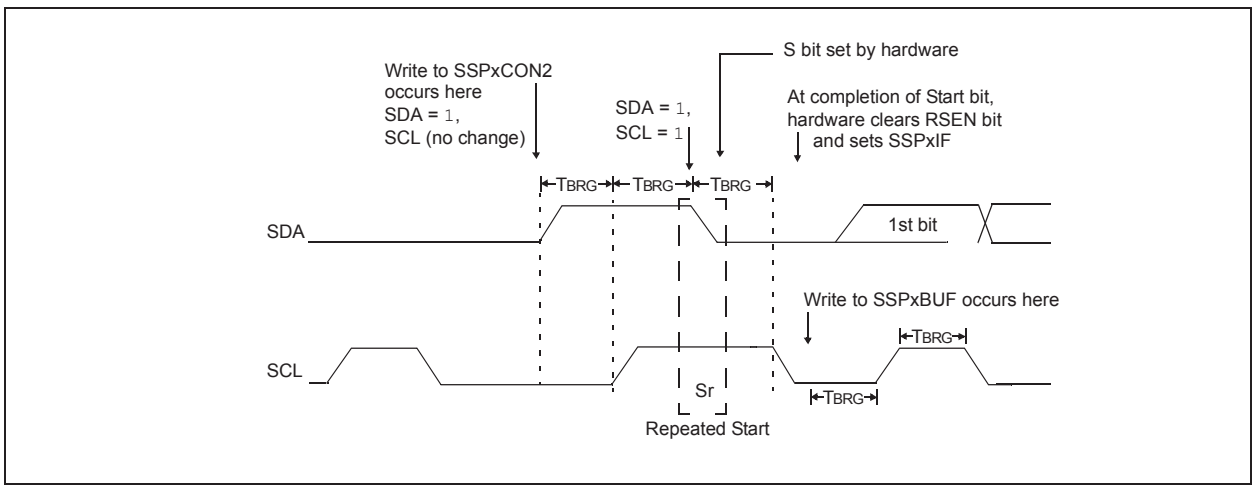


FIGURE 30-28: I^2C MASTER MODE WAVEFORM (TRANSMISSION, 7 OR 10-BIT ADDRESS)

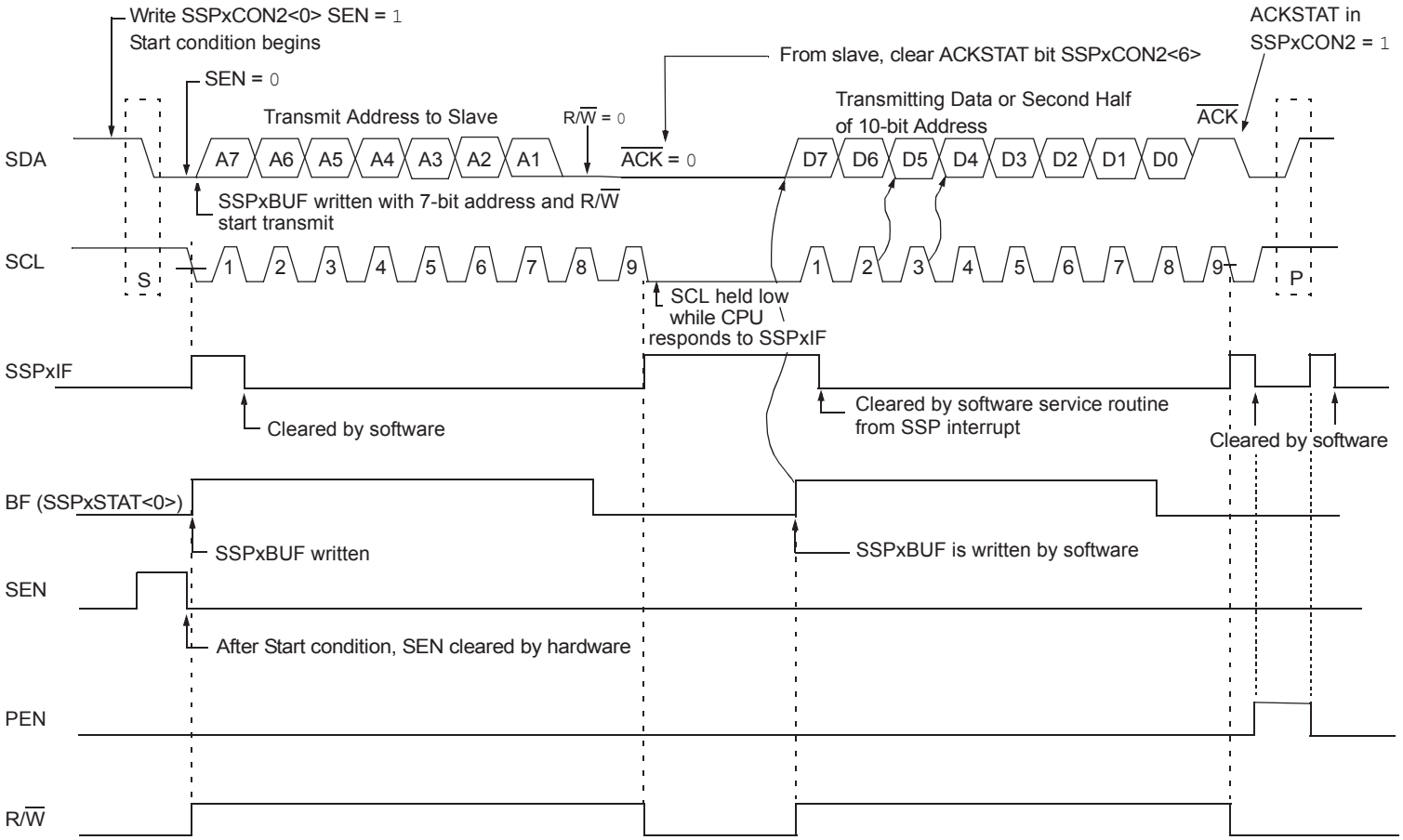
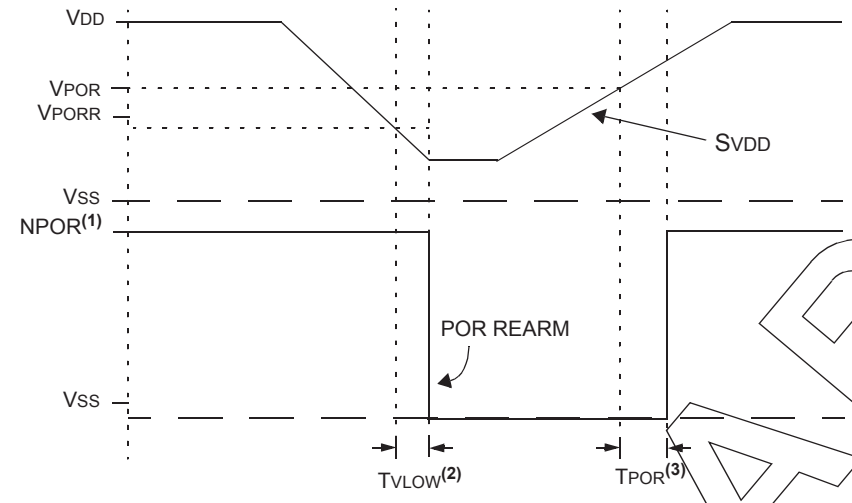


FIGURE 35-3: POR AND POR REARM WITH SLOW RISING VDD



Note 1: When NPOR is low, the device is held in Reset.
2: TPOR 1 μs typical.
3: TVLOW 2.7 μs typical.

TABLE 35-14: COMPARATOR SPECIFICATIONS

Standard Operating Conditions (unless otherwise stated) VDD = 3.0V, TA = 25°C See **Section 36.0 "DC and AC Characteristics Graphs and Charts"** for operating characterization.							
Param No.	**Sym.**	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Comments**
CM01	VIOFF	Input Offset Voltage	—	—	±50	mV	VICM = VDD/2
CM02	VICM	Input Common Mode Voltage	GND	—	VDD	V	
CM03	CMRR	Common Mode Input Rejection Ratio	—	50	—	dB	
CM04	CHYST	Comparator Hysteresis	15	25	35	mV	
CM05	TRESP(1)	Response Time, Rising Edge	—	300	600	ns	
		Response Time, Falling Edge	—	220	500	ns	
CM06*	TMCV2VO(2)	Mode Change to Valid Output	—	—	10	us	

* These parameters are characterized but not tested.

Note 1: Response time measured with one comparator input at VDD/2, while the other input transitions from VSS to VDD.

2: A mode change includes changing any of the control register values, including module enable.

TABLE 35-15: DIGITAL-TO-ANALOG CONVERTER (DAC) SPECIFICATIONS

Standard Operating Conditions (unless otherwise stated) VDD = 3.0V, TA = 25°C							
Param No.	**Sym.**	**Characteristics**	**Min.**	**Typ.†**	**Max.**	**Units**	**Comments**
DSB01	VLSB	Step Size	—	VDD/32	—	V	
DSB01	VACC	Absolute Accuracy	—	—	± 0.5	LSb	
DSB03*	RUNIT	Unit Resistor Value	—	6000	—	Ω	
DSB04*	TST	Settling Time(1)	—	—	10	µs	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Settling time measured while DACR<4:0> transitions from '00000' to '01111'.

TABLE 35-16: FIXED VOLTAGE REFERENCE (FVR) SPECIFICATIONS

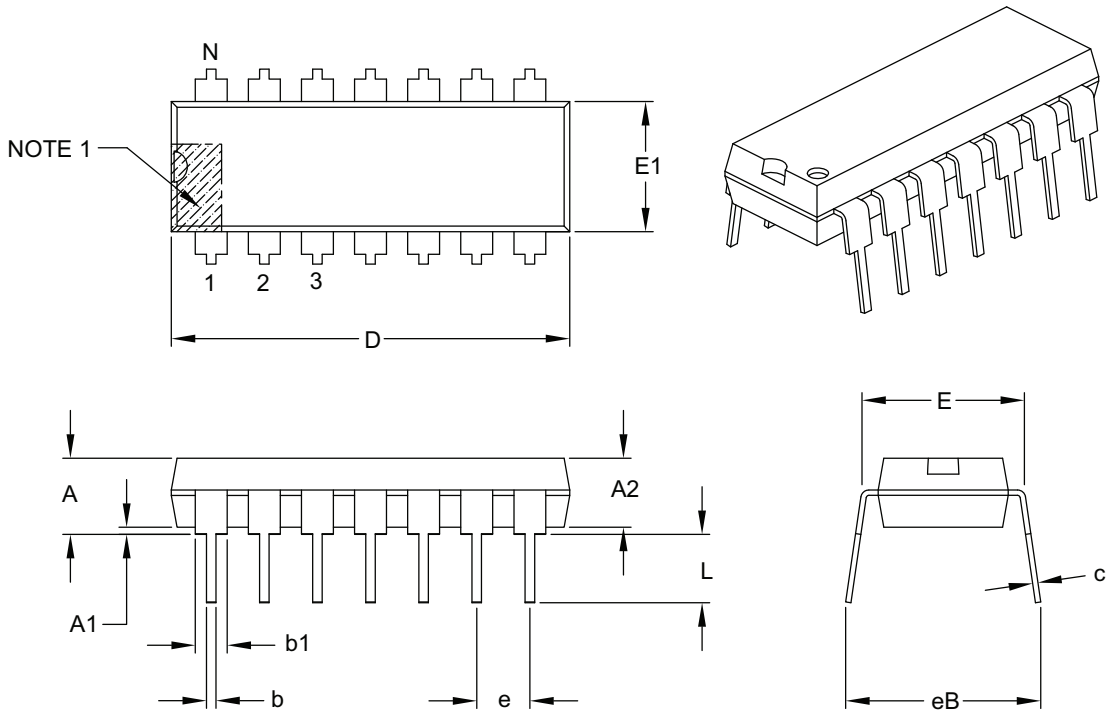
Standard Operating Conditions (unless otherwise stated)							
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
FVR01	VFVR1	1x Gain (1.024V nominal)	-4	—	4	%	VDD ≥ 2.5V, -40°C to 85°C
FVR02	VFVR2	2x Gain (2.048V nominal)	-4	—	4	%	VDD ≥ 2.5V, -40°C to 85°C
FVR03	VFVR4	4x Gain (4.096V nominal)	-5	—	5	%	VDD ≥ 4.75V, -40°C to 85°C
FVR04	TFVRST	FVR Start-up Time	—	—	—	µs	

38.2 Package Details

The following sections give the technical details of the packages.

14-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		14	
Pitch	e		.100 BSC	
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.735	.750	.775
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.045	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

1. Pin 1 visual index feature may vary, but must be located with the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-005B

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X](1)	-	X	/XX	XXX
Device	Tape and Reel Option		Temperature Range	Package	Pattern

Device:	PIC16F18326, PIC16LF18326, PIC16F18346, PIC16LF18346.	
Tape and Reel Option:	Blank T	= Standard packaging (tube or tray) = Tape and Reel(1)
Temperature Range:	I E	= -40°C to +85°C (Industrial) = -40°C to +125°C (Extended)
Package:(2)	JQ GZ P ST SL SO SS	= 16-lead UQFN (4x4) = 20-lead UQFN (4x4) = PDIP = TSSOP = 14-lead SOIC = 20-lead SOIC = SSOP
Pattern:	QTP, SQTP, Code or Special Requirements (blank otherwise)	

Examples:

a) PIC16LF18326- E/P
Extended temperature
PDIP package

b) PIC16LF18346- E/SO
Extended temperature,
SOIC package

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

2: Small form-factor packaging options may be available. Check www.microchip.com/packaging for small-form factor package availability, or contact your local Sales Office.