What is "Embedded - Microcontrollers"?

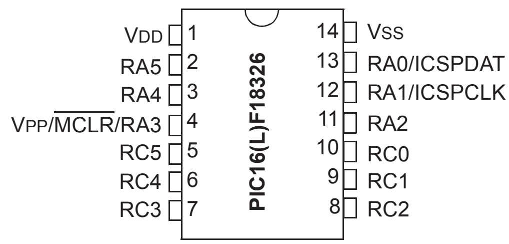
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	18
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 17x10b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf18346-e-ss

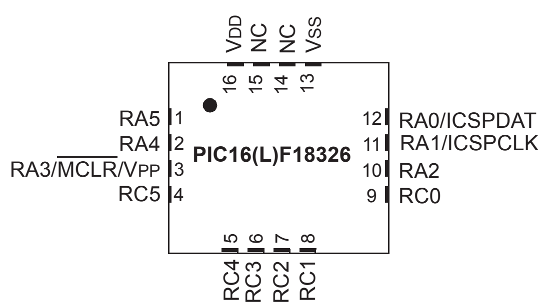
Pin Diagrams

FIGURE 1: 14-PIN PDIP, SOIC, TSSOP



Note: See Table 2 for location of all peripheral functions.

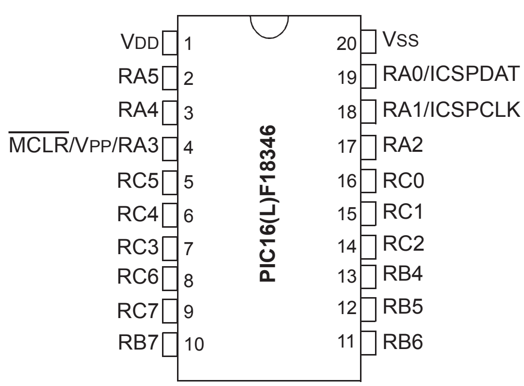
FIGURE 2: 16-PIN UQFN (4x4)



Note 1: See Table 2 for location of all peripheral functions.

2: It is recommended that the exposed bottom pad be connected to VSS, but must not be the main VSS connection to the device.

FIGURE 3: 20-PIN PDIP, SOIC, SSOP



Note: See Table 3 for location of all peripheral functions.

3.0 ENHANCED MID-RANGE CPU

This family of devices contains an enhanced mid-range 8-bit CPU core. The CPU has 48 instructions. Interrupt capability includes automatic context saving. The hardware stack is 16-levels deep and has Overflow and Underflow Reset capability. Direct, Indirect, and Relative Addressing modes are available. Two File Select Registers (FSRs) provide the ability to read program and data memory.

- Automatic Interrupt Context Saving
- 16-level Stack with Overflow and Underflow
- File Select Registers
- Instruction Set

FIGURE 3-1: CORE BLOCK DIAGRAM

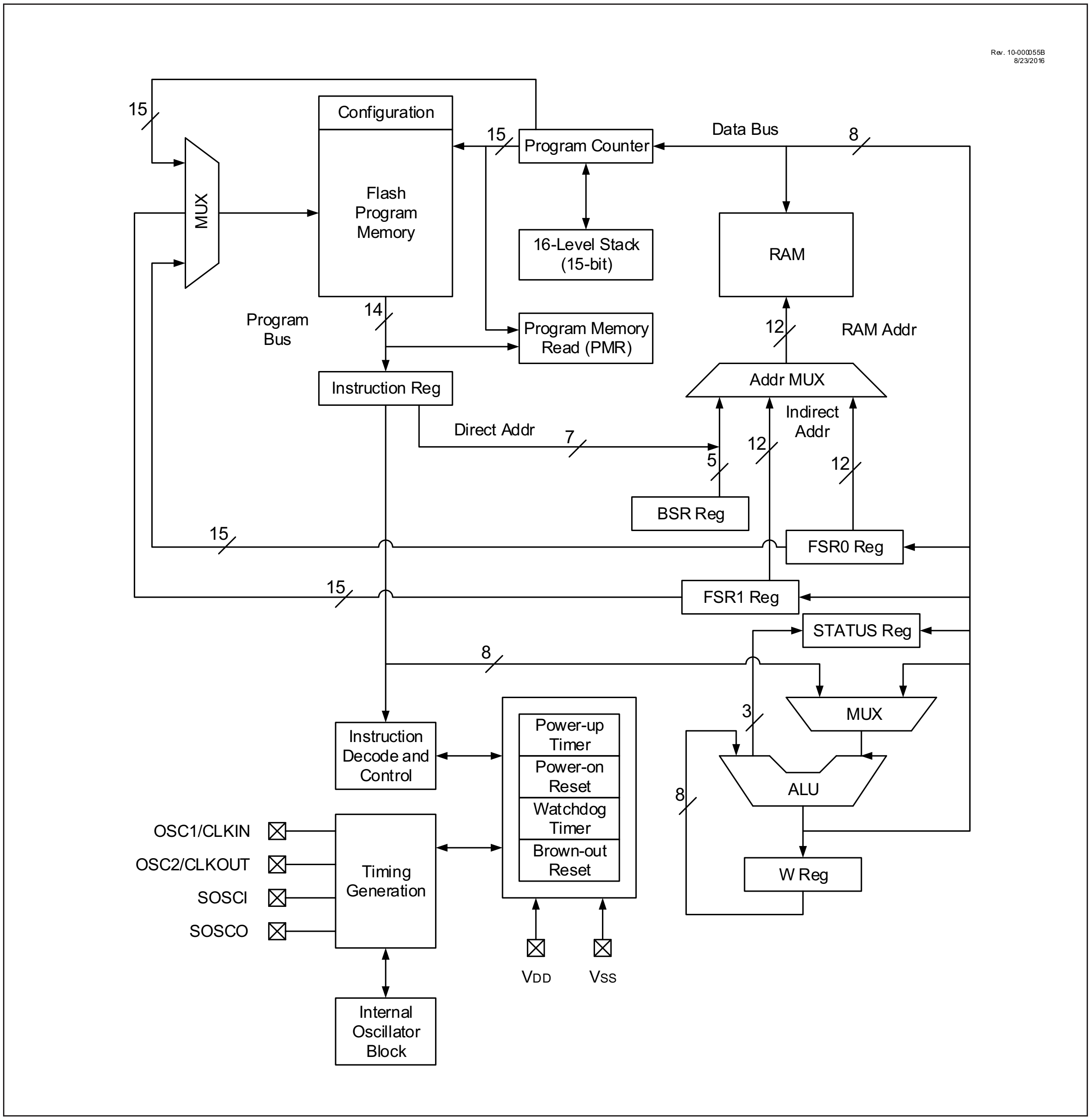


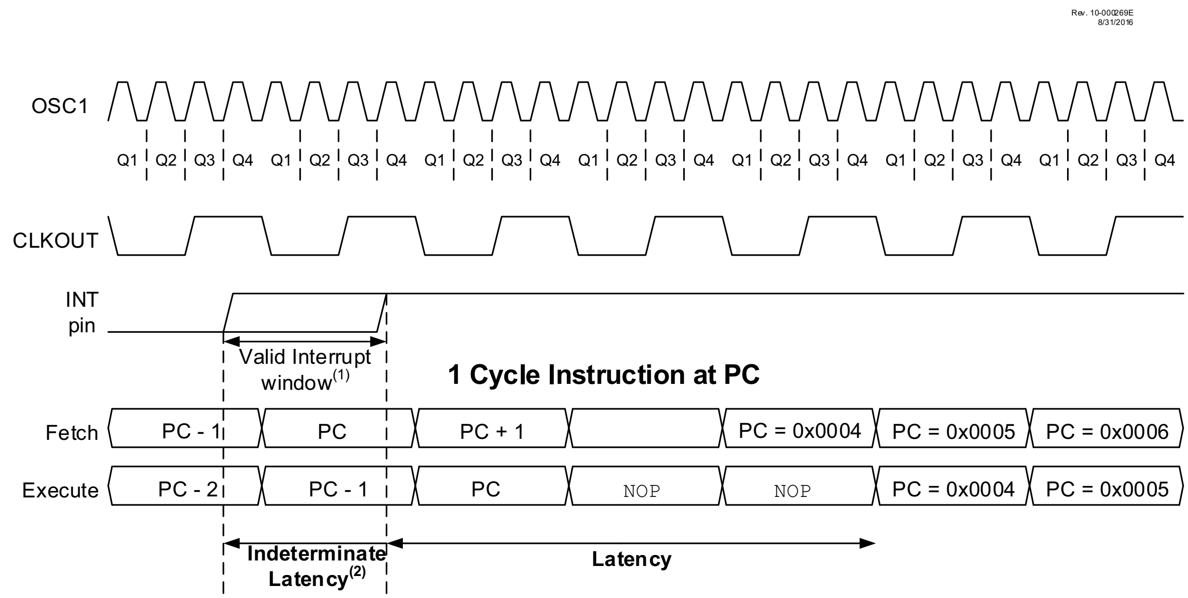
TABLE 4-4: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-31 (CONTINUED)

Address	Name	PIC16(L)F18326	PIC16(L)F18346	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
Bank 13													
				CPU CORE REGISTERS; see Table 4-2 for specifics									
68Ch	—	—		Unimplemented								—	—
68Dh	—	—		Unimplemented								—	—
68Eh	—	—		Unimplemented								—	—
68Fh	—	—		Unimplemented								—	—
690h	—	—		Unimplemented								—	—
691h	CWG1CLKCON			—	—	—	—	—	—	—	CS	`---- ---0`	`---- ---0`
692h	CWG1DAT			—	—	—	—	DAT<3:0>				`---- 0000`	`---- 0000`
693h	CWG1DBR			—	—	DBR<5:0>						`--00 0000`	`--00 0000`
694h	CWG1DBF			—	—	DBF<5:0>						`--00 0000`	`--00 0000`
695h	CWG1CON0			EN	LD	—	—	—	MODE<2:0>			`00-- -000`	`00-- -000`
696h	CWG1CON1			—	—	IN	—	POLD	POLC	POLB	POLA	`--x- 0000`	`--x- 0000`
697h	CWG1AS0			SHUTDOWN	REN	LSBD<1:0>		LSAC<1:0>		—	—	`0001 01--`	`0001 01--`
698h	CWG1AS1			—	—	—	AS4E	AS3E	AS2E	AS1E	AS0E	`---0 0000`	`---0 0000`
699h	CWG1STR			OVRD	OVRC	OVRB	OVRA	STRD	STRC	STRB	STRA	`0000 0000`	`0000 0000`
69Ah to 69Fh	—	—		Unimplemented								—	—

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.
Note 1: Only on PIC16F18326/18346.
2: Register accessible from both User and ICD Debugger.

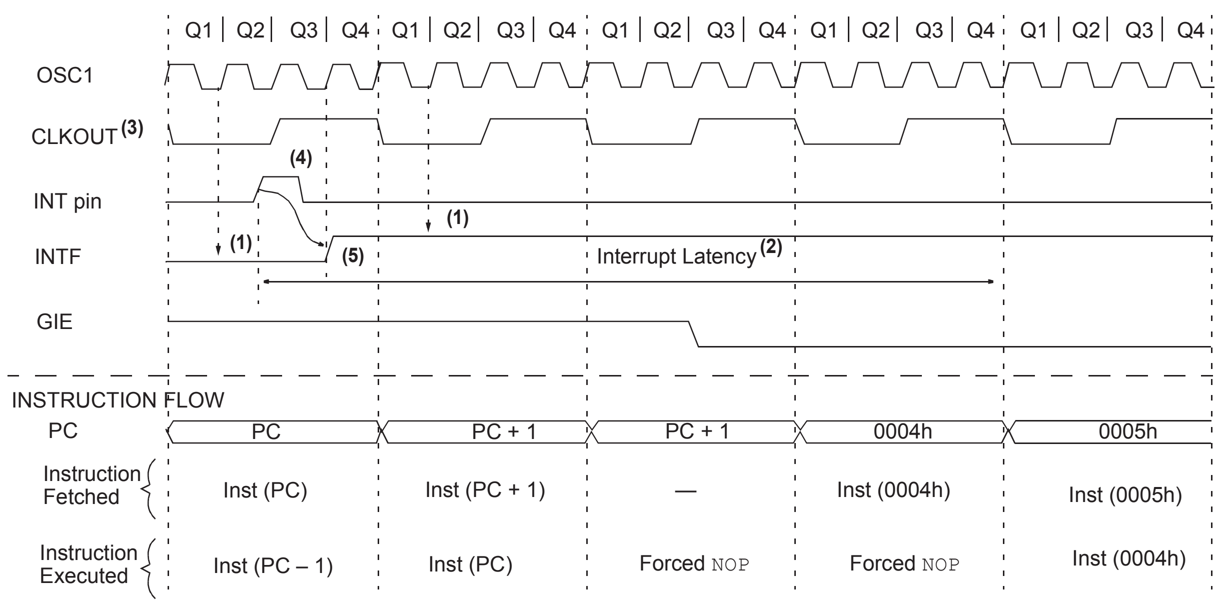
Preliminary

FIGURE 8-2: INTERRUPT LATENCY



Note 1: An interrupt may occur at any time during the interrupt window.
2: Since an interrupt may occur any time during the interrupt window, the actual latency can vary.

FIGURE 8-3: INT PIN INTERRUPT TIMING



Note 1: INTF flag is sampled here (every Q1).

2: Asynchronous interrupt latency = 3-5 TCY. Synchronous latency = 3-4 TCY, where TCY = instruction cycle time. Latency is the same whether Inst (PC) is a single cycle or a 2-cycle instruction.

3: CLKOUT not available in all oscillator modes.

4: For minimum width of INT pulse, refer to AC specifications in **Section 35.0 “Electrical Specifications”**.

5: INTF is enabled to be set any time during the Q4-Q1 cycles.

REGISTER 14-4: PMD3: PMD CONTROL REGISTER 3

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
CWG2MD	CWG1MD	PWM6MD	PWM5MD	CCP4MD	CCP3MD	CCP2MD	CCP1MD
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7 **CWG2MD:** Disable CWG2 bit
1 = CWG2 module disabled
0 = CWG2 module enabled

bit 6 **CWG1MD:** Disable CWG1 bit
1 = CWG1 module disabled
0 = CWG1 module enabled

bit 5 **PWM6MD:** Disable PWM6 bit
1 = PWM6 module disabled
0 = PWM6 module enabled

bit 4 **PWM5MD:** Disable PWM5 bit
1 = PWM5 module disabled
0 = PWM5 module enabled

bit 3 **CCP4MD:** Disable CCP4 bit
1 = CCP4 module disabled
0 = CCP4 module enabled

bit 2 **CCP3MD:** Disable CCP3 bit
1 = CCP3 module disabled
0 = CCP3 module enabled

bit 1 **CCP2MD:** Disable CCP2 bit
1 = CCP2 module disabled
0 = CCP2 module enabled

bit 0 **CCP1MD:** Disable CCP1 bit
1 = CCP1 module disabled
0 = CCP1 module enabled

15.0 INTERRUPT-ON-CHANGE

All pins on all ports can be configured to operate as Interrupt-On-Change (IOC) pins. An interrupt can be generated by detecting a signal that has either a rising edge or a falling edge. Any individual pin, or combination of pins, can be configured to generate an interrupt. The interrupt-on-change module has the following features:

- Interrupt-on-Change enable
  - Rising and falling edge detection
- Individual pin configuration
- Individual pin interrupt flags

Figure 15-1 is a block diagram of the IOC module.

15.1 Enabling the Module

To allow individual pins to generate an interrupt, the IOCIE bit of the PIE0 register must be set. If the IOCIE bit is disabled, the edge detection on the pin will still occur, but an interrupt will not be generated.

15.2 Individual Pin Configuration

For each pin, a rising edge detector and a falling edge detector are present. To enable a pin to detect a rising edge, the associated bit of the IOCxP register is set. To enable a pin to detect a falling edge, the associated bit of the IOCxN register is set.

A pin can be configured to detect rising and falling edges simultaneously by setting the associated bits in both of the IOCxP and IOCxN registers.

15.3 Interrupt Flags

The bits located in the IOCxF registers are status flags that correspond to the interrupt-on-change pins of each port. If an expected edge is detected on an appropriately enabled pin, then the status flag for that pin will be set, and an interrupt will be generated if the IOCIE bit is set. The IOCIF bit of the PIR0 register reflects the status of all IOCxF bits.

15.4 Clearing Interrupt Flags

The individual status flags, (IOCxF register bits), can be cleared by resetting them to zero. If another edge is detected during this clearing operation, the associated status flag will be set at the end of the sequence, regardless of the value actually being written.

In order to ensure that no detected edge is lost while clearing flags, only AND operations masking out known changed bits should be performed. The following sequence is an example of what should be performed.

EXAMPLE 15-1: CLEARING INTERRUPT FLAGS (PORTA EXAMPLE)

```
MOVLW  0xff
XORWF  IOCAF, W
ANDWF  IOCAF, F
```

15.5 Operation in Sleep

The interrupt-on-change interrupt event will wake the device from Sleep mode, if the IOCIE bit is set.

If an edge is detected while in Sleep mode, the affected IOCxF register will be updated prior to the first instruction executed out of Sleep.

 Preliminary

19.2 Register Definitions: PWM Control

REGISTER 19-1: PWMxCON: PWM CONTROL REGISTER

R/W-0/0	U-0	R-0	R/W-0/0	U-0	U-0	U-0	U-0
PWMxEN	—	PWMxOUT	PWMxPOL	—	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7 **PWMxEN:** PWM Module Enable bit
1 = PWM module is enabled
0 = PWM module is disabled

bit 6 **Unimplemented:** Read as ‘0’

bit 5 **PWMxOUT:** PWM Module Output Level when bit is read.

bit 4 **PWMxPOL:** PWMx Output Polarity Select bit
1 = PWM output is active-low.
0 = PWM output is active-high.

bit 3-0 **Unimplemented:** Read as ‘0’

REGISTER 19-2: PWMxDCH: PWM DUTY CYCLE HIGH BITS

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
PWMxDC<9:2>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **PWMxDC<9:2>:** PWM Duty Cycle Most Significant bits
These bits are the MSbs of the PWM duty cycle. The two LSbs are found in PWMxDCL Register.

REGISTER 19-3: PWMxDCL: PWM DUTY CYCLE LOW BITS

R/W-x/u	R/W-x/u	U-0	U-0	U-0	U-0	U-0	U-0
PWMxDC<1:0>		—	—	—	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-6 **PWMxDC<1:0>:** PWM Duty Cycle Least Significant bits
These bits are the LSbs of the PWM duty cycle. The MSbs are found in PWMxDCH Register.

bit 5-0 **Unimplemented:** Read as ‘0’

25.1 DSM Operation

The DSM module can be enabled by setting the MDEN bit in the MDCON register. Clearing the MDEN bit in the MDCON register, disables the DSM module by automatically switching the carrier high and carrier low signals to the VSS signal source. The modulator signal source is also switched to the MDBIT in the MDCON register. This not only assures that the DSM module is inactive, but that it is also consuming the least amount of current.

The values used to select the carrier high, carrier low, and modulator sources held by the Modulation Source, Modulation High Carrier, and Modulation Low Carrier control registers are not affected when the MDEN bit is cleared and the DSM module is disabled. The values inside these registers remain unchanged while the DSM is inactive. The sources for the carrier high, carrier low and modulator signals will once again be selected when the MDEN bit is set and the DSM module is again enabled and active.

The modulated output signal can be disabled without shutting down the DSM module. The DSM module will remain active and continue to mix signals, but the output value will not be sent to the DSM pin. During the time that the output is disabled, the DSM pin will remain low. The modulated output can be disabled by clearing the MDEN bit in the MDCON register.

25.2 Modulator Signal Sources

The modulator signal can be supplied from the following sources:

- CCP1 Output
- CCP2 Output
- PWM5 Output
- PWM6 Output
- MSSP1 SDO1 (SPI mode only)
- MSSP2 SDO2 (SPI mode only)
- Comparator C1 Output
- Comparator C2 Output
- EUSART1 TX Output
- External Signal on MDMIN pin
- NCO1 Output
- CLC1 Output
- CLC2 Output
- CLC3 Output
- CLC4 Output
- MDBIT bit in the MDCON register

The modulator signal is selected by configuring the MDMS <3:0> bits in the MDSRC register.

25.3 Carrier Signal Sources

The carrier high signal and carrier low signal can be supplied from the following sources:

- CCP1 Output
- CCP2 Output
- PWM5 Output
- PWM6 Output
- NCO1 Output
- FOSC (System Clock)
- HFINTOSC
- CLC1 Output
- CLC2 Output
- CLC3 Output
- CLC4 Output
- CLKR
- External Signal on MDCIN1 pin
- External Signal on MDCIN2 pin
- Vss

The carrier high signal is selected by configuring the MDCH <3:0> bits in the MDCARH register. The carrier low signal is selected by configuring the MDCL <3:0> bits in the MDCARL register.

25.4 Carrier Synchronization

During the time when the DSM switches between carrier high and carrier low signal sources, the carrier data in the modulated output signal can become truncated. To prevent this, the carrier signal can be synchronized to the modulator signal. When the modulator signal transitions away from the synchronized carrier, the unsynchronized carrier source is immediately active, while the synchronized carrier remains active until its next falling edge. When the modulator signal transitions back to the synchronized carrier, the unsynchronized carrier is immediately disabled, and the modulator waits until the next falling edge of the synchronized carrier before the synchronized carrier becomes active.

Synchronization is enabled separately for the carrier high and carrier low signal sources. Synchronization for the carrier high signal is enabled by setting the MDCHSYNC bit in the MDCARH register. Synchronization for the carrier low signal is enabled by setting the MDCLSYNC bit in the MDCARL register.

Figure 25-1 through Figure 25-6 show timing diagrams of using various synchronization methods.

REGISTER 27-3: TMRxL[1]: TIMERx LOW BYTE REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
TMRxL<7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **TMRxL<7:0>:** TMRx Low Byte bits

Note 1: ‘x’ refers to either ‘1’, ‘3’ or ‘5’ for the respective Timer1/3/5 registers.

REGISTER 27-4: TMRxH[1]: TIMERx HIGH BYTE REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
TMRxH<7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **TMRxH<7:0>:** TMRx High Byte bits

Note 1: ‘x’ refers to either ‘1’, ‘3’ or ‘5’ for the respective Timer1/3/5 registers.

REGISTER 29-3: CCPRxL REGISTER: CCPx REGISTER LOW BYTE

R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x
CCPRxL<7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Reset
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0
CCPxMODE = Capture mode
CCPRxL<7:0>: Captured value of TMR1/3/5L
CCPxMODE = Compare mode
CCPRxL<7:0>: LS Byte compared to TMR1/3/5L
CCPxMODE = PWM modes when CCPxFMT = 0
CCPRxL<7:0>: CCPW<7:0> – Pulse-width Least Significant eight bits
CCPxMODE = PWM modes when CCPxFMT = 1
CCPRxL<7:6>: CCPW<1:0> – Pulse-width Least Significant two bits
CCPRxL<5:0>: Not used.

REGISTER 29-4: CCPRxH REGISTER: CCPx REGISTER HIGH BYTE

R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x
CCPRxH<7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Reset
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0
CCPxMODE = Capture mode
CCPRxH<7:0>: Captured value of TMR1/3/5H
CCPxMODE = Compare mode
CCPRxH<7:0>: MS Byte compared to TMR1/3/5H
CCPxMODE = PWM modes when CCPxFMT = 0
CCPRxH<7:2>: Not used
CCPRxH<1:0>: CCPW<9:8> – Pulse-width Most Significant two bits
CCPxMODE = PWM modes when CCPxFMT = 1
CCPRxH<7:0>: CCPW<9:2> – Pulse-width Most Significant eight bits

TABLE 29-4: SUMMARY OF REGISTERS ASSOCIATED WITH CCPx

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
TRISA	—	—	TRISA5	TRISA4	—(2)	TRISA2	TRISA1	TRISA0	143
ANSELA	—	—	ANSA5	ANSA4	—	ANSA2	ANSA1	ANSA0	144
TRISB(1)	TRISB7	TRISB6	TRISB5	TRISB4	—	—	—	—	149
ANSELB(1)	ANSB7	ANSB6	ANSB5	ANSB4	—	—	—	—	150
TRISC	TRISC7(1)	TRISC6(1)	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	155
ANSELC	ANSC7(1)	ANSC6(1)	ANSC5	ANSC4	ANSC3	ANSC2	ANSC1	ANSC0	157
INTCON	GIE	PEIE	—	—	—	—	—	INTEDG	100
PIR4	CWG2IF	CWG1IF	TMR5GIF	TMR5IF	CCP4IF	CCP3IF	CCP2IF	CCP1IF	110
PIE4	CWG2IE	CWGIE	TMR5GIE	TMR5IE	CCP4IE	CCP3IE	CCP2IE	CCP1IE	105
CCPxCON	CCPxEN	—	CCPxOUT	CCPxFMT	CCPxMODE<3:0>				308
CCPxCAP	—	—	—	—	CCPxCTS<3:0>				309
CCPRxL	CCPRx<7:0>								310
CCPRxH	CCPRx<15:8>								310
CCPTMRS	C4TSEL<1:0>		C3TSEL<1:0>		C2TSEL<1:0>		C1TSEL<1:0>		311
CCP1PPS	—	—	—	CCP1PPS<4:0>					162
CCP2PPS	—	—	—	CCP2PPS<4:0>					162
CCP3PPS	—	—	—	CCP3PPS<4:0>					162
CCP4PPS	—	—	—	CCP4PPS<4:0>					162
RxyPPS	—	—	—	RxyPPS<4:0>					163
ADACT	—	—	—	ADACT<4:0>					246
CLCxSELy	—	—	LCxDyS<5:0>						229
CWGxDAT	—	—	—	—	DAT<3:0>				215
MDSRC	—	—	—	—	MDMS<3:0>				272
MDCARH	—	MDCHPOL	MDCHSYNC	—	MDCH<3:0>				273
MDCARL	—	MDCLPOL	MDCLSYNC	—	MDCL<3:0>				274

Legend: — = Unimplemented location, read as ‘0’. Shaded cells are not used by the CCP module.
Note 1: PIC16(L)F18346 only.
2: Unimplemented, read as ‘1’.

FIGURE 30-9: SPI MODE WAVEFORM (SLAVE MODE WITH CKE = 0)

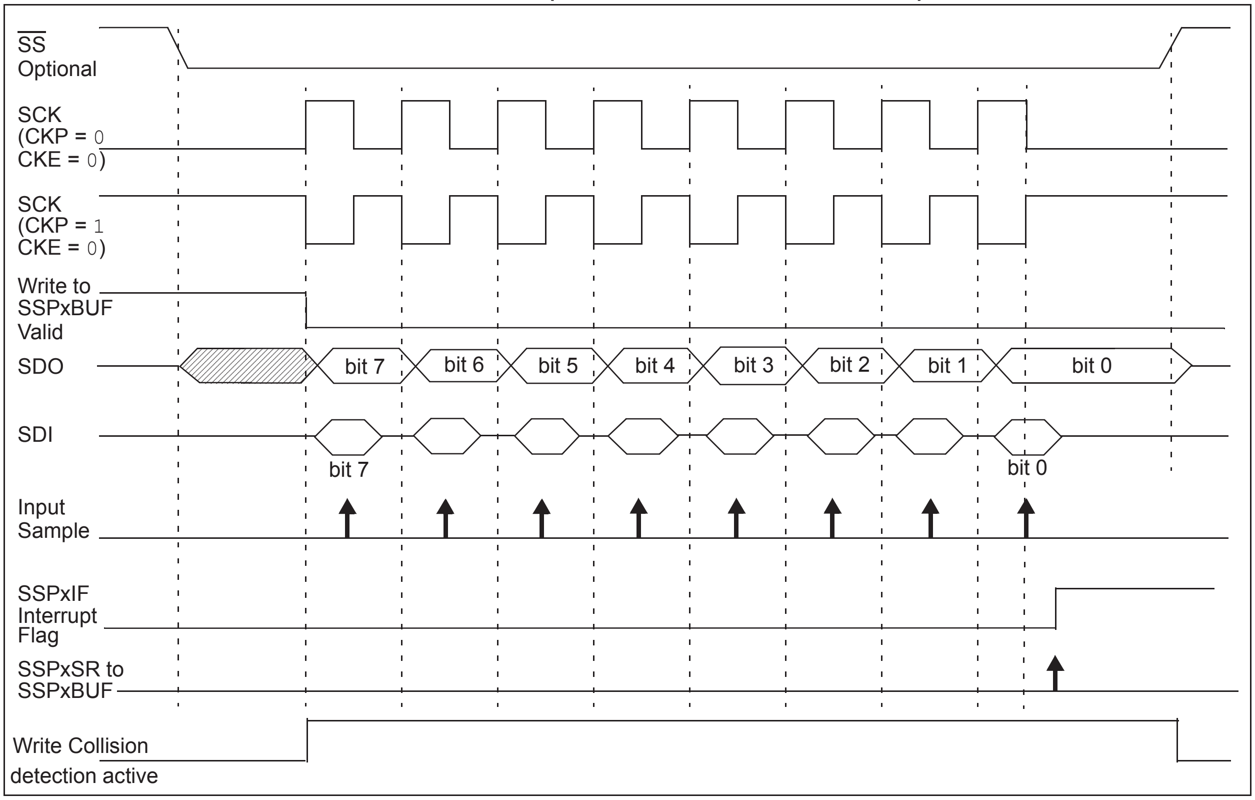
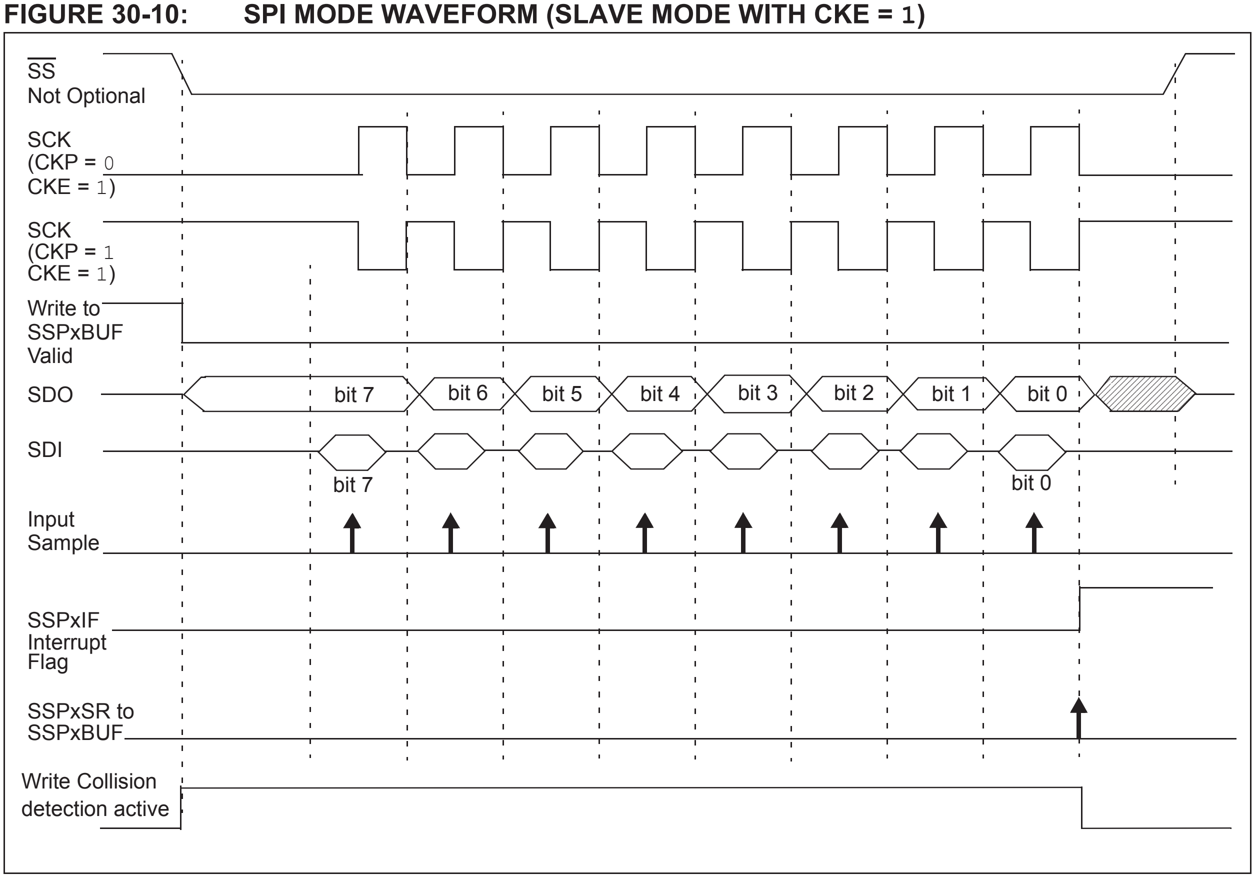


FIGURE 30-10: SPI MODE WAVEFORM (SLAVE MODE WITH CKE = 1)



30.2.6 SPI OPERATION IN SLEEP MODE

In SPI Master mode, when the Sleep mode is selected, all module clocks are halted and the transmission/reception will remain in that state until the device wakes. After the device returns to Run mode, the module will resume transmitting and receiving data.

In SPI Slave mode, the SPI Transmit/Receive Shift register operates asynchronously to the device. This allows the device to be placed in Sleep mode and data to be shifted into the SPI Transmit/Receive Shift register. When all eight bits have been received, the MSSP interrupt flag bit will be set and if enabled, will wake the device.

30.3 I^{2}C Mode Overview

The Inter-Integrated Circuit (I^{2}C) bus is a multi-master serial data communication bus. Devices communicate in a master/slave environment where the master devices initiate the communication. A slave device is controlled through addressing.

The I^{2}C bus specifies two signal connections:

- Serial Clock (SCL)
- Serial Data (SDA)

Figure 30-11 shows the block diagram of the MSSPx module when operating in I^{2}C mode.

Both the SCL and SDA connections are bidirectional open-drain lines, each requiring pull-up resistors for the supply voltage. Pulling the line to ground is considered a logical zero and letting the line float is considered a logical one.

Figure 30-2 and Figure 30-3 show a typical connection between two processors configured as master and slave devices.

The I^{2}C bus can operate with one or more master devices and one or more slave devices.

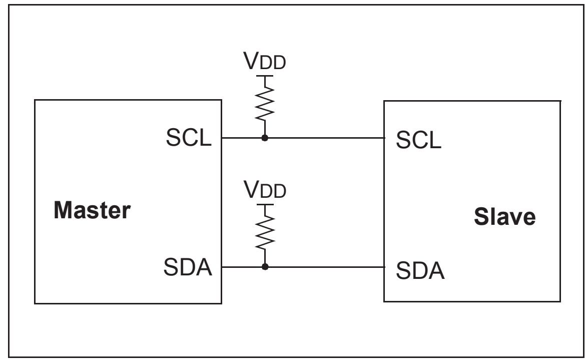
There are four potential modes of operation for a given device:

- Master Transmit mode
  (master is transmitting data to a slave)
- Master Receive mode
  (master is receiving data from a slave)
- Slave Transmit mode
  (slave is transmitting data to a master)
- Slave Receive mode
  (slave is receiving data from the master)

To begin communication, the master device sends out a Start condition followed by the address byte of the slave it intends to communicate with. This is followed by a single Read/Write bit, which determines whether the master intends to transmit to or receive data from the slave device.

If the requested slave exists on the bus, it will respond with an Acknowledge bit, otherwise known as an $\overline{\text{ACK}}$. The master then continues in either transmit or receive data from the slave device.

FIGURE 30-11: I^{2}C MASTER/ SLAVE CONNECTION



On the last byte of data communicated, the master device may end the transmission by sending a Stop bit. If the master device is in Receive mode, it sends a $\overline{\text{NACK}}$ in place of the last $\overline{\text{ACK}}$ bit. A Stop bit is indicated by a low-to-high transition of the SDA line while the SCL line is held high.

In some cases, the master may want to maintain control of the bus and re-initiate another transmission. If so, the master device may send a Restart condition in place of the Stop bit or last $\overline{\text{ACK}}$ bit when it is in Receive mode.

The I^{2}C bus specifies three message protocols;

- Single message where a master writes data to a slave.
- Single message where a master reads data from a slave.
- Combined message where a master initiates a minimum of two writes, or two reads, or a combination of writes and reads, to one or more slaves.

30.3.1 CLOCK STRETCHING

When a slave device has not completed processing data, it can delay the transfer of more data through the process of clock stretching. An addressed slave device may hold the SCL clock line low after receiving or sending a bit, indicating that it is not yet ready to continue. The master that is communicating with the slave will attempt to raise the SCL line in order to transfer the next bit, but will detect that the clock line has not yet been released. Because the SCL connection is open-drain, the slave has the ability to hold that line low until it is ready to continue communicating.

Clock stretching allows receivers that cannot keep up with a transmitter to control the flow of incoming data.

31.1.1.5 TSR Status

The TRMT bit of the TX1STA register indicates the status of the TSR register. This is a read-only bit. The TRMT bit is set when the TSR register is empty and is cleared when a character is transferred to the TSR register from the TX1REG. The TRMT bit remains clear until all bits have been shifted out of the TSR register. No interrupt logic is tied to this bit, so the user has to poll this bit to determine the TSR status.

Note:	The TSR register is not mapped in data memory, so it is not available to the user.

31.1.1.6 Transmitting 9-bit Characters

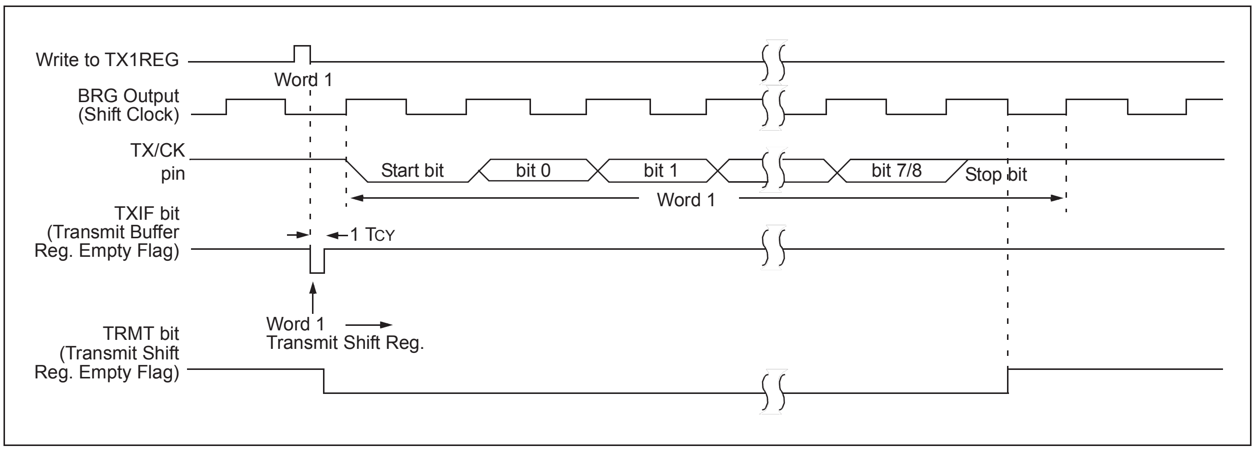
The EUSART1 supports 9-bit character transmissions. When the TX9 bit of the TX1STA register is set, the EUSART1 will shift nine bits out for each character transmitted. The TX9D bit of the TX1STA register is the ninth, and Most Significant data bit. When transmitting 9-bit data, the TX9D data bit must be written before writing the eight Least Significant bits into the TX1REG. All nine bits of data will be transferred to the TSR shift register immediately after the TX1REG is written.

A special 9-bit Address mode is available for use with multiple receivers. See **Section 31.1.2.7 “Address Detection”** for more information on the Address mode.

31.1.1.7 Asynchronous Transmission Setup

1. Initialize the SP1BRGH, SP1BRGL register pair and the BRGH and BRG16 bits to achieve the desired baud rate (see **Section 31.3 “EUSART1 Baud Rate Generator (BRG)”**).
2. Enable the asynchronous serial port by clearing the SYNC bit and setting the SPEN bit.
3. If 9-bit transmission is desired, set the TX9 control bit. A set ninth data bit will indicate that the eight Least Significant data bits are an address when the receiver is set for address detection.
4. Set SCKP bit if inverted transmit is desired.
5. Enable the transmission by setting the TXEN control bit. This will cause the TXIF interrupt bit to be set.
6. If interrupts are desired, set the TXIE interrupt enable bit of the PIE1 register. An interrupt will occur immediately provided that the GIE and PEIE bits of the INTCON register are also set.
7. If 9-bit transmission is selected, the ninth bit should be loaded into the TX9D data bit.
8. Load 8-bit data into the TX1REG register. This will start the transmission.

FIGURE 31-3: ASYNCHRONOUS TRANSMISSION



REGISTER 32-1: CLKRCON: REFERENCE CLOCK CONTROL REGISTER

R/W-0/0	U-0	U-0	R/W-1/1	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
CLKREN	—	—	CLKRDC<1:0>		CLKRDIV<2:0>		
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **CLKREN:** Reference Clock Module Enable bit
- `1` = Reference clock module enabled
- `0` = Reference clock module is disabled

bit 6-5 **Unimplemented:** Read as '`0`'

bit 4-3 **CLKRDC<1:0>:** Reference Clock Duty Cycle bits (1)
- `11` = Clock outputs duty cycle of 75%
- `10` = Clock outputs duty cycle of 50%
- `01` = Clock outputs duty cycle of 25%
- `00` = Clock outputs duty cycle of 0%

bit 2-0 **CLKRDIV<2:0>:** Reference Clock Divider bits
- `111` = FOSC divided by 128
- `110` = FOSC divided by 64
- `101` = FOSC divided by 32
- `100` = FOSC divided by 16
- `011` = FOSC divided by 8
- `010` = FOSC divided by 4
- `001` = FOSC divided by 2
- `000` = FOSC

Note 1: Bits are valid for Reference Clock divider values of two or larger, the base clock cannot be further divided.

TABLE 32-1: SUMMARY OF REGISTERS ASSOCIATED WITH CLOCK REFERENCE OUTPUT

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
TRISA	—	—	TRISA5	TRISA4	—(2)	TRISA2	TRISA1	TRISA0	143
TRISB(1)	TRISB7	TRISB6	TRISB5	TRISB4	—	—	—	—	149
TRISC	TRISC7(1)	TRISC6(1)	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	155
CLKRCON	CLKREN	—	—	CLKRDC<1:0>		CLKRDIV<2:0>			227
CLCxSELy	—	—	LCxDyS<5:0>						229
MDCARH	—	MDCHPOL	MDCHSYNC	—	MDCH<3:0>				273
MDCARL	—	MDCLPOL	MDCLSYNC	—	MDCL<3:0>				274

Legend: — = unimplemented, read as '`0`'. Shaded cells are not used by the CLKR module.
Note 1: PIC16(L)F18346 only.
2: Unimplemented, read as '`1`'.

TABLE 35-4: I/O PORTS(1)

Param. No.	Sym.	Characteristic	Min.	Typ.†	Max.	Units	Conditions
DC CHARACTERISTICS			**Standard Operating Conditions (unless otherwise stated)**				
	V_{IL}	**Input Low Voltage**					
		I/O PORT:					
D300		with TTL buffer	—	—	0.8	V	4.5V ≤ V_{DD} ≤ 5.5V
D301			—	—	0.15 V_{DD}	V	1.8V ≤ V_{DD} ≤ 4.5V
D302		with Schmitt Trigger buffer	—	—	0.2 V_{DD}	V	2.0V ≤ V_{DD} ≤ 5.5V
D303		with I^2C levels	—	—	0.3 V_{DD}	V	
D304		with SMBus levels	—	—	0.8	V	2.7V ≤ V_{DD} ≤ 5.5V
D305		$\overline{MCLR}$	—	—	0.2 V_{DD}	V	
	V_{IH}	**Input High Voltage**					
		I/O PORT:					
D320		with TTL buffer	2.0	—	—	V	4.5V ≤ V_{DD} ≤ 5.5V
D321			0.25 V_{DD} + 0.8	—	—	V	1.8V ≤ V_{DD} ≤ 4.5V
D322		with Schmitt Trigger buffer	0.8 V_{DD}	—	—	V	2.0V ≤ V_{DD} ≤ 5.5V
D323		with I^2C levels	0.7 V_{DD}	—	—	V	
D324		with SMBus levels	2.1	—	—	V	2.7V ≤ V_{DD} ≤ 5.5V
D325		$\overline{MCLR}$	0.7 V_{DD}	—	—	V	
	I_{IL}	**Input Leakage Current(2)**					
D340		I/O Ports	—	± 5	± 125	nA	V_{SS} ≤ V_{PIN} ≤ V_{DD}, Pin at high-impedance, 85°C
D341			—	± 5	± 1000	nA	V_{SS} ≤ V_{PIN} ≤ V_{DD}, Pin at high-impedance, 125°C
D342		$\overline{MCLR}$(2)	—	± 50	± 200	nA	V_{SS} ≤ V_{PIN} ≤ V_{DD}, Pin at high-impedance, 85°C
	I_{PUR}	**Weak Pull-up Current**					
D350			25	120	200	μA	V_{DD} = 3.0V, V_{PIN} = V_{SS}
	V_{OL}	**Output Low Voltage(3)**					
D360		I/O ports	—	—	0.6	V	I_{OL} = 10.0 mA, V_{DD} = 3.0V
	V_{OH}	**Output High Voltage(3)**					
D370		I/O ports	V_{DD} - 0.7	—	—	V	I_{OH} = 6.0 mA, V_{DD} = 3.0V
D380	C_{IO}	**All I/O pins**	—	5	50	pF	

* These parameters are characterized but not tested.

† Data in "Typ." column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Negative current is defined as current sourced by the pin.

2: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Excluding OSC2 in CLKOUT mode.

TABLE 35-5: I/O AND CLOCK TIMING SPECIFICATIONS

Standard Operating Conditions (unless otherwise stated)							
Param. No.	Sym.	Characteristic	Min.	Typ.†	Max.	Units	Conditions
High Voltage Entry Programming Mode Specifications							
MEM01	VIHH	Voltage on $\overline{MCLR}$/VPP pin to enter Programming mode	8	—	9	V	**Note 2**
MEM02	IPPGM	Current on $\overline{MCLR}$/VPP pin during Programming mode	—	—	600	uA	**Note 2**
Programming Mode Specifications							
MEM10	VBE	VDD for Bulk Erase	—	2.7	—	V	
MEM11	IDDPGM	Supply Current during Programming Operation	—	—	3	mA	
Data EEPROM Memory Specifications							
MEM20	ED	DataEE Byte Endurance	100k	—	—	E/W	-40°C ≤ TA ≤ 85°C
MEM21	TD_RET	Characteristic Retention	—	40	—	Year	Provided no other specifications are violated
MEM22	ND_REF	Total Erase/Write Cycles before Refresh	—	—	100k	E/W	
MEM23	VD_RW	VDD for Read or Erase/Write Operation	VDDMIN	—	VDDMAX	V	
MEM24	TD_BEW	Byte Erase and Write Cycle Time	—	4.0	5.0	ms	
Program Flash Memory Specifications							
MEM30	EP	Flash Memory Cell Endurance	10k	—	—	E/W	-40°C ≤ TA ≤ 85°C **(Note 1)**
MEM31	EPHEF	High-Endurance Flash Memory Cell Endurance	100k	—	—	E/W	TBD
MEM32	TP_RET	Characteristic Retention	—	40	—	Year	Provided no other specifications are violated
MEM33	VP_RD	VDD for Read Operation	VDDMIN	—	VDDMAX	V	
MEM34	VP_REW	VDD for Row Erase or Write Operation	VDDMIN	—	VDDMAX	V	
MEM35	TP_REW	Self-Timed Row Erase or Self-Timed Write	—	2.0	2.5	ms	

† Data in “Typ.” column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Flash Memory Cell Endurance for the Flash memory is defined as: One Row Erase operation and one Self-Timed Write.

2: Required only if CONFIG3.LVP is disabled.

TABLE 35-9: PLL CLOCK TIMING SPECIFICATIONS

Standard Operating Conditions (unless otherwise stated)							
Param. No.	Sym.	Characteristic	Min.	Typ.†	Max.	Units	Conditions
PLL01	FPLLIN	PLL Input Frequency Range	4	—	8	MHz	
PLL02	FPLLOUT	PLL Output Frequency Range	16	—	32	MHz	
PLL03	TPLLST	PLL Lock Time from Start-up	—	200	—	μs	
PLL04	FPLLJIT	PLL Output Frequency Stability (Jitter)	-0.25	—	0.25	%	

* These parameters are characterized but not tested.

† Data in “Typ.” column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 35-7: CLKOUT AND I/O TIMING

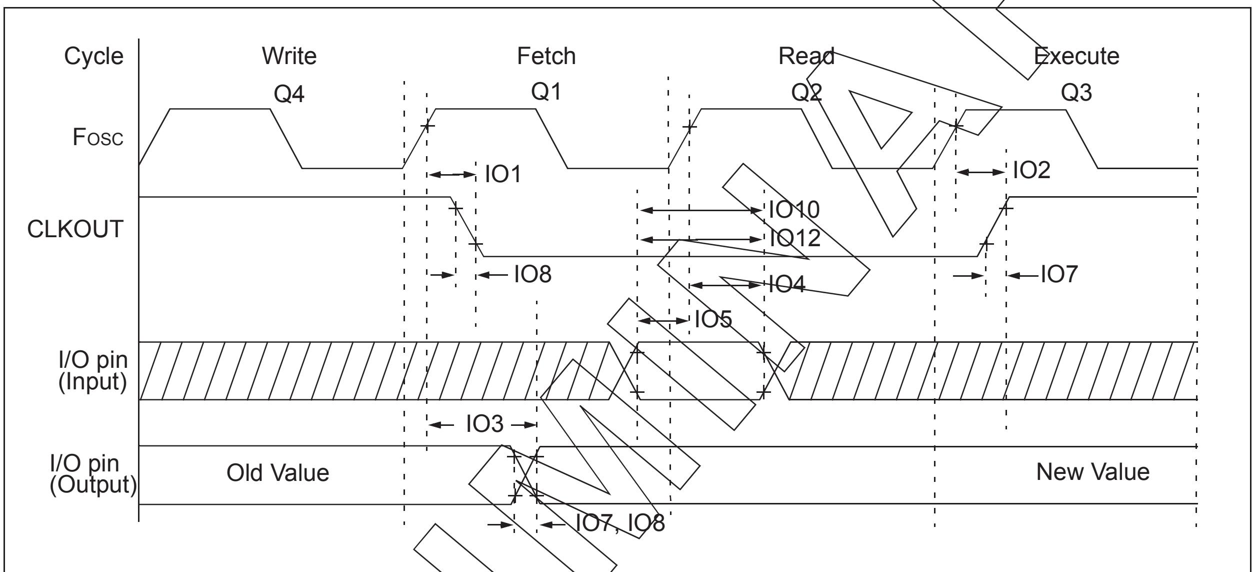
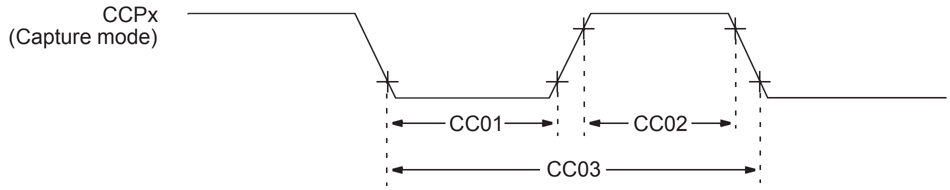


FIGURE 35-13: CAPTURE/COMPARE/PWM TIMINGS (CCP)



Note: Refer to Figure 35-4 for Load conditions.

TABLE 35-18: CAPTURE/COMPARE/PWM CHARACTERISTICS (CCP)

Standard Operating Conditions (unless otherwise stated)								
Param. No.	**Sym.**	**Characteristic**		**Min.**	**Typ.†**	**Max.**	**Units**	**Conditions**
CC01*	T_{ccL}	CCPx Input Low Time	No Prescaler	$0.5T_{CY}$ + 20	—	—	ns	
			With Prescaler	20	—	—	ns	
CC02*	T_{ccH}	CCPx Input High Time	No Prescaler	$0.5T_{CY}$ + 20	—	—	ns	
			With Prescaler	20	—	—	ns	
CC03*	T_{ccP}	CCPx Input Period		$\frac{3T_{CY} + 40}{N}$	—	—	ns	N = prescale value

* These parameters are characterized but not tested.

† Data in "Typ." column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

36.0 DC AND AC CHARACTERISTICS GRAPHS AND CHARTS

Charts and graphs are not available at this time.