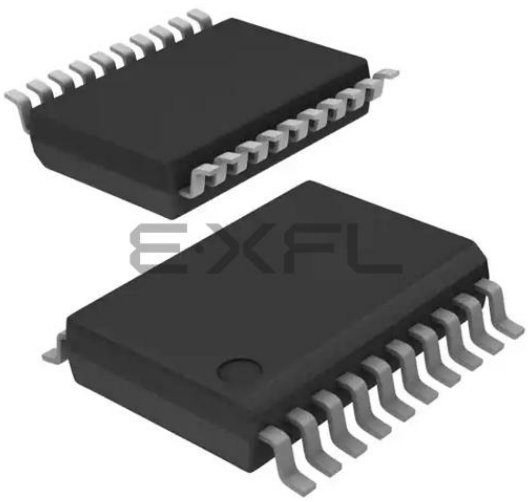

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	18
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 17x10b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf18346-i-ss

TABLE 4-4: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-31 (CONTINUED)

Address	Name	PIC16(L)F18326	PIC16(L)F18346	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
Bank 13													
CPU CORE REGISTERS; see Table 4-2 for specifics													
68Ch	—	—		Unimplemented								—	—
68Dh	—	—		Unimplemented								—	—
68Eh	—	—		Unimplemented								—	—
68Fh	—	—		Unimplemented								—	—
690h	—	—		Unimplemented								—	—
691h	CWG1CLKCON			—	—	—	—	—	—	—	CS	---- ---0	---- ---0
692h	CWG1DAT			—	—	—	—	DAT<3:0>				---- 0000	---- 0000
693h	CWG1DBR			—	—	DBR<5:0>						--00 0000	--00 0000
694h	CWG1DBF			—	—	DBF<5:0>						--00 0000	--00 0000
695h	CWG1CON0			EN	LD	—	—	—	MODE<2:0>			00-- -000	00-- -000
696h	CWG1CON1			—	—	IN	—	POLD	POLC	POLB	POLA	--x- 0000	--x- 0000
697h	CWG1AS0			SHUTDOWN	REN	LSBD<1:0>		LSAC<1:0>		—	—	0001 01--	0001 01--
698h	CWG1AS1			—	—	—	AS4E	AS3E	AS2E	AS1E	AS0E	---0 0000	---0 0000
699h	CWG1STR			OVRD	OVRC	OVRB	OVRA	STRD	STRC	STRB	STRA	0000 0000	0000 0000
69Ah to 69Fh	—	—		Unimplemented								—	—

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.
Note 1: Only on PIC16F18326/18346.
2: Register accessible from both User and ICD Debugger.

TABLE 4-4: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-31 (CONTINUED)

Address	Name	PIC16(L)F18326	PIC16(L)F18346	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
Bank 14													
CPU CORE REGISTERS; see Table 4-2 for specifics													
70Ch	—	—		Unimplemented								—	—
70Dh	—	—		Unimplemented								—	—
70Eh	—	—		Unimplemented								—	—
70Fh	—	—		Unimplemented								—	—
710h	—	—		Unimplemented								—	—
711h	CWG2CLKCON			—	—	—	—	—	—	—	CS	`---- ---0`	`---- ---0`
712h	CWG2DAT			—	—	—	—	DAT<3:0>				`---- 0000`	`---- 0000`
713h	CWG2DBR			—	—	DBR<5:0>						`--00 0000`	`--00 0000`
714h	CWG2DBF			—	—	DBF<5:0>						`--00 0000`	`--00 0000`
715h	CWG2CON0			EN	LD	—	—	—	MODE<2:0>			`00-- -000`	`00-- -000`
716h	CWG2CON1			—	—	IN	—	POLD	POLC	POLB	POLA	`--x- 0000`	`--x- 0000`
717h	CWG2AS0			SHUTDOWN	REN	LSBD<1:0>		LSAC<1:0>		—	—	`0001 01--`	`0001 01--`
718h	CWG2AS1			—	—	—	AS4E	AS3E	AS2E	AS1E	AS0E	`---0 0000`	`---0 0000`
719h	CWG2STR			OVRD	OVRC	OVRB	OVRA	STRD	STRC	STRB	STRA	`0000 0000`	`0000 0000`
71Ah to 71Fh	—	—		Unimplemented								—	—

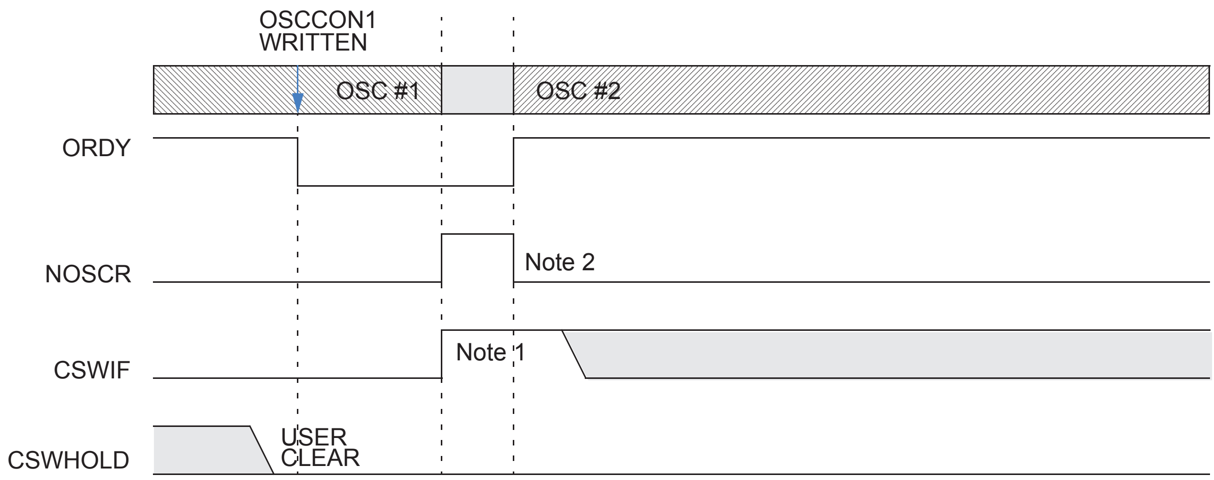
Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Only on PIC16F18326/18346.

2: Register accessible from both User and ICD Debugger.

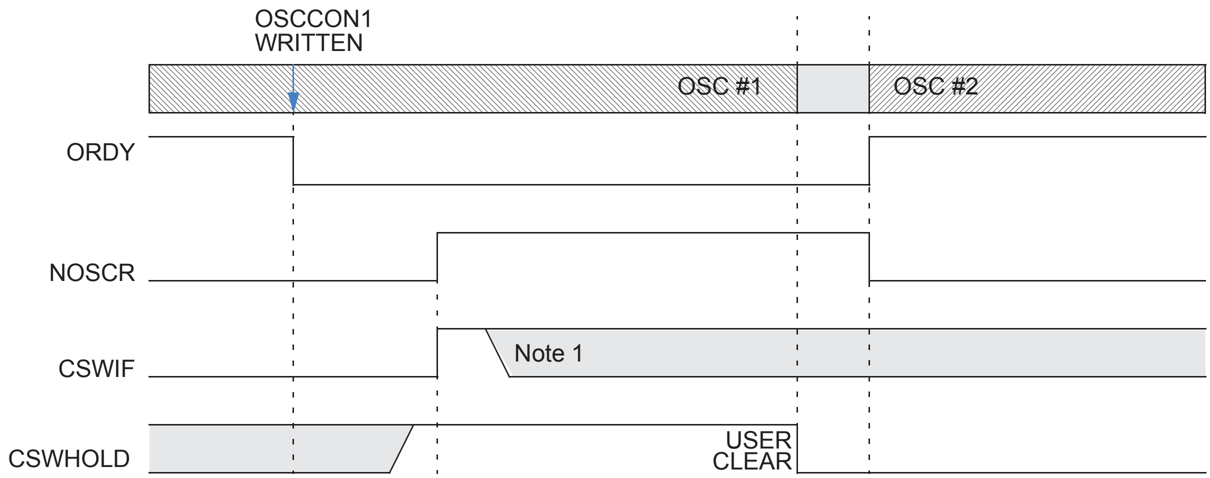
Preliminary

FIGURE 7-6: CLOCK SWITCH (CSWHOLD = 0)



Note 1: CSWIF is asserted coincident with NOSCR; interrupt is serviced at OSC#2 speed.
2: The assertion of NOSCR is hidden from the user because it appears only for the duration of the switch.

FIGURE 7-7: CLOCK SWITCH (CSWHOLD = 1)



Note 1: CSWIF is asserted coincident with NOSCR, and may be cleared before or after clearing CSWHOLD = 0.

REGISTER 8-3: PIE1: PERIPHERAL INTERRUPT ENABLE REGISTER 1

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	BCL1IE	TMR2IE	TMR1IE
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7 **TMR1GIE:** Timer1 Gate Interrupt Enable bit
1 = Enables the Timer1 gate acquisition interrupt
0 = Disables the Timer1 gate acquisition interrupt

bit 6 **ADIE:** Analog-to-Digital Converter (ADC) Interrupt Enable bit
1 = Enables the ADC interrupt
0 = Disables the ADC interrupt

bit 5 **RCIE:** EUSART Receive Interrupt Enable bit
1 = Enables the EUSART receive interrupt
0 = Disables the EUSART receive interrupt

bit 4 **TXIE:** EUSART Transmit Interrupt Enable bit
1 = Enables the EUSART transmit interrupt
0 = Disables the EUSART transmit interrupt

bit 3 **SSP1IE:** Synchronous Serial Port (MSSP) Interrupt Enable bit
1 = Enables the MSSP interrupt
0 = Disables the MSSP interrupt

bit 2 **BCL1IE:** MSSP1 Bus Collision Interrupt Enable bit
1 = MSSP bus collision interrupt enabled
0 = MSSP bus collision interrupt not enabled

bit 1 **TMR2IE:** TMR2 to PR2 Match Interrupt Enable bit
1 = Enables the Timer2 to PR2 match interrupt
0 = Disables the Timer2 to PR2 match interrupt

bit 0 **TMR1IE:** Timer1 Overflow Interrupt Enable bit
1 = Enables the Timer1 overflow interrupt
0 = Disables the Timer1 overflow interrupt

Note: Bit PEIE of the INTCON register must be set to enable any peripheral interrupt.

REGISTER 8-4: PIE2: PERIPHERAL INTERRUPT ENABLE REGISTER 2

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
TMR6IE	C2IE	C1IE	NVMIE	SSP2IE	BCL2IE	TMR4IE	NCO1IE
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7 **TMR6IE:** TMR6 to PR6 Match Interrupt Enable bit
1 = TMR6 to PR6 match interrupt is enabled
0 = TMR6 to PR6 match is not enabled

bit 6 **C2IE:** Comparator C2 Interrupt Enable bit
1 = Enables the Comparator C2 interrupt
0 = Disables the Comparator C2 interrupt

bit 5 **C1IE:** Comparator C1 Interrupt Enable bit
1 = Enables the Comparator C1 interrupt
0 = Disables the Comparator C1 interrupt

bit 4 **NVMIE:** NVM Interrupt Enable Bit
1 = ENVM task complete interrupt enabled
0 = NVM interrupt not enabled

bit 3 **SSP2IE:** Master Synchronous Serial Port (MSSP2) Interrupt Enable bit
1 = Enables the MSSP2 interrupt
0 = Disables the MSSP2 interrupt

bit 2 **BCL2IE:** MSSP2 Bus Collision Interrupt Enable bit
1 = MSSP bus collision interrupt enabled
0 = MSSP bus collision interrupt not enabled

bit 1 **TMR4IE:** TMR4 to PR4 Match Interrupt Enable bit
1 = TMR4 to PR4 match interrupt is enabled
0 = TMR4 to PR4 match is not enabled

bit 0 **NCO1IE:** NCO Interrupt Enable bit
1 = NCO rollover interrupt enabled
0 = NCO rollover interrupt not enabled

Note: Bit PEIE of the INTCON register must be set to enable any peripheral interrupt.

13.8 Register Definitions: PPS Input Selection

REGISTER 13-1: xxxPPS: PERIPHERAL xxx INPUT SELECTION

U-0	U-0	U-0	R/W-q/u	R/W-q/u	R/W-q/u	R/W-q/u	R/W-q/u
—	—	—	xxxPPS<4:0>				
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	q = value depends on peripheral

bit 7-5 **Unimplemented:** Read as ‘0’

bit 4-0 **xxxPPS<4:0>:** Peripheral xxx Input Selection bits
11xxx = Reserved. Do not use.

10111 = Peripheral input is RC7(1)
10110 = Peripheral input is RC6(1)
10101 = Peripheral input is RC5
10100 = Peripheral input is RC4
10011 = Peripheral input is RC3
10010 = Peripheral input is RC2
10001 = Peripheral input is RC1
10000 = Peripheral input is RC0
...
01111 = Peripheral input is RB7(1)
01110 = Peripheral input is RB6(1)
01101 = Peripheral input is RB5(1)
01100 = Peripheral input is RB4(1)
...
0011x = Reserved. Do not use.
00101 = Peripheral input is RA5
00100 = Peripheral input is RA4
00011 = Peripheral input is RA3
00010 = Peripheral input is RA2
00001 = Peripheral input is RA1
00000 = Peripheral input is RA0

Note 1: PIC16(L)F18346 only.

19.0 PULSE-WIDTH MODULATION (PWM)

The PWMx modules generate Pulse-Width Modulated (PWM) signals of varying frequency and duty cycle.

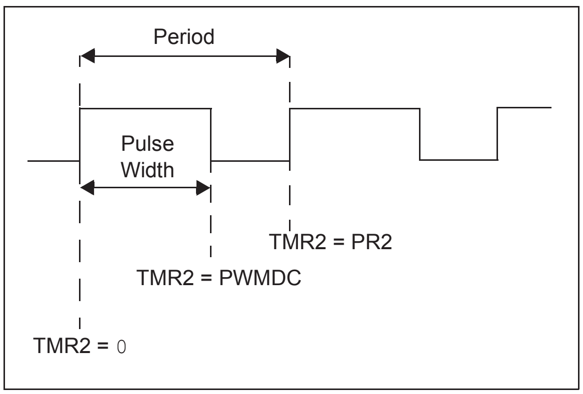
In addition to the CCP modules, the PIC16(L)F18326/18346 devices contain two PWM modules.

Pulse-Width Modulation (PWM) is a scheme that provides power to a load by switching quickly between fully on and fully off states. The PWM signal resembles a square wave where the high portion of the signal is considered the ON state (pulse width), and the low portion of the signal is considered the OFF state. The term duty cycle describes the proportion of the ON time to the OFF time and is expressed in percentages, where 0% is fully OFF and 100% is fully ON. A lower duty cycle corresponds to less power applied and a higher duty cycle corresponds to more power applied. The PWM period is defined as the duration of one complete cycle or the total amount of on and off time combined.

PWM resolution defines the maximum number of steps that can be present in a single PWM period. A higher resolution allows for more precise control of the pulse-width time and in turn the power that is applied to the load.

Figure 19-1 shows a typical waveform of the PWM signal.

FIGURE 19-1: PWM OUTPUT



19.1 Standard PWM Mode

The standard PWM mode generates a Pulse-Width Modulation (PWM) signal on the PWMx pin with up to ten bits of resolution. The period, duty cycle, and resolution are controlled by the following registers:

- TMR2, TMR4 or TMR6 registers
- PR2, PR4 or PR6 registers
- PWMxCON registers
- PWMxDCH registers
- PWMxDCL registers

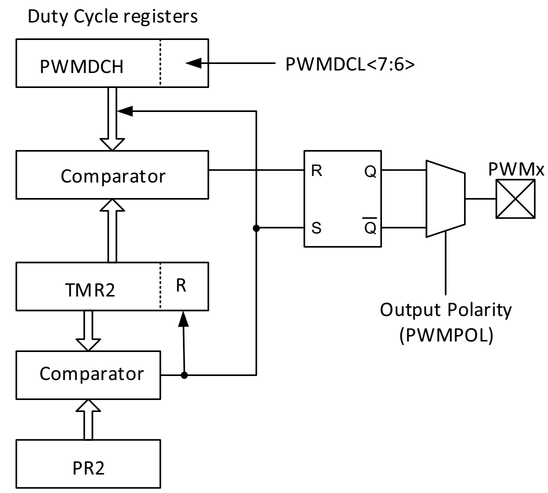
Figure 29-2 shows a simplified block diagram of the PWM operation.

If PWMPOL = 0, the default state of the output is '0'. If PWMPOL = 1, the default state is '1'. If PWMEN = 0, the output will be the default state.

Note:	The corresponding TRIS bit must be cleared to enable the PWM output on the PWMx pin

Note:	The formulas and text refer to TMR2 and PR2, for simplicity. The same formulas and text apply to TMR4/6 and PR4/6. The timer sources can be selected in Register 19-4. For additional information on TMR2/4/6, refer to **Section 28.0 "Timer 2/4/6 Module"**

FIGURE 19-2: SIMPLIFIED PWM BLOCK DIAGRAM



19.1.1 PWM PERIOD

Referring to Figure 19-1, the PWM output has a period and a pulse width. The frequency of the PWM is the inverse of the period (1/period).

The PWM period is specified by writing to the PR2 register. The PWM period can be calculated using the following formula:

EQUATION 19-1: PWM PERIOD

$$PWM\ Period = [(PR2) + 1] \bullet 4 \bullet TOSC \bullet (TMR2\ Prescale\ Value)$$

Note: TOSC = 1/FOSC

When TMR2 is equal to PR2, the following three events occur on the next increment cycle:

- TMR2 is cleared
- The PWMx pin is set (Exception: If the PWM duty cycle = 0%, the pin will not be set.)
- The PWM pulse width is latched from PWMxDC.

Note: If the pulse-width value is greater than the period, the assigned PWM pin(s) will remain unchanged.

19.1.2 PWM DUTY CYCLE

The PWM duty cycle is specified by writing a 10-bit value to the PWMxDC register. The PWMxDCH contains the eight MSbs and bits <7:6> of the PWMxDCL register contain the two LSbs.

The PWMDC register is double-buffered and can be updated at any time. This double buffering is essential for glitch-free PWM operation. New values take effect when TMR2 = PR2. Note that PWMDC is left-justified.

The 8-bit timer TMR2 register is concatenated with either the 2-bit internal system clock (FOSC), or two bits of the prescaler, to create the 10-bit time base. The system clock is used if the Timer2 prescaler is set to 1:1.

Equation 19-2 is used to calculate the PWM pulse width.

Equation 19-3 is used to calculate the PWM duty cycle ratio.

EQUATION 19-2: PULSE WIDTH

$$Pulse\ Width = (PWMxDC) \bullet T_{OSC} \bullet (TMR2\ Prescale\ Value)$$

EQUATION 19-3: DUTY CYCLE RATIO

$$Duty\ Cycle\ Ratio = \frac{(PWMxDC)}{4(PR2 + 1)}$$

TABLE 19-3: SUMMARY OF REGISTERS ASSOCIATED WITH PWMx

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
TRISA	—	—	TRISA5	TRISA4	—(2)	TRISA2	TRISA1	TRISA0	143
ANSELA	—	—	ANSA5	ANSA4	—	ANSA2	ANSA1	ANSA0	144
TRISB(1)	TRISB7	TRISB6	TRISB5	TRISB4	—	—	—	—	149
ANSELB(1)	ANSB7	ANSB6	ANSB5	ANSB4	—	—	—	—	150
TRISC	TRISC7(1)	TRISC6(1)	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	155
ANSELC	ANSC7(1)	ANSC6(1)	ANSC5	ANSC4	ANSC3	ANSC2	ANSC1	ANSC0	157
PWM5CON	PWM5EN	—	PWM5OUT	PWM5POL	—	—	—	—	196
PWM5DCH	PWM5DC<9:2>								196
PWM5DCL	PWM5DC<1:0>		—	—	—	—	—	—	196
PWM6CON	PWM6EN	—	PWM6OUT	PWM6POL	—	—	—	—	196
PWM6DCH	PWM6DC<9:2>								196
PWM6DCL	PWM6DC<1:0>		—	—	—	—	—	—	196
PWMTMRS	—	—	—	—	P6TSEL<1:0>		P5TSEL<1:0>		197
INTCON	GIE	PEIE	—	—	—	—	—	INTEDG	100
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	BCL1IF	TMR2IF	TMR1IF	107
PIR2	TMR6IF	C2IF	C1IF	NVMIF	SSP2IF	BCL2IF	TMR4IF	NCO1IF	108
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	BCL1IE	TMR2IE	TMR1IE	102
PIE2	TMR6IE	C2IE	C1IE	NVMIE	SSP2IE	BCL2IE	TMR4IE	NCO1IE	103
T2CON	—	T2OUTPS<3:0>				TMR2ON	T2CKPS<1:0>		298
T4CON	—	T4OUTPS<3:0>				TMR4ON	T4CKPS<1:0>		292
T6CON	—	T6OUTPS<3:0>				TMR6ON	T6CKPS<1:0>		292
TMR2	TMR2<7:0>								299
TMR4	TMR4<7:0>								299
TMR6	TMR6<7:0>								299
PR2	PR2<7:0>								299
PR4	PR4<7:0>								299
PR6	PR6<7:0>								299
CWGxDAT	—	—	—	—	DAT<3:0>				215
CLCxSELy	—	—	LCxDyS<5:0>						229
MDSRC	—	—	—	—	MDMS<3:0>				272
MDCARH	—	MDCHPOL	MDCHSYNC	—	MDCH<3:0>				273
MDCARL	—	MDCLPOL	MDCLSYNC	—	MDCL<3:0>				274

Legend: – = Unimplemented locations, read as '0'. Shaded cells are not used by the PWM module.
Note 1: PIC16(L)F18346 only.
2: Unimplemented, read as '1'.

REGISTER 20-9: CWGxDBF: CWGx FALLING DEAD-BAND COUNT REGISTER

U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	DBF<5:0>					
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	q = Value depends on condition

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **DBF<5:0>:** CWG Falling Edge Triggered Dead-Band Count bits
`11 1111` = 63-64 CWG clock periods
`11 1110` = 62-63 CWG clock periods
.
.
.
`00 0010` = 2-3 CWG clock periods
`00 0001` = 1-2 CWG clock periods
`00 0000` = 0 CWG clock periods. Dead-band generation is bypassed.

25.1 DSM Operation

The DSM module can be enabled by setting the MDEN bit in the MDCON register. Clearing the MDEN bit in the MDCON register, disables the DSM module by automatically switching the carrier high and carrier low signals to the VSS signal source. The modulator signal source is also switched to the MDBIT in the MDCON register. This not only assures that the DSM module is inactive, but that it is also consuming the least amount of current.

The values used to select the carrier high, carrier low, and modulator sources held by the Modulation Source, Modulation High Carrier, and Modulation Low Carrier control registers are not affected when the MDEN bit is cleared and the DSM module is disabled. The values inside these registers remain unchanged while the DSM is inactive. The sources for the carrier high, carrier low and modulator signals will once again be selected when the MDEN bit is set and the DSM module is again enabled and active.

The modulated output signal can be disabled without shutting down the DSM module. The DSM module will remain active and continue to mix signals, but the output value will not be sent to the DSM pin. During the time that the output is disabled, the DSM pin will remain low. The modulated output can be disabled by clearing the MDEN bit in the MDCON register.

25.2 Modulator Signal Sources

The modulator signal can be supplied from the following sources:

- CCP1 Output
- CCP2 Output
- PWM5 Output
- PWM6 Output
- MSSP1 SDO1 (SPI mode only)
- MSSP2 SDO2 (SPI mode only)
- Comparator C1 Output
- Comparator C2 Output
- EUSART1 TX Output
- External Signal on MDMIN pin
- NCO1 Output
- CLC1 Output
- CLC2 Output
- CLC3 Output
- CLC4 Output
- MDBIT bit in the MDCON register

The modulator signal is selected by configuring the MDMS <3:0> bits in the MDSRC register.

25.3 Carrier Signal Sources

The carrier high signal and carrier low signal can be supplied from the following sources:

- CCP1 Output
- CCP2 Output
- PWM5 Output
- PWM6 Output
- NCO1 Output
- FOSC (System Clock)
- HFINTOSC
- CLC1 Output
- CLC2 Output
- CLC3 Output
- CLC4 Output
- CLKR
- External Signal on MDCIN1 pin
- External Signal on MDCIN2 pin
- Vss

The carrier high signal is selected by configuring the MDCH <3:0> bits in the MDCARH register. The carrier low signal is selected by configuring the MDCL <3:0> bits in the MDCARL register.

25.4 Carrier Synchronization

During the time when the DSM switches between carrier high and carrier low signal sources, the carrier data in the modulated output signal can become truncated. To prevent this, the carrier signal can be synchronized to the modulator signal. When the modulator signal transitions away from the synchronized carrier, the unsynchronized carrier source is immediately active, while the synchronized carrier remains active until its next falling edge. When the modulator signal transitions back to the synchronized carrier, the unsynchronized carrier is immediately disabled, and the modulator waits until the next falling edge of the synchronized carrier before the synchronized carrier becomes active.

Synchronization is enabled separately for the carrier high and carrier low signal sources. Synchronization for the carrier high signal is enabled by setting the MDCHSYNC bit in the MDCARH register. Synchronization for the carrier low signal is enabled by setting the MDCLSYNC bit in the MDCARL register.

Figure 25-1 through Figure 25-6 show timing diagrams of using various synchronization methods.

EQUATION 29-2: PULSE WIDTH

$$Pulse\ Width = (CCPRxH{:}CCPRxL\ register\ pair) \bullet T_{OSC} \bullet (TMR2\ Prescale\ Value)$$

EQUATION 29-3: DUTY CYCLE RATIO

$$Duty\ Cycle\ Ratio = \frac{(CCPRxH{:}CCPRxL\ register\ pair)}{4(PR2 + 1)}$$

The CCPRxH:CCPRxL register pair and a 2-bit internal latch are used to double buffer the PWM duty cycle. This double buffering provides glitchless PWM operation.

The 8-bit timer TMR2/4/6 register is concatenated with either the 2-bit internal system clock (FOSC), or two bits of the prescaler, to create the 10-bit time base. The system clock is used if the Timer2/4/6 prescaler is set to 1:1.

When the 10-bit time base matches the CCPRxH:CCPRxL register pair, then the CCPx pin is cleared (see Figure 29-4).

29.4.6 PWM RESOLUTION

PWM resolution, expressed in number of bits, defines the maximum number of discrete steps that can be present in a single PWM period. For example, a 10-bit resolution will result in 1024 discrete steps, whereas an 8-bit resolution will result in 256 discrete steps.

The maximum PWM resolution is ten bits when PRx is 255. The resolution is a function of the PRx register value as shown by Equation 29-4.

EQUATION 29-4: PWM RESOLUTION

$$Resolution = \frac{\log[4(PRx + 1)]}{\log(2)}\ bits$$

Note:	If the pulse-width value is greater than the period the assigned PWM pin(s) will remain unchanged.

TABLE 29-1: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS (FOSC = 20 MHz)

PWM Frequency	1.22 kHz	4.88 kHz	19.53 kHz	78.12 kHz	156.3 kHz	208.3 kHz
Timer Prescale	16	4	1	1	1	1
PRx Value	0xFF	0xFF	0xFF	0x3F	0x1F	0x17
Maximum Resolution (bits)	10	10	10	8	7	6.6

TABLE 29-2: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS (FOSC = 8 MHz)

PWM Frequency	1.22 kHz	4.90 kHz	19.61 kHz	76.92 kHz	153.85 kHz	200.0 kHz
Timer Prescale	16	4	1	1	1	1
PRx Value	0x65	0x65	0x65	0x19	0x0C	0x09
Maximum Resolution (bits)	8	8	8	6	5	5

29.4.7 OPERATION IN SLEEP MODE

In Sleep mode, the TMR2/4/6 register will not increment and the state of the module will not change. If the CCPx pin is driving a value, it will continue to drive that value. When the device wakes up, TMR2/4/6 will continue from its previous state.

29.4.8 CHANGES IN SYSTEM CLOCK FREQUENCY

The PWM frequency is derived from the system clock frequency. Any changes in the system clock frequency will result in changes to the PWM frequency. See **Section 7.0 "Oscillator Module"** for additional details.

29.4.9 EFFECTS OF RESET

Any Reset will force all ports to Input mode and the CCP registers to their Reset states.

30.6 I²C Master Mode

Master mode is enabled by setting and clearing the appropriate SSPM<3:0> bits in the SSPxCON1 register and by setting the SSPEN bit. In Master mode, the SDA and SCK pins must be configured as inputs. The MSSP peripheral hardware will override the output driver TRIS controls when necessary to drive the pins low.

Master mode of operation is supported by interrupt generation on the detection of the Start and Stop conditions. The Stop (P) and Start (S) bits are cleared from a Reset or when the MSSPx module is disabled. Control of the I²C bus may be taken when the P bit is set, or the bus is Idle.

In Firmware Controlled Master mode, user code conducts all I²C bus operations based on Start and Stop bit condition detection. Start and Stop condition detection is the only active circuitry in this mode. All other communication is done by the user software directly manipulating the SDA and SCL lines.

The following events will cause the SSP Interrupt Flag bit, SSPxIF, to be set (SSP interrupt, if enabled):

- Start condition generation
- Stop condition generation
- Data transfer byte transmitted/received
- Acknowledge transmitted/received
- Repeated Start generated

Note 1:	The MSSPx module, when configured in I²C Master mode, does not allow queuing of events. For instance, the user is not allowed to initiate a Start condition and immediately write the SSPxBUF register to initiate transmission before the Start condition is complete. In this case, the SSPxBUF will not be written to and the WCOL bit will be set, indicating that a write to the SSPxBUF did not occur
2:	When in Master mode, Start/Stop detection is masked and an interrupt is generated when the SEN/PEN bit is cleared and the generation is complete.

30.6.1 I²C MASTER MODE OPERATION

The master device generates all of the serial clock pulses and the Start and Stop conditions. A transfer is ended with a Stop condition or with a Repeated Start condition. Since the Repeated Start condition is also the beginning of the next serial transfer, the I²C bus will not be released.

In Master Transmitter mode, serial data is output through SDA, while SCL outputs the serial clock. The first byte transmitted contains the slave address of the receiving device (7 bits) and the Read/$\overline{\text{Write}}$ (R/$\overline{\text{W}}$) bit. In this case, the R/$\overline{\text{W}}$ bit will be logic '0'. Serial data is transmitted eight bits at a time. After each byte is transmitted, an Acknowledge bit is received. Start and Stop conditions are output to indicate the beginning and the end of a serial transfer.

In Master Receive mode, the first byte transmitted contains the slave address of the transmitting device (7 bits) and the R/$\overline{\text{W}}$ bit. In this case, the R/$\overline{\text{W}}$ bit will be logic '1'. Thus, the first byte transmitted is a 7-bit slave address followed by a '1' to indicate the receive bit. Serial data is received via SDA, while SCL outputs the serial clock. Serial data is received eight bits at a time. After each byte is received, an Acknowledge bit is transmitted. Start and Stop conditions indicate the beginning and end of transmission.

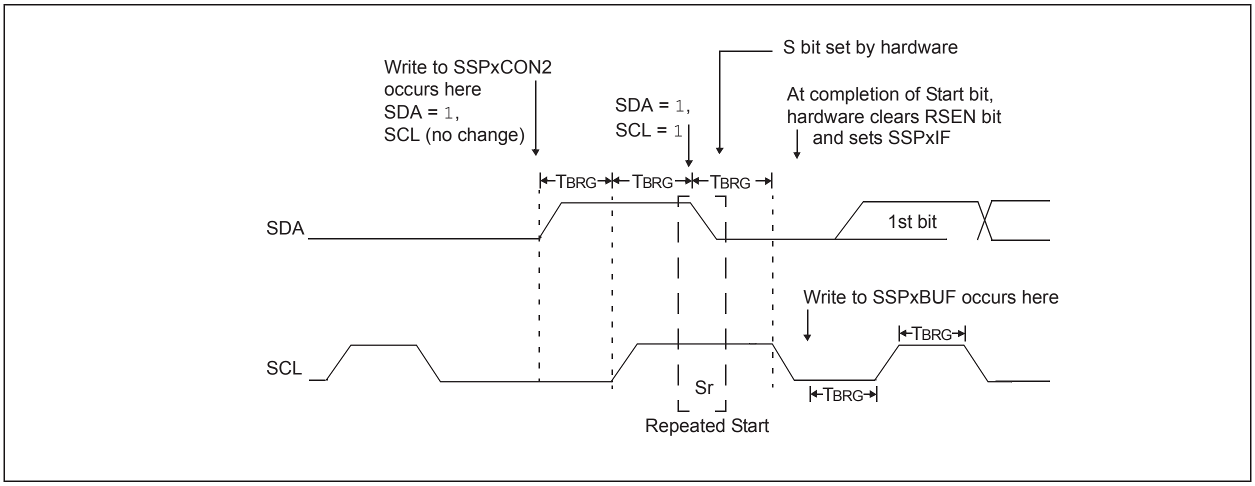
A Baud Rate Generator is used to set the clock frequency output on SCL. See **Section 30.7 "Baud Rate Generator"** for more detail.

30.6.5 I²C MASTER MODE REPEATED START CONDITION TIMING

A Repeated Start condition (Figure 30-27) occurs when the RSEN bit of the SSPxCON2 register is programmed high and the master state machine is no longer active. When the RSEN bit is set, the SCL pin is asserted low. When the SCL pin is sampled low, the Baud Rate Generator is loaded and begins counting. The SDA pin is released (brought high) for one Baud Rate Generator count (TBRG). When the Baud Rate Generator times out, if SDA is sampled high, the SCL pin will be deasserted (brought high). When SCL is sampled high, the Baud Rate Generator is reloaded and begins counting. SDA and SCL must be sampled high for one TBRG. This action is then followed by assertion of the SDA pin (SDA = 0) for one TBRG while SCL is high. SCL is asserted low. Following this, the RSEN bit of the SSPxCON2 register will be automatically cleared and the Baud Rate Generator will not be reloaded, leaving the SDA pin held low. As soon as a Start condition is detected on the SDA and SCL pins, the S bit of the SSPxSTAT register will be set. The SSPxIF bit will not be set until the Baud Rate Generator has timed out.

> **Note 1:** If RSEN is programmed while any other event is in progress, it will not take effect.
>
> **2:** A bus collision during the Repeated Start condition occurs if:
>
> - SDA is sampled low when SCL goes from low-to-high.
> - SCL goes low before SDA is asserted low. This may indicate that another master is attempting to transmit a data '1'.

FIGURE 30-27: REPEATED START CONDITION WAVEFORM



30.6.7 I^2C MASTER MODE RECEPTION

Master mode reception (Figure 30-29) is enabled by programming the Receive Enable bit, RCEN bit of the SSPxCON2 register.

Note:	The MSSPx module must be in an Idle state before the RCEN bit is set or the RCEN bit will be disregarded.

The Baud Rate Generator begins counting and on each rollover, the state of the SCL pin changes (high-to-low/low-to-high) and data is shifted into the SSPxSR. After the falling edge of the eighth clock, the receive enable flag is automatically cleared, the contents of the SSPxSR are loaded into the SSPxBUF, the BF flag bit is set, the SSPxIF flag bit is set and the Baud Rate Generator is suspended from counting, holding SCL low. The MSSPx is now in Idle state awaiting the next command. When the buffer is read by the CPU, the BF flag bit is automatically cleared. The user can then send an Acknowledge bit at the end of reception by setting the Acknowledge Sequence Enable, ACKEN bit of the SSPxCON2 register.

30.6.7.1 BF Status Flag

In receive operation, the BF bit is set when an address or data byte is loaded into SSPxBUF from SSPxSR. It is cleared when the SSPxBUF register is read.

30.6.7.2 SSPOV Status Flag

In receive operation, the SSPOV bit is set when eight bits are received into the SSPxSR and the BF flag bit is already set from a previous reception.

30.6.7.3 WCOL Status Flag

If the user writes the SSPxBUF when a receive is already in progress (i.e., SSPxSR is still shifting in a data byte), the WCOL bit is set and the contents of the buffer are unchanged (the write does not occur).

30.6.7.4 Typical Receive Sequence:

1. The user generates a Start condition by setting the SEN bit of the SSPxCON2 register.
2. SSPxIF is set by hardware on completion of the Start.
3. SSPxIF is cleared by software.
4. User writes SSPxBUF with the slave address to transmit and the R/$\overline{W}$ bit set.
5. Address is shifted out the SDA pin until all eight bits are transmitted. Transmission begins as soon as SSPxBUF is written to.
6. The MSSPx module shifts in the $\overline{ACK}$ bit from the slave device and writes its value into the ACKSTAT bit of the SSPxCON2 register.
7. The MSSPx module generates an interrupt at the end of the ninth clock cycle by setting the SSPxIF bit.
8. User sets the RCEN bit of the SSPxCON2 register and the master clocks in a byte from the slave.
9. After the eighth falling edge of SCL, SSPxIF and BF are set.
10. Master clears SSPxIF and reads the received byte from SSPxBUF, clears BF.
11. Master sets $\overline{ACK}$ value sent to slave in ACKDT bit of the SSPxCON2 register and initiates the $\overline{ACK}$ by setting the ACKEN bit.
12. Master's $\overline{ACK}$ is clocked out to the slave and SSPxIF is set.
13. User clears SSPIF.
14. Steps 8-13 are repeated for each received byte from the slave.
15. Master sends a not $\overline{ACK}$ or Stop to end communication.

TABLE 35-3: POWER-DOWN CURRENTS (IPD)(1,2,3)

PIC16LF18326/18346			Standard Operating Conditions (unless otherwise stated)						
PIC16F18326/18346			Standard Operating Conditions (unless otherwise stated) VREGPM = 1						
Param. No.	Symbol	Device Characteristics	Min.	Typ.†	Max. +85°C	Max. +125°C	Units	Conditions	
								VDD	Note
D200	IPD	IPD Base	—	0.05	2	9	μA	3.0V	
D200	IPD	IPD Base	—	0.8	4	12	μA	3.0V	
			—	13	22	27	μA	3.0V	VREGPM = 0
D201	IPD_WDT	Low-Frequency Internal Oscillator/WDT	—	0.8	5	13	μA	3.0V	
D201	IPD_WDT	Low-Frequency Internal Oscillator/WDT	—	0.9	5	13	μA	3.0V	
D202	IPD_SOSC	Secondary Oscillator (SOSC)	—	0.6	5	13	μA	3.0V	
D202	IPD_SOSC	Secondary Oscillator (SOSC)	—	0.8	9	15	μA	3.0V	
D203	IPD_FVR	FVR	—	40	47	47	μA	3.0V	
D203	IPD_FVR	FVR	—	33	44	44	μA	3.0V	
D204	IPD_BOR	Brown-out Reset (BOR)	—	12	17	19	μA	3.0V	
D204	IPD_BOR	Brown-out Reset (BOR)	—	12	18	20	μA	3.0V	
D205	IPD_LPBOR	Low Power Brown-out Reset (LPBOR)	—	3	5	13	μA	3.0V	
D205	IPD_LPBOR	Low Power Brown-out Reset (LPBOR)	—	4	5	13	μA	3.0V	
D207	IPD_ADCA	ADC - Active	—	0.9	5	13	μA	3.0V	ADC is converting(4)
D207	IPD_ADCA	ADC - Active	—	0.9	5	13	μA	3.0V	ADC is converting(4)
D208	IPD_CMP	Comparator	—	32	43	45	μA	3.0V	
D208	IPD_CMP	Comparator	—	31	42	44	μA	3.0V	

* These parameters are characterized but not tested.

† Data in "Typ." column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The peripheral current is the sum of the base IPD and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base IDD or IPD current from this limit. Max values should be used when calculating total current consumption.

2: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VSS.

3: All peripheral currents listed are on a per-peripheral basis if more than one instance of a peripheral is available.

4: ADC clock source is ADCRC.

TABLE 35-7: EXTERNAL CLOCK/OSCILLATOR TIMING REQUIREMENTS(1)

Standard Operating Conditions (unless otherwise stated)							
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Typ.†**	**Max.**	**Units**	**Conditions**
ECL Oscillator							
OS1	FECL	Clock Frequency	—	—	500	kHz	
OS2	TECL_DC	Clock Duty Cycle	40	—	60	%	
ECM Oscillator							
OS3	FECM	Clock Frequency	—	—	4	MHz	**Note 4**
OS4	TECM_DC	Clock Duty Cycle	40	—	60	%	
ECH Oscillator							
OS5	FECH	Clock Frequency	—	—	32	MHz	
OS6	TECH_DC	Clock Duty Cycle	40	—	60	%	
LP Oscillator							
OS7	FLP	Clock Frequency	—	—	100	kHz	**Note 4**
XT Oscillator							
OS8	FXT	Clock Frequency	—	—	4	MHz	**Note 4**
HS Oscillator							
OS9	FHS	Clock Frequency	—	—	20	MHz	**Note 4**
System Clock							
OS20	FOSC	System Clock Frequency	—	—	32	MHz	**Note 2, Note 3**
OS21	FCY	Instruction Frequency	—	FOSC/4	—	MHz	
OS22	TCY	Instruction Period	125	1/FCY	—	ns	

* These parameters are characterized but not tested.

† Data in "Typ." column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min" values with an external clock applied to OSC1 pin. When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

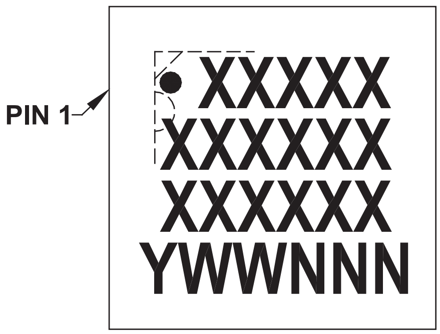
2: The system clock frequency (FOSC) is selected by the "main clock switch controls" as described in **Section 7.3 "Clock Switching"**.

3: The system clock frequency (FOSC) must meet the voltage requirements defined in the **Section 35.2 "Standard Operating Conditions"**. LP, XT and HS oscillator modes require an appropriate crystal or resonator to be connected to the device.

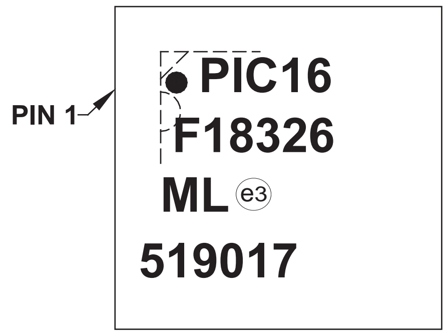
4: For clocking the device with an external square wave, one of the EC mode selections must be used.

Package Marking Information (Continued)

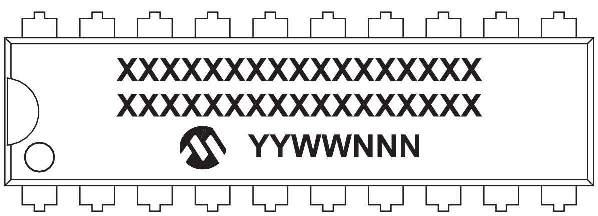
16-Lead UQFN (4x4x0.5mm)



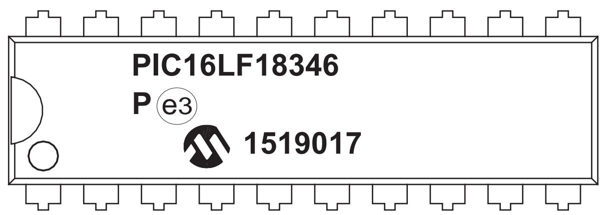
Example



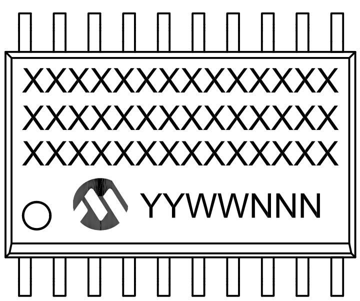
20-Lead PDIP (300 mil)



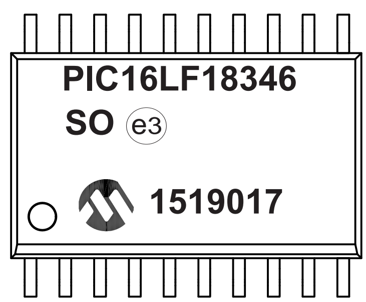
Example



20-Lead SOIC (7.50 mm)



Example

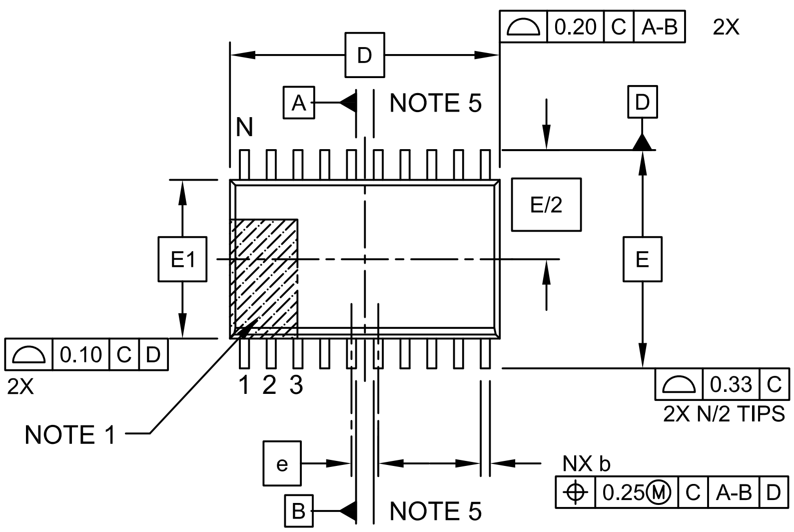


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	e3	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

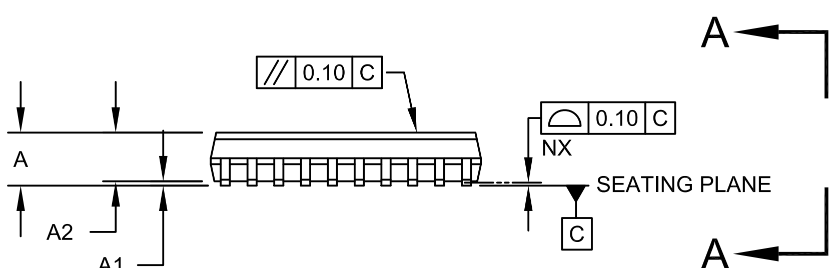
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

20-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

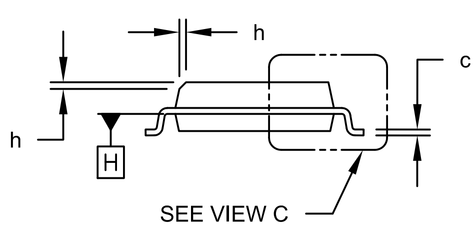
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

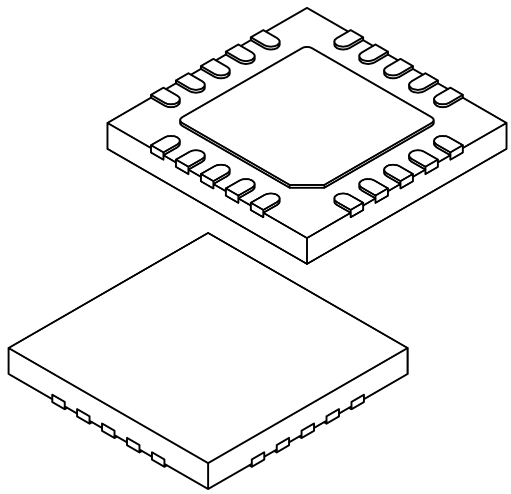


VIEW A-A

Microchip Technology Drawing C04-094C Sheet 1 of 2

20-Lead Ultra Thin Plastic Quad Flat, No Lead Package (GZ) - 4x4x0.5 mm Body [UQFN]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		20	
Pitch	e		0.50 BSC	
Overall Height	A	0.45	0.50	0.55
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.127 REF	
Overall Width	E		4.00 BSC	
Exposed Pad Width	E2	2.60	2.70	2.80
Overall Length	D		4.00 BSC	
Exposed Pad Length	D2	2.60	2.70	2.80
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.30	0.40	0.50
Terminal-to-Exposed-Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-255A Sheet 2 of 2

