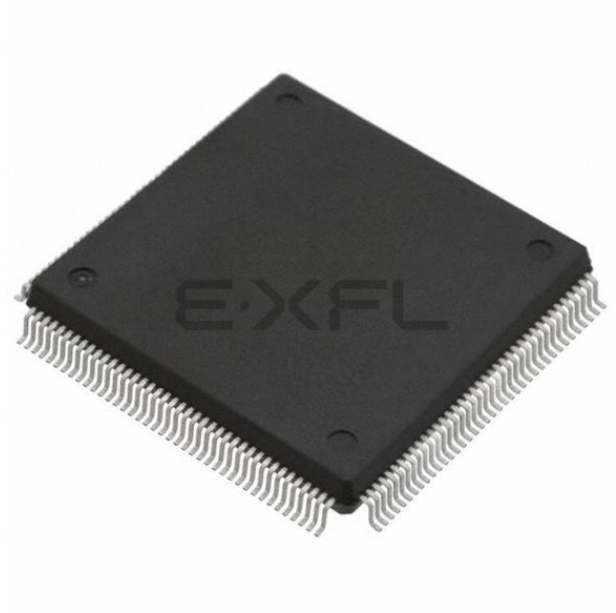

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Details	
Product Status	Obsolete
Core Processor	Coldfire V2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	16MHz
Co-Processors/DSP	-
RAM Controllers	DRAM
Graphics Acceleration	-
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	-
Package / Case	160-BQFP
Supplier Device Package	160-QFP (28x28)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcf5206cab16a

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2.7 CLOCK AND RESET SIGNALS

2.7.1 Clock Input (CLK)

CLK is the MCF5206 synchronous clock, and clocks or sequences the MCF5206 internal logic and external signals.

2.7.2 Reset ($\overline{\text{RSTI}}$)

Asserting the active-low $\overline{\text{RSTI}}$ input causes the MCF5206 processor to enter reset exception processing. When $\overline{\text{RSTI}}$ is recognized, the address bus, data bus, TT, SIZ, R/$\overline{\text{W}}$, ATM and $\overline{\text{TS}}$ is three-stated; $\overline{\text{BR}}$ and $\overline{\text{BD}}$ is negated.

If $\overline{\text{RSTI}}$ is asserted with $\overline{\text{HIZ}}$ asserted, the MCF5206 enters master reset mode. In this reset mode, the entire MCF5206 (including the DRAM controller refresh circuitry) is reset. You must use master reset for all power-on resets.

If $\overline{\text{RSTI}}$ is asserted with $\overline{\text{HIZ}}$ negated, the MCF5206 enters normal reset mode. In this reset mode, the DRAM controller refresh circuitry is not reset and continues to generate refresh cycles at the programmed rate and with the programmed waveform timing.

2.7.3 Reset Out ($\overline{\text{RTS[2]}}$/$\overline{\text{RSTO}}$)

$\overline{\text{RTS[2]}}$ is multiplexed with the $\overline{\text{RSTO}}$ signal. Programming the Pin Assignment Register (PAR) in the SIM determines the function of this pin. During reset, this pin is configured to be $\overline{\text{RSTO}}$.

$\overline{\text{RSTO}}$ is an output that drives peripherals to reset. There are no more than two clocks from the assertion of $\overline{\text{RSTI}}$ to the assertion of $\overline{\text{RSTO}}$, and $\overline{\text{RSTO}}$ remains asserted for at least 31 clocks after the negation of $\overline{\text{RSTI}}$. $\overline{\text{RSTO}}$ is also asserted for at least 31 clocks on a software watchdog time-out that is programmed to generate a reset.

2.8 DRAM CONTROLLER SIGNALS

The following DRAM signals provide a glueless interface to external DRAM:

2.8.1 Row Address Strobes ($\overline{\text{RAS[1:0]}}$)

These active-low output signals provide control for the row address strobe ($\overline{\text{RAS}}$) input pins on industry-standard DRAMs. There is one $\overline{\text{RAS}}$ output for each DRAM bank: $\overline{\text{RAS[0]}}$ controls DRAM bank 0 and $\overline{\text{RAS[1]}}$ controls DRAM bank 1. You can customize $\overline{\text{RAS}}$ timing to match the specifications of the DRAM being used by programming the DRAMC Timing Register (see **Section 10.4.2.2 DRAM Controller Timing register (DCTR).**).

2.8.2 Column Address Strobes ($\overline{\text{CAS[3:0]}}$)

These active-low output signals provide control for the column address strobe ($\overline{\text{CAS}}$) input pins on industry-standard DRAMs. The $\overline{\text{CAS}}$ signals enable data byte lanes: $\overline{\text{CAS[0]}}$ controls access to D[31:24], $\overline{\text{CAS[1]}}$ to D[23:16], $\overline{\text{CAS[2]}}$ to D[15:8], and $\overline{\text{CAS[3]}}$ to D[7:0]. You should use $\overline{\text{CAS[3:0]}}$ for a 32-bit wide DRAM bank, $\overline{\text{CAS[1:0]}}$ for a 16-bit wide DRAM

The DSCLK input signal is used as the development serial clock for the serial interface to the debug module.The maximum frequency for the DSCLK signal is 1/2 the CLK frequency. See the **Debug Support** section for additional information on this signal.

2.13.4 Break Point (TMS/$\overline{\text{BKPT}}$)

The MTMOD signal determines the function of this dual-purpose pin. If MTMOD = 0, then the TMS function is selected. If MTMOD =1, the $\overline{\text{BKPT}}$ function is selected. MTMOD should not change while $\overline{\text{RSTI}}$ = 1.

The assertion of the active-low $\overline{\text{BKPT}}$ input signal causes a hardware breakpoint to occur in the processor when in the debug mode. See the **Debug Support** section for additional information on this signal.

2.13.5 Development Serial Input (TDI/DSI)

The MTMOD signal determines the function of this dual-purpose pin. If MTMOD = 0, then TDI is selected. If MTMOD = 1, then DSI is selected. MTMOD should not change while $\overline{\text{RSTI}}$ = 1.

The DSI input signal is the serial data input for the Debug module commands. See the **Debug Support** section for additional information on this signal.

2.13.6 Development Serial Output (TDO/DSO)

The MTMOD signal determines the function of this dual-purpose pin. When MTMOD = 0, TDO is selected. When MTMOD = 1, then DSO is selected. MTMOD should not change while $\overline{\text{RSTI}}$ = 1.

The DSO output signal is the serial data output for the debug module responses. See the **Debug Support** section for additional information on this signal.

2.14 JTAG SIGNALS

2.14.1 Test Clock (TCK)

TCK is the dedicated JTAG test logic clock that is independent of the MCF5206 processor clock. The internal JTAG controller logic is designed such that holding TCK high or low for an indefinite period of time does not cause the JTAG test logic to lose state information. TCK should be grounded if it is not used.

2.14.2 Test Reset ($\overline{\text{TRST}}$/DSCLK)

The MTMOD signal determines the function of this dual-purpose pin. If MTMOD= 0, the TRST function is selected. If MTMOD=1, the DSCLK function is selected. MTMOD should not be changed while $\overline{\text{RSTI}}$ = 1.

The assertion of the active-low $\overline{\text{TRST}}$ input pin asynchronously resets the JTAG TAP controller to the test logic reset state, causing the JTAG instruction register to choose the

"bypass" command. When this occurs, all the JTAG logic is benign and does not interfere with the normal functionality of the MCF5206 processor. Although this signal is asynchronous, we recommend that $\overline{\text{TRST}}$ make only a 0 to 1 (asserted to negated) transition while TMS is held at a logic 1 value. $\overline{\text{TRST}}$ has an internal pullup so that if it is not driven low, its value defaults to a logic level of 1. However, if JTAG is not being used, $\overline{\text{TRST}}$ can either be tied to ground, placing the JTAG controller in the test logic reset state immediately, or tied to VDD, causing the JTAG controller (if TMS is a logic 1) to eventually end up in the test logic reset state after five clocks of TCK.

2.14.3 Test Mode Select (TMS/$\overline{\text{BKPT}}$)

The MTMOD signal determines the function of this dual-purpose pin. If MTMOD = 0, then the TMS function is selected. If MTMOD =1, the BKPT function is selected. MTMOD should not change while $\overline{\text{RSTI}}$ = 1.

The TMS input signal provides the JTAG controller with information to determine which test operation should be performed. The value of TMS and the current state of the internal 16-state JTAG controller state machine at the rising edge of TCK determine whether the JTAG controller holds its current state or advances to the next state. This directly controls whether JTAG data or instruction operations occur. TMS has an internal pullup so that if it is not driven low, its value defaults to a logic level of 1. However, if TMS is not being used, it should be tied to VDD.

2.14.4 Test Data Input (TDI/DSI)

The MTMOD signal determines the function of this dual-purpose pin. If MTMOD = 0, then TDI is selected. If MTMOD = 1, then DSI is selected. MTMOD should not change while $\overline{\text{RSTI}}$ = 1.

The TDI input signal provides the serial data port for loading the various JTAG shift registers (the boundary scan register, the bypass register, and the instruction register). Shifting in of data depends on the state of the JTAG controller state machine and the instruction currently in the instruction register. This data shift occurs on the rising edge of TCK. TDI also has an internal pullup so that if it is not driven low, its value defaults to a logic level of 1. However, if TDI is not being used, it should be tied to VDD.

2.14.5 Test Data Output (TDO/DSO)

The MTMOD signal determines the function of this dual-purpose pin. When MTMOD = 0, TDO is selected. When MTMOD = 1, then DSO is selected. MTMOD should not change while $\overline{\text{RSTI}}$ = 1.

The TDO output signal provides the serial data port for outputting data from the JTAG logic. Shifting out of data depends on the state of the JTAG controller state machine and the instruction currently in the instruction register. This data shift occurs on the falling edge of TCK. When TDO is not outputting test data, it is placed in a high-impedence state. TDO can also be three-stated to allow bussed or parallel connections to other devices having JTAG.

Table 2-11. MCF5206 Signal Summary (Continued)

SIGNAL NAME	MNEMONIC	INPUT/OUTPUT	ACTIVE STATE	RESET STATE
Bus Driven	$\overline{BD}$	Out	Low	Negated
Clock Input	CLK	In	-	-
Reset	$\overline{RSTI}$	In	Low	-
Row Address Strobe	$\overline{RAS}$[1:0]	Out	Low	Master Reset - Negated Normal Reset - Unaffected
Column Address Strobe	$\overline{CAS}$[3:0]	Out	Low	Master Reset - Negated Normal Reset - Unaffected
DRAM Write	$\overline{DRAMW}$	Out	Low	Negated
Receive Data	RxD[1], RxD[2]	In	-	-
Transmit Data	TxD[1], TxD[2]	Out	-	Asserted
Request-To-Send	$\overline{RTS}$[1]	Out	Low	Negated
Request-To-Send	$\overline{RTS}$[2]/ $\overline{RSTO}$	Out/ Out	Low/ Low	Asserted
Clear-To-Send	$\overline{CTS}$[1], $\overline{CTS}$[2]	In	Low	-
Timer Input	TIN[1], TIN[2]	In	-	-
Timer Output	TOUT[1], TIN[2]	Out	-	Asserted
Serial Clock Line	SCL	In,Out	Low	Negated
Serial Data Line	SDA	In,Out	Low	Negated
General Purpose I/O/ Processor Status	PP[7:4]/ PST[3:0]	In.Out/ Out	-/ -	Three-stated
General Purpose I/O/ Debug Data	PP[3:0]/ DDATA[3:0]	In,Out/ Out	-/ -	Three-stated
Test Clock	TCK	In	-	-
Test Data Output/Development Serial Output	TDO/ DSO	Out/ Out	-/ -	Three-Stated/ Negated
Test Mode Select/ Break Point	TMS/ $\overline{BKPT}$	In/ In	-/ Low	-/ -
Test Data Input / Development Serial Input	TDI/ DSI	In/ In	-/ -	-/ -
Test Reset/Development Serial Clock	$\overline{TRST}$/ DSCLK	In/ In	Low/ -	-/ -
Motorola Test Mode	MTMOD	In	-	-
High Impedance	$\overline{HIZ}$	In	Low	-

address space.

2. Read the source data and write it to the SRAM. There are various instructions to support this function, including memory-to-memory move instructions, or the MOVEM opcode. The MOVEM instruction is optimized to generate line-sized burst fetches on 0-modulo-16 addresses, so this opcode generally provides maximum performance.
3. After the data has been loaded into the SRAM, it may be appropriate to load a revised value into the RAMBAR with a new set of “attributes.” These attributes consist of the write-protect and address space mask fields.

The ColdFire processor or an external emulator using the Debug module can perform these initialization functions.

5.3.4 Power Management

As noted previously, depending upon the configuration defined by the RAMBAR, instruction fetch accesses can be sent to the SRAM module and the I-Cache simultaneously. If the access is mapped to the SRAM module, it sources the read data, discarding the I-Cache access. If the SRAM is used only for data operands, setting the SC and UC mask bits in the RAMBAR to 1 lowers power dissipation. This disables the SRAM during all instruction fetches. Additionally, if the SRAM contains only instructions, setting the SD and UD mask bits in the RAMBAR to 1 masking operand accesses reduces power dissipation.

Consider the examples on Table 5-2 of typical RAMBAR settings:

Table 5-2. Examples of Typical RAMBAR Settings

DATA CONTAINED IN SRAM	RAMBAR[7:0]
Code only	$2B
Data only	$35
Both Code and Data	$21

Figure 6-5 shows a longword supervisor code read from a 32-bit port.

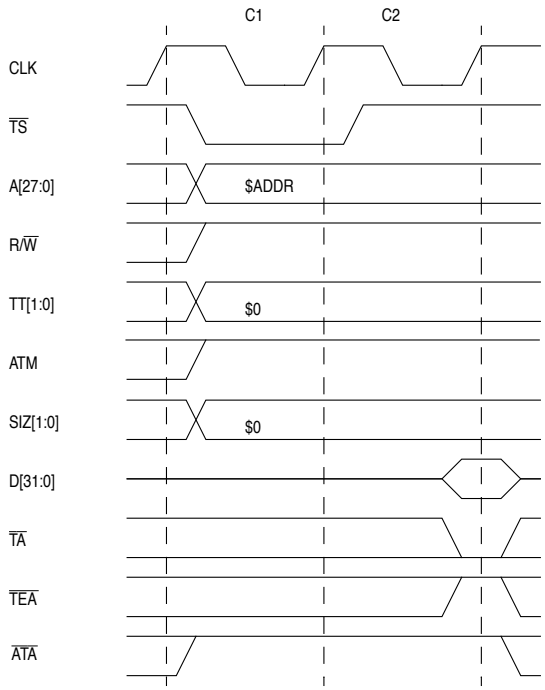

Figure 6-5. Longword-Read Transfer From a 32-Bit Port (No Wait States)

Clock 1 (C1)

The read cycle starts in C1. During C1, the MCF5206 places valid values on the address bus (A[27:0]) and transfer control signals. The transfer type (TT[1:0]) signals identify the specific access type. Access type and mode (ATM) identifies the transfer as reading code. The read/write (R/$\overline{W}$) signal is driven high for a read cycle, and the size signals (SIZ[1:0]) are driven low to indicate a longword transfer. The MCF5206 asserts transfer start ($\overline{TS}$) to indicate the beginning of a bus cycle.

Clock 2 (C2)

During C2, the MCF5206 negates transfer start ($\overline{TS}$), drives access type and mode (ATM) high to identify the transfer as supervisor. The selected device(s) places the addressed data onto D[31:0] and asserts the transfer acknowledge ($\overline{TA}$). At the end of C2, the MCF5206 samples the level of $\overline{TA}$ and if $\overline{TA}$ is asserted, latches the current value of D[31:0]. If $\overline{TA}$ is asserted, the transfer of the longword is complete and the transfer terminates. If $\overline{TA}$ is negated, the MCF5206 continues to sample $\overline{TA}$ and inserts wait states instead of terminating the transfer. The MCF5206 continues to sample $\overline{TA}$ on successive rising edges of CLK until it is asserted. If the bus monitor timer is enabled and $\overline{TA}$ is not

Clock 9 (C9)

This clock is identical to C3, except that the data value corresponds to the fourth longword of data for the line. This is the last CLK cycle of the line write transfer and the MCF5206 three-states D[31:0] at the start of the next CLK cycle.

6.5.10 Burst-Inhibited Read Transfers: Word, Longword, and Line with Asynchronous Acknowledge

If the burst-enable bit is cleared in the appropriate Chip Select Control Register (CSCR) or Default Memory Control Register (DMCR) and the operand size is larger than the port size of the memory being accessed, the MCF5206 performs word, longword, and line transfers in burst-inhibited mode. When burst-inhibit mode is selected, the size of the transfer (indicated by SIZ[1:0]) reflects the port size if the operand being read is larger than the port size, or the operand size if the port size is larger than the operand size. A transfer size of line (SIZ[1:0] = $3) is never indicated in burst-inhibited mode. If the operand size is line, the size pins (SIZ[1:0]) always indicates the port size.

The basic transfer of a burst-inhibited read using asynchronous termination is the same as “normal” read using asynchronous termination with the addition of more transfers, until the entire operand has been accessed. Figure 6-24 is a flowchart for burst-inhibited read transfers to 8-, 16-, or 32-bit ports with asynchronous termination. Bus operations are similar for each case and vary only with the size indicated, the portion of the data bus used for the transfer, and the specific number of cycles needed for each transfer. The flowchart is specifically for a burst-inhibited transfer of four transfers long.

MCF5206 has implicit ownership of the bus. When the external bus master negates $\overline{BG}$, the MCF5206 negates $\overline{BD}$ and three-state the address, data, $\overline{TS}$, R/$\overline{W}$, and SIZ signals after completing the current bus cycle. Figure 6-35 illustrates two-wire bus arbitration with the bus lock bit cleared.

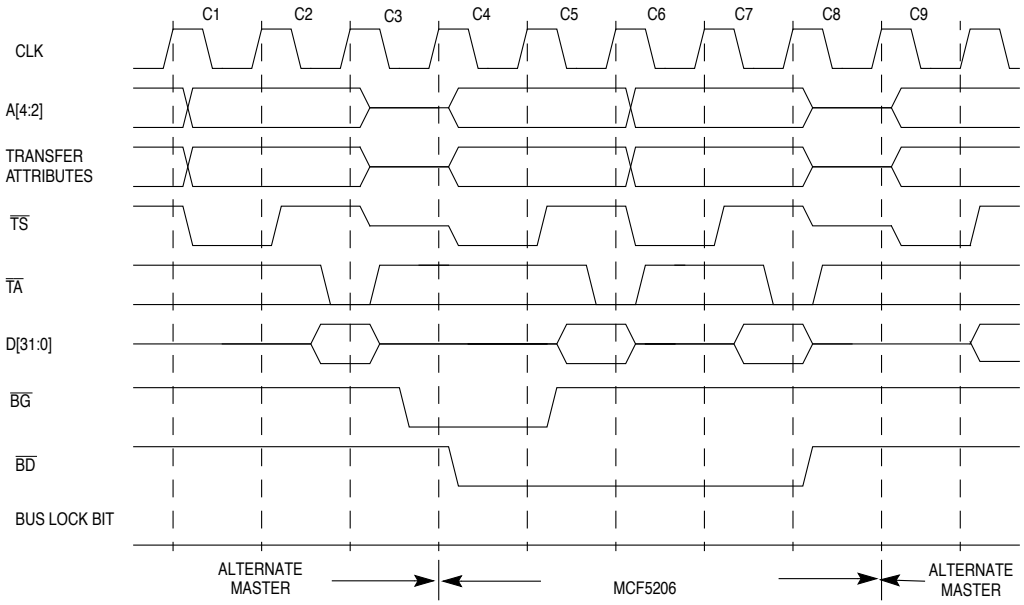

Figure 6-35. Two-Wire Bus Arbitration with Bus Lock Negated

In Figure 6-35 during clocks C1 and C2, the external master is the bus owner. During C3, the external master relinquishes control of the bus by asserting $\overline{BG}$ to the MCF5206. At this point, the bus lock bit is cleared, but because there is an internal access pending, the MCF5206 asserts $\overline{BD}$ during C4 and begins the access. Thus, the MCF5206 becomes the explicit master of the external bus. This access is a burst-inhibited access. During C5, the external master removes the grant from the MCF5206 by negating $\overline{BG}$. Because the MCF5206 is performing a burst-inhibited access, it continues to assert $\overline{BD}$ until the final transfer of the access has completed. The MCF5206 negates $\overline{BD}$ during C8, returning ownership of the external bus to the external master.

In the second case, the bus lock bit in the SIM Configuration Register (SIMR) is set to 1 and the MCF5206 has explicit ownership of the bus. In this case, when the external bus master negates $\overline{BG}$, the MCF5206 continues to assert $\overline{BD}$ and continues to drive address, attributes, and control signals. The MCF5206 retains mastership of the bus until the bus lock bit in the SIM Configuration Register (SIMR) is cleared. By setting the bus lock bit to 1, you can select the MCF5206 to be the highest priority master, even when mastership of the bus is controlled by an external master. In this fashion, the MCF5206 can be

Transfer Acknowledge Flowchart

Figure 6-44 illustrates $\overline{TA}$ assertion by the MCF5206 during external master write transfers.

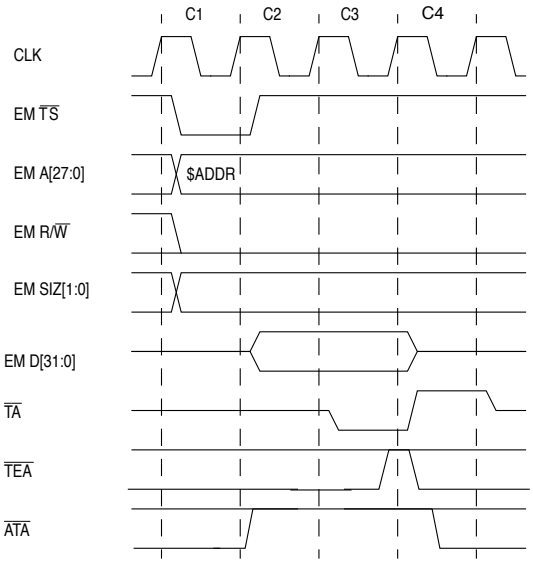

Figure 6-44. Alternate Master Write Transfer Using MCF5206 Transfer-Acknowledge Timing (No Wait States)

Clock 1 (C1)

The write cycle starts in C1. During C1, the external master drives valid values on the address bus (A[27:0]) and transfer control signals. The read/write (R/$\overline{W}$) signal is driven low for a write cycle, and the size signals (SIZ[1:0]) are driven to indicate the transfer size. The external master asserts transfer start ($\overline{TS}$) to indicate the beginning of a bus cycle.

Clock 2 (C2)

At the start of C2, the MCF5206 registers and decodes the external master address bus, read/write and size signals. If the external master automatic acknowledge (EMAA) bit in the Default Memory Control Register (DMCR) is set to 1, the MCF5206 selects the indicated number of wait states for loading into the internal wait state counter. During C2, the external master negates $\overline{TS}$, places the data on the data bus (D[31:0]), and samples the level of $\overline{TA}$. The selected device(s) decode the address and latch the data when it is ready.

Clock 3 (C3)

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SECTION 10
DRAM CONTROLLER

10.1 INTRODUCTION

The DRAM controller (DRAMC) provides a glueless interface between the ColdFire core and external DRAM. The DRAMC supports two banks of DRAM. Each DRAM bank can be from 128 KByte to 256 MByte, in widths of 8, 16, or 32 bits. Two row address strobe ($\overline{RAS}$[1:0]) signals are provided externally to access the two DRAM banks. Data byte lanes are enabled using the four column address strobe ($\overline{CAS}$[3:0]) signals. The DRAM write ($\overline{DRAMW}$) signal indicates if the DRAM transfer is a read or a write. The DRAMC handles address multiplexing internally, allowing for a glueless DRAM interface. The DRAMC has an internal refresh timer that generates $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles. You can program $\overline{RAS}$ and $\overline{CAS}$ waveform timing and refresh rates. External master use of the DRAMC for accessing the DRAM banks is also supported.

10.1.1 Features

The following list summarizes the key DRAMC features:

- Supports two banks of DRAM
- Supports Normal Mode, Fast Page Mode, and Burst Page Mode
- Supports EDO DRAMs
- Supports glueless row address/column address multiplexing
- Programmable $\overline{RAS}$ and $\overline{CAS}$ timings
- Programmable refresh timer for $\overline{CAS}$-before-$\overline{RAS}$ refresh
- Supports external master use of the DRAMC

10.2 DRAM CONTROLLER I/O

10.2.1 Control Signals

The DRAMC has seven control signal signals: $\overline{CAS}$[0], $\overline{CAS}$[1], $\overline{CAS}$[2], $\overline{CAS}$[3], $\overline{RAS}$[0], $\overline{RAS}$[1], and $\overline{DRAMW}$.

10.2.1.1 ROW ADDRESS STROBES ($\overline{RAS}$[0], $\overline{RAS}$[1]). These active-low output signals provide control for the row address strobe ($\overline{RAS}$) input pins on industry-standard DRAMs. There is one $\overline{RAS}$ output for each DRAM bank: $\overline{RAS}$[0] controls DRAM bank 0 and $\overline{RAS}$[1] controls DRAM bank 1. $\overline{RAS}$ timing can be customized to match the specifications of the DRAM being used by programming the DRAMC Timing Register (see **Section 10.4.2.2 DRAM Controller Timing Register (DCTR)**).

Clock H3

The internal transfer acknowledge asserts to indicate that the longword read transfer is completed and that data on D[31:0] is registered on the next rising edge of CLK.

Clock H4

The MCF5206 negates the internal transfer acknowledge, and $\overline{CAS}$[3:0], ending the longword read transfer. At this point the new page has been opened; therefore, the MCF5206 continues to assert $\overline{RAS}$. Once $\overline{CAS}$[3:0] are negated the DRAM disables its output drivers and the D[31:0] are three-stated. The negation of $\overline{CAS}$[3:0] begins the $\overline{CAS}$ precharge.

Clock H6

Clock H6 is the earliest the next transfer initiated by the ColdFire core can start. In this case, a page-hit longword read is shown. The page-hit longword read transfer starts in H6. During H6, the MCF5206 drives the column address on A[27:9], drives $\overline{DRAMW}$ high indicating a DRAM read transfer, drives SIZ[1:0] to $0 indicating a longword transfer, and asserts $\overline{TS}$.

Clock L6

The MCF5206 asserts $\overline{CAS}$[3:0] to indicate the column address is valid on A[27:9]. At this point, the DRAM turns on its output drivers and begin driving data on D[31:0].

Clock H7

Clock H7 is the same as Clock H3.

Clock H8

The MCF5206 negates the internal transfer acknowledge, and $\overline{CAS}$[3:0], ending the page-hit longword read transfer. Since the DRAM bank is in Fast Page Mode, the MCF5206 continues to assert $\overline{RAS}$. Once $\overline{CAS}$[3:0] are negated the DRAM disables it's output drivers and D[31:0] are three-stated. The negation of $\overline{CAS}$[3:0] begins the $\overline{CAS}$ precharge.

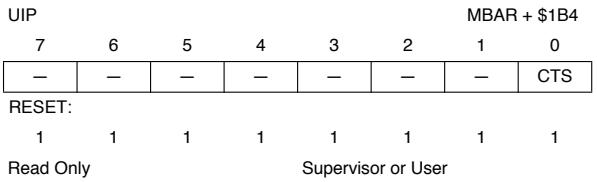
10.3.4.3 PAGE-HIT WRITE TRANSFER IN FAST PAGE MODE. A write transfer to an open page results in a page-hit write. The timing of page-hit write transfers differs from the timing of page-hit read transfers. On a page-hit write transfer, $\overline{CAS}$ is asserted one cycle later than in a page-hit read transfer. This is because the write data is not driven until the cycle after $\overline{TS}$ is asserted and data must be set up prior to $\overline{CAS}$ assertion. The start of a page-hit write transfer to a DRAM bank in fast page mode can be delayed by the DRAMC until the programmed $\overline{CAS}$ precharge time is reached.

The fastest possible nonburst page-hit write transfer in fast page mode requires 3 clocks. The fastest possible burst page-hit write transfer in fast page mode requires 3 clocks for the initial transfer and 2 clocks for all secondary writes. You can program the DCTR to generate slower fast page mode transfers.

IVR7–IVR0 — Interrupt Vector Bits

This 8-bit number indicates the offset from the base of the vector table where the address of the exception handler for the specified interrupt is located. The UIVR is reset to $0F, which indicates an uninitialized interrupt condition.

11.4.1.14.1 Input Port Register (UIP). The UIP register shows the current state of the $\overline{\text{CTS}}$ input.



$\overline{\text{CTS}}$ — Current State

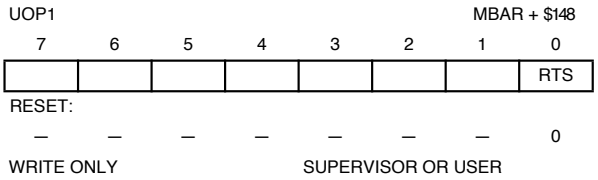
1 = The current state of the $\overline{\text{CTS}}$ input is logic 1
0 = The current state of the $\overline{\text{CTS}}$ input is logic 0

The information contained in this bit is latched and reflects the state of the input pin at the time that the UIP is read.

NOTE

This bit has the same function and value as the UIPCR bit 0.

11.4.1.14.2 Output Port Data Registers (UOP1, UOP0). The $\overline{\text{RTS}}$ output is set by a bit set command (writing to UOP1) and is cleared by a bit reset command (writing to UOP0).



$\overline{\text{RTS}}$ — Output Port Parallel Output

1 = A write cycle to the OPset address asserts the $\overline{\text{RTS}}$ signal.
0 = This bit is not affected by writing a zero to this address.

NOTE

The output port bits are inverted at the pins so the $\overline{\text{RTS}}$ set bit provides an asserted $\overline{\text{RTS}}$ pin.

Command Formats:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$1				$D				$0				$0			

Byte DUMP Command

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X	DATA [7:0]							

Byte DUMP Result

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$1				$D				$4				$0			

Word DUMP Command

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA [15:0]															

Word DUMP Result

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$1				$D				$8				$0			

Long DUMP Command

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA [31:16]															
DATA [15:0]															

Long DUMP Result

EDWU–Enable Data Breakpoint for the Upper Data Word

If set, this bit enables the data breakpoint trigger based on the KD[31:16] word.

EDLL–Enable Data Breakpoint for the Lower Lower Data Byte

If set, this bit enables the data breakpoint trigger based on the KD[7:0] byte.

EDLM–Enable Data Breakpoint for the Lower Middle Data Byte

If set, this bit enables the data breakpoint trigger based on the KD[15:8] byte.

EDUM–Enable Data Breakpoint for the Upper Middle Data Byte

If set, this bit enables the data breakpoint trigger based on the KD[23:16] byte.

EDUU–Enable Data Breakpoint for the Upper Upper Data Byte

If set, this bit enables the data breakpoint trigger based on the KD[31:24] byte.

DI–Data Breakpoint Invert

This bit provides a mechanism to invert the logical sense of all the data breakpoint comparators. This can develop a trigger based on the occurrence of a data value not equal to the one programmed into the DBR.

The assertion of any of the EA bits enables the address breakpoint. If all three bits are cleared, this breakpoint is disabled.

EAI–Enable Address Breakpoint Inverted

If set, this bit enables the address breakpoint based outside the range defined by ABLR and ABHR.

EAR–Enable Address Breakpoint Range

If set, this bit enables the address breakpoint based on the inclusive range defined by ABLR and ABHR.

EAL–Enable Address Breakpoint Low

If set, this bit enables the address breakpoint based on the address contained in the ABLR.

EPC–Enable PC Breakpoint

If set, this bit enables the PC breakpoint. Clearing this bit disables the PC breakpoint.

PCI–PC Breakpoint Invert

If set, this bit allows execution outside a given region as defined by PBR and PBMR to enable a trigger. If cleared, the PC breakpoint is defined within the region defined by PBR and PBMR.

14.3.1.6 CONFIGURATION/STATUS REGISTER (CSR). The Configuration/Status Register defines the operating configuration for the processor and memory subsystem. In

also configure the direction of bidirectional pins and establish high-impedance states on some pins. The EXTEST instruction becomes active on the falling edge of TCK in the update-IR state when the data held in the instruction-shift register is equivalent to octal 0.

15.3.1.2 IDCODE. The IDCODE instruction selects the 32-bit IDcode register for connection as a shift path between the TDI pin and the TDO pin. This instruction lets you interrogate the MCF5206 to determine its version number and other part identification data. The IDcode register has been implemented in accordance with IEEE 1149.1 so that the least significant bit of the shift register stage is set to logic 1 on the rising edge of TCK following entry into the capture-DR state. Therefore, the first bit to be shifted out after selecting the IDcode register is always a logic 1. The remaining 31-bits are also set to fixed values (see 15.3.2 IDcode Register) on the rising edge of TCK following entry into the capture-DR state.

The IDCODE instruction is the default value placed in the instruction register when a JTAG reset is accomplished by either asserting $\overline{\text{TRST}}$ or holding TMS high while clocking TCK through at least five rising edges and the falling edge after the fifth rising edge. A JTAG reset causes the TAP state machine to enter the test-logic-reset state (normal operation of the TAP state machine into the test-logic-reset state also results in placing the default value of octal 1 into the instruction register). The shift register portion of the instruction register is loaded with the default value of octal 1 when in the Capture-IR state and a rising edge of TCK occurs.

15.3.1.3 SAMPLE/PRELOAD INSTRUCTION. The SAMPLE/PRELOAD instruction provides two separate functions. First, it obtains a sample of the system data and control signals present at the MCF5206 input pins and just prior to the boundary scan cell at the output pins. This sampling occurs on the rising edge of TCK in the capture-DR state when an instruction encoding of octal 4 is resident in the instruction register. You can observe this sampled data by shifting it through the boundary-scan register to the output TDO by using the shift-DR state. Both the data capture and the shift operation are transparent to system operation. You are responsible for providing some form of external synchronization to achieve meaningful results because there is no internal synchronization between TCK and the system clock, CLK.

The second function of the SAMPLE/PRELOAD instruction is to initialize the boundary scan register update cells before selecting EXTEST or CLAMP. This is achieved by ignoring the data being shifted out of the TDO pin while shifting in initialization data. The update-DR state in conjunction with the falling edge of TCK can then transfer this data to the update cells. This data is applied to the external output pins when one of the instructions listed above is applied.

15.3.1.4 HIGHZ INSTRUCTION. The HIGHZ instruction anticipates the need to backdrive the output pins and protect the input pins from random toggling during circuit board testing. The HIGHZ instruction selects the bypass register, forcing all output and bidirectional pins to the high-impedance state.

15.5 RESTRICTIONS

The test logic is implemented using static logic design, and TCK can be stopped in either a high or low state without loss of data. The system logic, however, operates on a different system clock which is not synchronized to TCK internally. Any mixed operation requiring the use of 1149.1 test logic in conjunction with system functional logic that uses both clocks, must have coordination and synchronization of these clocks done externally to the MCF5206.

15.6 DISABLING THE IEEE 1149.1 STANDARD OPERATION

There are two methods by which the MCF5206 can be used without the IEEE 1149.1 test logic being active: (1) Nonuse of the JTAG test logic by either nontermination (disconnection) or intentional fixing of TAP logic values, and (2) Intentional disabling of the JTAG test logic by assertion of the $\overline{\text{JTAG}}$ signal (entering Debug mode).

There are several considerations that must be addressed if the IEEE 1149.1 logic is not going to be used once the MCF5206 is assembled onto a board. The prime consideration is to ensure that the IEEE 1149.1 test logic remains transparent and benign to the system logic during functional operation. This requires the minimum of either connecting the $\overline{\text{TRST}}$ pin to logic 0, or connecting the TCK clock pin to a clock source that supplies five rising edges and the falling edge after the fifth rising edge, to ensure that the part enters the test-logic-reset state. The recommended solution is to connect $\overline{\text{TRST}}$ to logic 0. Another consideration is that the TCK pin does not have an internal pullup as is required on the TMS, TDI, and $\overline{\text{TRST}}$ pins; therefore, it should not be left unterminated to preclude mid-level input values. Figure 15-3 shows pin values recommended for disabling JTAG with the MCF5206 in JTAG mode ($\overline{\text{JTAG}}$=0).

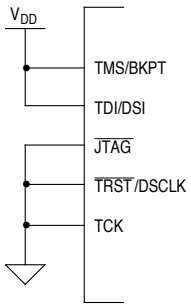


Figure 15-3. Disabling JTAG in JTAG Mode

A second method of using the MCF5206 without the IEEE 1149.1 logic being active is to select Debug mode by placing a logic 1 on the defined compliance enable pin, $\overline{\text{JTAG}}$. When $\overline{\text{JTAG}}$ is a logic 1, then the IEEE 1149.1 test controller is placed in the test-logic-reset state by the internal assertion of the $\overline{\text{TRST}}$ signal to the controller, and, the TAP pins function as debug mode pins. While in JTAG mode, input pins TDI/DSI, TMS/$\overline{\text{BKPT}}$, and

16.1.3 Thermal Resistance

CHARACTERISTIC	SYMBOL[b]	VALUE	RATING
Thermal resistance, junction to ambient Thermal resistance, junction to top reference	q_{ja} Y_{jt}	38 3	°C/W °C/W

[b] q_{ja} and Y_{jt} parameters are simulated in accordance with EIA/JESD Standard 51-2 for natural convection. Motorola recommends the use of q_{ja} and power dissipation specifications in the system design to prevent device junction temperatures from exceeding the rated specification. System designers should be aware that device junction temperatures can be significantly influenced by the board layout and surrounding devices. Conformance to the device junction temperature specification can be verified by physical measurement in the customer's system using the Y_{jt} parameter, the device power dissipation, and the method described in EIA/JESD Standard 51-2.

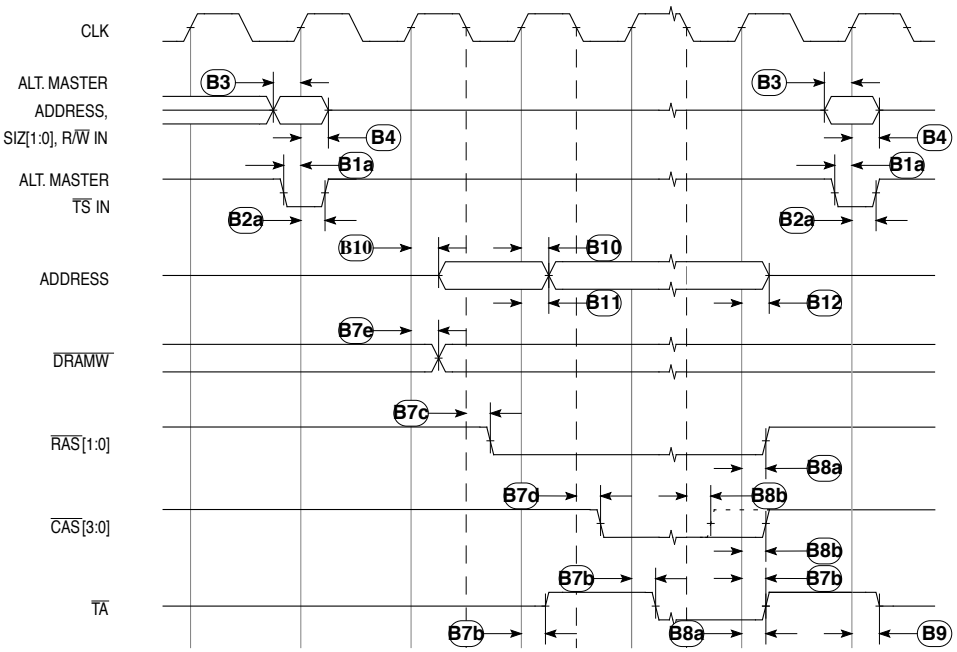
16.1.4 Output Loading

CHARACTERISTIC	SYMBOL	MAXIMUM	UNIT
Load Capacitance (All signals)	C_L	50	pF

16.2 DC ELECTRICAL SPECIFICATIONS

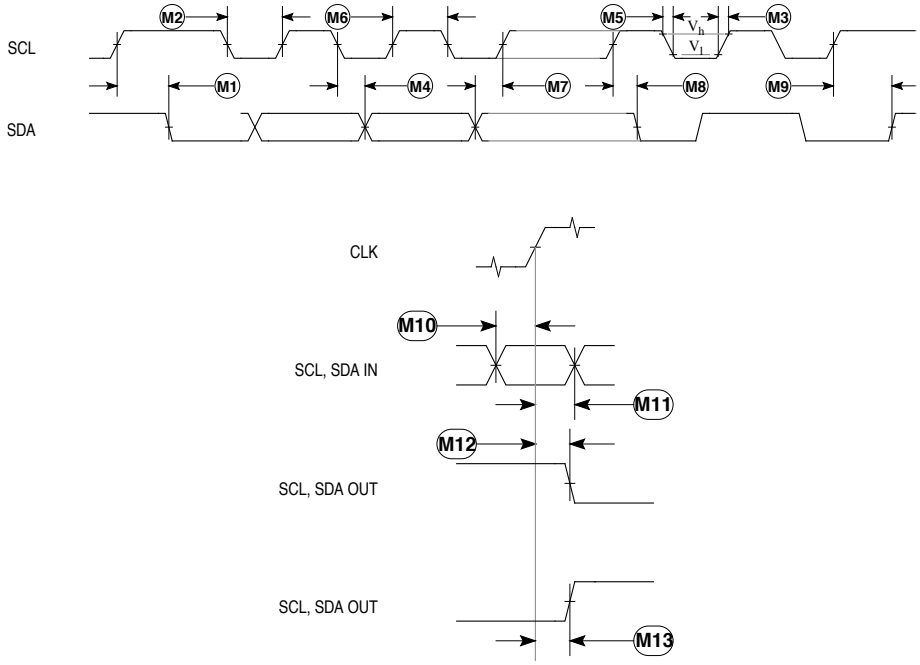
CHARACTERISTIC	SYMBOL	MIN	MAX	UNIT
Operation voltage range	V_{DD}	4.75	5.25	V
Input high voltage	V_{IH}	2	V_{DD}	V
Input low voltage	V_{IL}	GND	0.8	V
Input signal undershoot	–	–	0.8	V
Input signal overshoot	–	–	0.8	V
Input leakage current @ GND, V_{DD} CLK, A[27:0], D[31:0], $\overline{TS}$, SIZ[1:0], R/$\overline{W}$, $\overline{TA}$, $\overline{ATA}$, $\overline{TEA}$, IPL[2]/$\overline{IRQ}$[7], IPL[1]/$\overline{IRQ}$[4], IPL[0]/$\overline{IRQ}$[1], $\overline{BG}$, RxD[2:1], $\overline{CTS}$[2:1], TIN[1:0], PP[7:0]/PST[3:0]/DDATA[3:0], $\overline{RSTI}$, TCK, $\overline{HIZ}$, JTAG	I_{in}	–	20	µA
HI-Z (three-state) leakage current @GND, V_{DD} A[27:0], D[31:0], $\overline{TS}$, TT[1:0], ATM, SIZ[1:0], R/$\overline{W}$, $\overline{TA}$, TDO/DSO	I_{TSI}	–	20	µA
Signal Low Input Current, V_{IL} = 0.8V TMS/$\overline{BKPT}$, TDI/DSI, $\overline{TRST}$/DSCLK	I_{IL}	TBD	TBD	mA
Signal High Input Current, V_{IH} = 2.0V TMS/$\overline{BKPT}$, TDI/DSI, $\overline{TRST}$/DSCLK	I_{IH}	TBD	TBD	mA
Output high voltage, I_{OH} = 8mA (All signals except $\overline{RAS}$[1:0], $\overline{CAS}$[3:0], $\overline{DRAMW}$), I_{OH} = 16mA ($\overline{RAS}$[1:0], $\overline{CAS}$[3:0], $\overline{DRAMW}$)	V_{OH}	2.4	–	V
Output low voltage , I_{OL} = 8mA (All signals except $\overline{RAS}$[1:0], $\overline{CAS}$[3:0], $\overline{DRAMW}$), I_{OL} = 16mA ($\overline{RAS}$[1:0], $\overline{CAS}$[3:0], $\overline{DRAMW}$)	V_{OL}	–	0.5	V
Pin capacitance*	C_{in}	–	10	pF

* This specification periodically sampled but not 100% tested.



DRAM Control By Alternate Master Timing

16.3.13 M-Bus Module Timing Diagram



M-Bus Timing