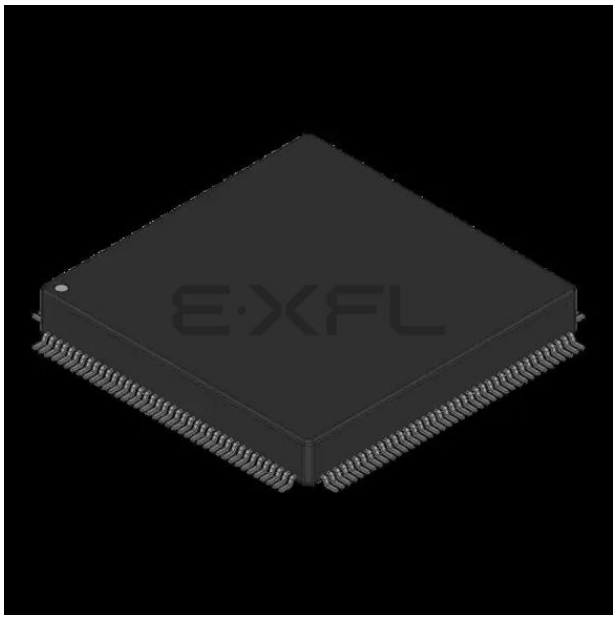
Motorola - MCF5206FT25A Datasheet



Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	Coldfire V2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	25MHz
Co-Processors/DSP	-
RAM Controllers	DRAM
Graphics Acceleration	-
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	160-BQFP
Supplier Device Package	160-QFP (28x28)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcf5206ft25a

TABLE OF CONTENTS (Continued)

Section 7

- ColdFire Processor Core
  - Variable-length RISC
  - 32-bit internal address bus with 28 bit external bus
  - Chip Select and DRAM
  - internal 32-bit decoding
  - 32-bit data bus
  - 16 user-visible 32-bit wide registers
  - Supervisor / User modes for system protection
  - Vector base register to relocate exception-vector table
  - Optimized for high-level language constructs
  - 17 MIPS at 33 MHz
- 512 Byte Direct-mapped instruction cache
- 512 Byte on-chip SRAM
  - Provides one-cycle access to critical code and data
- DRAM Controller
  - Programmable refresh timer provides CAS-before-RAS refresh
  - Support for 2 separate memory banks
  - Support for page-mode DRAMs and extended-data-out (EDO) DRAMs
  - Allows external bus master access
- Dual Universal Synchronous/Asynchronous Receiver/Transmitter (DUART)
  - Full duplex operation
  - Baud-rate generator
  - Modem control signals available ($\overline{\text{CTS}}$, $\overline{\text{RTS}}$)
  - Processor-interrupt capability
- Dual 16-Bit General-Purpose Multimode Timers
  - 8-bit prescaler
  - Timer input and output pins
  - 30ns resolution with 33 MHz system clock
  - Processor-interrupt capability
- Motorola Bus (M-Bus) Module
  - Interchip bus interface for EEPROMs, LCD controllers, A/D converters, keypads
  - Compatible with industry-standard I^2C Bus
  - Master or slave modes support multiple masters
  - Automatic interrupt generation with programmable level
- System Interface
  - Glueless bus interface to 8-, 16-, and 32-bit DRAM, SRAM, ROM, and I/O devices
  - 8 programmable chip-select signals
  - Programmable wait states and port sizes
  - Allows external bus masters to access chip-selects
  - System protection

  - 16-bit software watchdog timer with prescaler
  - Double bus fault monitor
  - Bus timeout monitor
  - Spurious interrupt monitor
- Programmable interrupt controller
  - Low interrupt latency
  - 3 external interrupt inputs
  - Programmable interrupt priority and autovector generator
- IEEE 1149.1 test (JTAG) support
- 8-bit general-purpose I/O interface

- System Debug Support
  - Real-time trace
  - Background debug interface
- Fully Static 5.0-Volt Operation
- 160 Pin QFP Package

contents of the fill buffer versus its corresponding cache location. At the time of the miss, the hardware indicator is set, marking the fill buffer as “most recently used.” If a subsequent access occurs to the cache location defined by bits [8:4] of the fill buffer address, the data in the cache memory array is now most recently used, so the hardware indicator is cleared. In all cases, the indicator defines whether the contents of the line fill buffer or the memory data array are most recently used. At the time of the next cache miss, the contents of the line-fill buffer are written into the memory array if the entire line is present, and the fill buffer data is still most recently used compared to the memory array.

The fill buffer can also be used as temporary storage for line-sized bursts of non-cacheable references under control of CACR[10]. With this bit set, a noncacheable instruction fetch is processed as defined by Table 4-2. For this condition, the fill buffer is loaded and subsequent references can hit in the buffer, but the data is never loaded into the memory array.

Table 4-2 shows the relationship between CACR bits 31 and 10 and the type of instruction fetch.

Table 4-2. Instruction Cache Operation as Defined by CACR[31, 10]

CACR[31]	CACR[10]	TYPE OF INSTR. FETCH	DESCRIPTION
0	0	N/A	Instruction cache is completely disabled; all fetches are word, longword in size.
0	1	N/A	All fetches are word, longword in size
1	X	Cacheable	Fetch size is defined by Table 5-1 and contents of the line-fill buffer can be written into the memory array
1	0	Noncacheable	All fetches are longword in size, and not loaded into the line-fill buffer
1	1	Noncacheable	Fetch size is defined by Table 5-1 and loaded into the line-fill buffer, but are never written into the memory array.

4.4 INSTRUCTION CACHE PROGRAMMING MODEL

Three supervisor registers define the operation of the instruction cache and local bus controller: the Cache Control Register (CACR) and two Access Control Registers (ACR0, ACR1).

4.4.1 Instruction Cache Registers Memory Map

Table 4-3 below shows the memory map of the Instruction cache and access control registers.

The following lists several keynotes regarding the programming model table:

- The Cache Control Register and Access Control Registers can only be accessed in supervisor mode using the MOVEC instruction with an Rc value of $002, $004 and $005, respectively.

DATE: 9-1-98
REVISION NO.: 1.1
PAGES AFFECTED: SEE CHANGE BARS

SECTION 5
SRAM

5.1 SRAM FEATURES

- 512 Byte SRAM, Organized as 128 x 32 Bits
- Single-Cycle Access
- Physically Located on ColdFire core's High-Speed Local Bus
- Byte, Word, Longword Address Capabilities
- Memory Mapping Defined by the Customer

5.2 SRAM OPERATION

The SRAM module provides a general-purpose memory block that the ColdFire core can access in a single cycle. You can specify the location of the memory block to any 0-modulo-512 address within the four gigabyte address space. The memory is ideal for storing critical code or data structures, or for use as the system stack. Because the SRAM module is physically connected to the processor's high-speed local bus, it can service core-initiated accesses, or memory-referencing commands from the debug module.

Depending on configuration information, instruction fetches can be sent to both the instruction cache and the SRAM block simultaneously. If the instruction fetch address is mapped into the region defined by the SRAM, the SRAM provides the data back to the processor, and the I-Cache data is discarded. Accesses from the SRAM module are not cached.

5.3 PROGRAMMING MODEL

5.3.1 SRAM Register Memory Map

Table 5-1 below shows the memory map of the SRAM register.

The following lists several keynotes regarding the programming model table:

- The SRAM base address register can only be accessed in supervisor mode using the MOVEC instruction with an Rc value of $C04.
- Addresses not assigned to the register and undefined register bits are reserved for future expansion. Write accesses to these reserved address spaces and reserved register bits have no effect; read accesses return zeros.
- The reset value column indicates the register initial value at reset. Certain registers can be uninitialized at reset, i.e., they may contain random values after reset.

of cycles used for each transfer. A bursted transfer can be from two to 16 transfers long. The flow chart shown is for four bursting transfers.

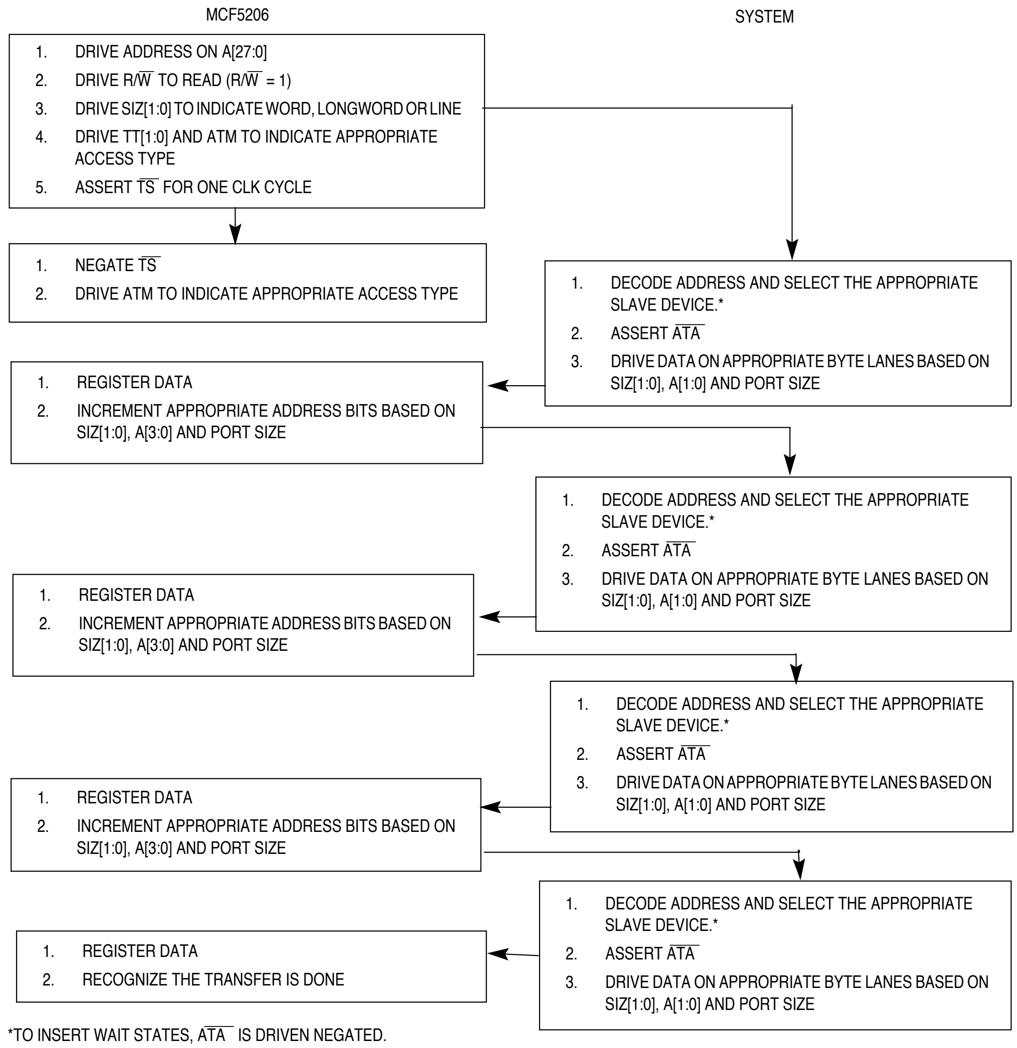


Figure 6-20. Bursting Word-, Longword-, and Line-Read Transfer with Asynchronous Termination Flowchart

Clock 3 (C3)

At the end of C3, the MCF5206 samples the level of internal asynchronous transfer acknowledge and if it is asserted, latches the current value of D[31:24]. If internal asynchronous transfer acknowledge is asserted, the transfer of the first byte is complete. If internal asynchronous transfer acknowledge is negated, the MCF5206 continues to sample internal asynchronous transfer acknowledge and inserts wait states instead of terminating the transfer. The MCF5206 continues to sample internal asynchronous transfer acknowledge until it is asserted. As long as $\overline{ATA}$ is asserted by the falling edge of C2, internal asynchronous transfer acknowledge is asserted by the rising edge of C3.

Clock 4 (C4)

This clock is identical to C1, except the address bus is incremented to point to the second byte of data.

Clock 5 (C5)

This clock is identical to C2.

Clock 6 (C6)

This clock is identical to C3, except once internal $\overline{ATA}$ is recognized, the data corresponds to the second byte of data.

6.5.11 Burst-Inhibited Write Transfers: Word, Longword, and Line with Asynchronous Acknowledge

The basic transfer of a burst-inhibited write using asynchronous termination is the same as “normal” write transfers with asynchronous termination but with the addition of more transfers until the entire operand has been accessed. Figure 6-26 is a flowchart for burst-inhibited write transfers to 8-, 16-, or 32-bit ports using asynchronous termination. Bus operations are similar for each case and vary only with the size indicated, the portion of the data bus used for the transfer, and the specific number of cycles needed for each transfer. The flowchart specifically depicts a burst-inhibited transfer of four accesses long.

NOTE

The MCF5206 can start a transfer during the CLK cycle after $\overline{BG}$ is asserted. The external arbiter should not assert $\overline{BG}$ to the MCF5206 until the previous external master has stopped driving the bus. $\overline{BG}$ cannot be asserted while another external master transfer is still in progress or damage to the part could occur.

When the bus has been removed from the MCF5206, one of two situations can occur. In the first case, the bus lock bit in the SIMR is cleared and the MCF5206 has explicit ownership of the bus. When the external bus master negates $\overline{BG}$, the MCF5206 completes the current transfer, then negate $\overline{BD}$ and three-state the address, data, $\overline{TS}$, R/$\overline{W}$, and SIZ signals after completing the current bus cycle.

In the second case, the bus lock bit in the SIMR is set to 1 and the MCF5206 has explicit ownership of the bus. In this case, when the external bus master negates $\overline{BG}$, the MCF5206 continues to assert $\overline{BD}$ and continues to drive address, attributes, and control signals. The MCF5206 retains mastership of the bus until the bus lock bit in the SIMR is cleared. By asserting the bus lock bit, you can select the MCF5206 to be the highest priority master, even when mastership of the bus is controlled by an external arbiter. In this fashion, the MCF5206 can be guaranteed mastership of the bus when executing time-

generate a spurious interrupt exception, $\overline{TEA}$ would have to be generated.

7.2.4 Software Watchdog Timer

The software watchdog timer (SWT) prevents system lockup in case the software becomes trapped in loops with no controlled exit. The SWT can be enabled via the software watchdog enable bit in the SYPCR. If enabled, the SWT requires a special service sequence execution on a periodic basis. If this periodic servicing action does not occur, the SWT times out and results in a hardware reset or a level 7 interrupt, as programmed by the software watchdog reset/interrupt select bit in the SYPCR. If the SWT times out and is programmed to generate a hardware reset, an internal reset is generated and the software watchdog timer reset bit in the reset status register is set. Additionally, if the RTS2/$\overline{RSTO}$ pin is programmed for $\overline{RSTO}$, $\overline{RSTO}$ is asserted for 32 CLK cycles. Refer to subsection **7.3.2.10 Pin Assignment Register (PAR)** for more information on programming. Also refer to the ColdFire WWW home page at http://www.mot.com/SPS/HPESD/prod/coldfire/MCF5206.html (Product Information Section) for samples of initialization code.

The 8-bit interrupt vector for the SWT interrupt is stored in the software watchdog interrupt vector register (SWIVR). The software watchdog prescalar (SWP) and software watchdog timing (SWT) bits in SYPCR determine the SWT time-out period.

The SWT service sequence consists of these two steps: write $55 to SWSR, then write $AA to the SWSR. Both writes must occur in the order listed prior to the SWT time-out, but any number of instructions or accesses to the SWSR can be executed between the two writes. This order allows interrupts and exceptions to occur, if necessary, between the two writes.

NOTE

If the SYSPCR is programmed for the SWT to generate an interrupt and the SWT times out, the SWT must be serviced in the interrupt handler routine by writing the $55, $AA sequence to the SWSR.

7.2.5 Interrupt Controller

The SIM provides a centralized interrupt controller for all MCF5206 interrupt sources, including:

- External Interrupts ($\overline{IPL}$/$\overline{IRQ}$)
- Software watchdog timer
- Timer modules
- MBUS (I^2C) module
- UART modules

All interrupt inputs are level sensitive. An interrupt request must be held valid for at least two consecutive CLK periods to be considered a valid input. The three external interrupt inputs

Chip Select Mask Register(CSMR2 - CSMR7)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BAM31	BAM30	BAM29	BAM28	BAM27	BAM26	BAM25	BAM24	BAM23	BAM22	BAM21	BAM20	BAM19	BAM18	BAM17	BAM16
RESET: -	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	SC	SD	UC	UD	-
RESET: 0	0	0	0	0	0	0	0	0	0	0	-	-	-	-	0

BAM31-BAM16 - Base Address Mask

This field defines the chip select block size through the use of address mask bits. Any bit set to 1 masks the corresponding base address register (CSAR) bit (the base address bit becomes a “don’t care” in the decode).

0 = Corresponding address bit is used in chip select address decode.
1 = Corresponding address bit is not used in chip select address decode.

C/I, SC, SD, UC, UD - CPU Space, Supervisor Code, Supervisor Data, User Code, User Data Transfer Mask

These fields allows specific types of transfers to be inhibited from accessing a chip select. If a transfer mask bit is cleared, a transfer of that type can access the corresponding chip select. If a transfer mask bit is set to 1, an transfer of that type can not access the corresponding chip select. The transfer mask bits are:

C/I = CPU space and Interrupt Acknowledge Cycle mask ($\overline{CS}$[1] only)
SC = Supervisor Code mask
SD = Supervisor Data mask
UC = User Code mask
UD = User Data mask

For each transfer mask bit:

0 = Do not mask this type of transfer for the chip select. A transfer of this type can occur for this chip select.
1 = Mask this type of transfer from the chip select. If this type of transfer is generated, this chip select activation is not activated.

NOTE

The C/I, SC, SD, UC, and UD bits are ignored during alternate master transfers. Therefore, an alternate master transfer can activate a chip select regardless of the transfer masks.

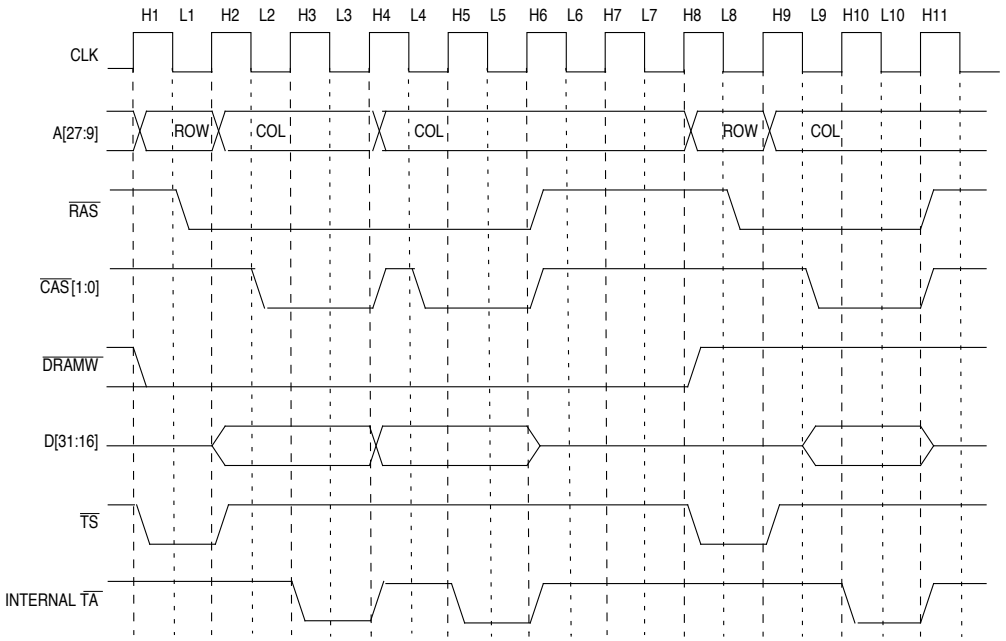


Figure 10-12. Longword Write Transfer Followed by a Word Read Transfer in Burst Page Mode with 16-Bit DRAM

Clock H1

The first word write transfer of the longword burst starts in H1. During H1, the MCF5206 drives the row address on A[27:9], drives $\overline{\text{DRAMW}}$ low indicating a DRAM write transfer, drives SIZ[1:0] to $0 indicating a longword transfer, and asserts $\overline{\text{TS}}$.

Clock L1

The MCF5206 asserts $\overline{\text{RAS}}$ to indicate the row address is valid on A[27:9].

Clock H2

The MCF5206 negates $\overline{\text{TS}}$, drives the column address on A[27:9], and begins driving the data on D[31:16].

Clock L2

The MCF5206 asserts $\overline{\text{CAS}}$[1:0] to indicate the column address is valid on A[27:9].

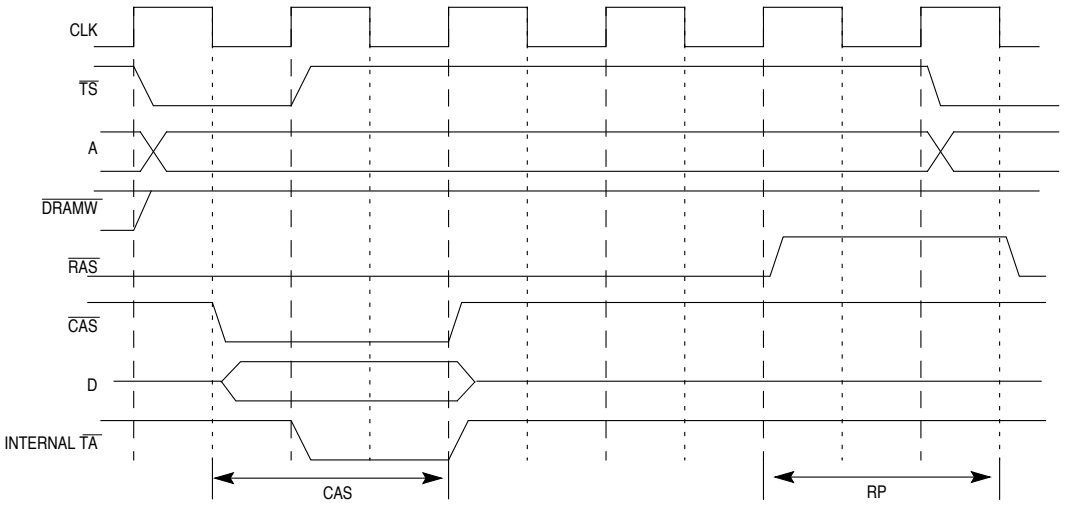


Figure 10-20. Fast Page Mode Page Hit and Page Miss DRAM Transfer Timing

CAS - Column Address Strobe Time

This field, together with the EDO field, controls the number of system clocks that $\overline{CAS}$ is asserted on transfers once a page is open in fast page mode and burst page mode. Refer to Figure 10-18 for timing diagrams of fast-page-mode or burst-page- mode transfers to standard DRAMs and Figure 10-21 for fast-page-mode or burst-page-mode transfers to EDO DRAMs.

For EDO = 0:

0 = $\overline{CAS}$ is asserted for 1.5 system clocks
1 = $\overline{CAS}$ is asserted for 2.5 system clocks

For EDO = 1:

0 = $\overline{CAS}$ is asserted for 1.0 system clock
1 = $\overline{CAS}$ is asserted for 2.0 system clocks

You can use this feature for flow control to prevent overrun in the receiver by using the $\overline{RTS}$ output to control the $\overline{CTS}$ input of the transmitting device. If both the receiver and transmitter are programmed for $\overline{RTS}$ control, $\overline{RTS}$ control is disabled for both because such a configuration is incorrect. See **Section 11.4.1.2 Mode Register 2 (UMR2)** for information on programming the transmitter $\overline{RTS}$ control. On UART 2, $\overline{RTS}$ is muxed.

RxIRQ — Receiver Interrupt Select

1 = FFULL is the source that generates IRQ
0 = RxRDY is the source that generates IRQ

ERR — Error Mode

This bit controls the meaning of the three FIFO status bits (RB, FE, and PE) in the USR.

1 = Block mode—The values in the channel USR are the accumulation (i.e., the logical OR) of the status for all characters coming to the top of the FIFO since the last reset error status command for the channel was issued. Refer to **Section 11.4.1.5 Command Register (UCR)** for more information on UART module commands.
0 = Character mode—The values in the channel USR reflect the status of the character at the top of the FIFO.

NOTE

You must use ERR = 0 to obtain the correct A/$\overline{D}$ flag information when in multidrop mode.

PM1–PM0 — Parity Mode

These bits encode the type of parity used for the channel (see Table 11-3). The parity bit is added to the transmitted character and the receiver performs a parity check on incoming data. These bits can alternatively select multidrop mode for the channel.

PT — Parity Type

This bit selects the parity type if parity is programmed by the parity mode bits; if multidrop mode is selected, it configures the transmitter for data character transmission or address character transmission. Table 11-3 lists the parity mode and type or the multidrop mode for each combination of the parity mode and the parity type bits.

Table 11-3. PMx and PT Control Bits

PM1	PM0	PARITY MODE	PT	PARITY TYPE
0	0	With Parity	0	Even Parity
0	0	With Parity	1	Odd Parity
0	1	Force Parity	0	Low Parity
0	1	Force Parity	1	High Parity
1	0	No Parity	X	No Parity
1	1	Multidrop Mode	0	Data Character
1	1	Multidrop Mode	1	Address Character

while the receiver shifts and updates from the bottom of the stack when the shift register has been filled (see Figure 11-4).

URB — MBAR + $18C

7	6	5	4	3	2	1	0
RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
RESET:							
1	1	1	1	1	1	1	1

READ ONLY — SUPERVISOR OR USER

RB7–RB0 — These bits contain the character in the receiver buffer.

11.4.1.7 TRANSMITTER BUFFER (UTB). The transmitter buffer consists of two registers: the transmitter-holding register and the transmitter shift register (see Figure 11-4). The holding register accepts characters from the bus master if the TxRDY bit in the channel's USR is set. A write to the transmitter buffer clears the TxRDY bit, inhibiting additional characters until the shift register is ready to accept more data. When the shift register is empty, it checks the holding register for a valid character to be sent (TxRDY bit cleared). If a valid character is present, the shift register loads the character and reasserts the TxRDY bit in the USR. Writes to the transmitter buffer when the channel's UART Status Register (USR) TxRDY bit is clear and when the transmitter is disabled have no effect on the transmitter buffer.

UTB — MBAR + $18C

7	6	5	4	3	2	1	0
TB7	TB6	TB5	TB4	TB3	TB2	TB1	TB0
RESET:							
0	0	0	0	0	0	0	0

WRITE ONLY — SUPERVISOR OR USER

TB7–TB0 — These bits contain the character in the transmitter buffer.

11.4.1.8 INPUT PORT CHANGE REGISTER (UIPCR). The UIPCR shows the current state and the change-of-state for the $\overline{\text{CTS}}$ pin.

UIPCR — MBAR + $190

7	6	5	4	3	2	1	0
0	0	0	COS	1	1	1	CTS
RESET:							
0	0	0	0	1	1	1	1

READ ONLY — SUPERVISOR OR USER

1. The occurrence of the catastrophic fault-on-fault condition automatically halts the processor. The halt status is posted on the PST port ($F).
2. The occurrence of a hardware breakpoint (reference subsection **Section 14.3 Real-Time Debug Support**) can be configured to generate a pending halt condition in a manner similar to the assertion of the $\overline{\text{BKPT}}$ signal. In some cases, the occurrence of this type of breakpoint halts the processor in an imprecise manner. Once the hardware breakpoint is asserted, the processor halts at the next sample point. See **Section 14.3.2 Theory of Operation** for more detail.
3. The execution of the HALT (also known as BGND on the 683xx devices) instruction immediately suspends execution and posts the halt status ($F) on the PST outputs. By default, this is a supervisor instruction and attempted execution while in user mode generates a privilege-violation exception. A User Halt Enable (UHE) control bit is provided in the Configuration/Status Register (CSR) to allow execution of HALT in user mode.
4. The assertion of the $\overline{\text{BKPT}}$ input pin is treated as an pseudo-interrupt, i.e., the halt condition is made pending until the processor core samples for halts/interrupts. The processor samples for these conditions once during the execution of each instruction. If there is a pending halt condition at the sample time, the processor suspends execution and enters the halted state. The halt status ($F) is reflected in the PST outputs.

The halt source is indicated in CSR[27:24]; for simultaneous halt conditions, the highest priority source is indicated.

There are two special cases to be considered that involve the assertion of the $\overline{\text{BKPT}}$ pin.

After $\overline{\text{RSTI}}$ is negated, the processor waits for 16 clock cycles before beginning reset exception processing. If the $\overline{\text{BKPT}}$ input pin is asserted within the first eight cycles after $\overline{\text{RSTI}}$ is negated, the processor enters the halt state, signaling that status on the PST outputs ($F). While in this state, all resources accessible via the Debug module can be referenced. Once the system initialization is complete, the processor response to a BDM GO command depends on the set of BDM commands performed while “breakpointed.” Specifically, if the processor’s PC register was loaded, the GO command causes the processor to exit the halt state and pass control to the instruction address contained in the PC. In this case, the normal reset exception processing is bypassed. Conversely, if the PC register was not loaded, the GO BDM command causes the processor to exit the halt state and continue with reset exception processing.

ColdFire 52xx processors also handle a special case with the assertion of $\overline{\text{BKPT}}$ while the processor is stopped by execution of the STOP instruction. For this case when the $\overline{\text{BKPT}}$ is asserted, the processor exits the stopped mode and enters the halted state. Once halted, the standard BDM commands may be exercised. When the processor is restarted, it continues with the execution of the next sequential instruction, i.e., the instruction following the STOP opcode.

The debug module Configuration/Status Register (CSR) maintains status defining the condition that caused the CPU to halt.

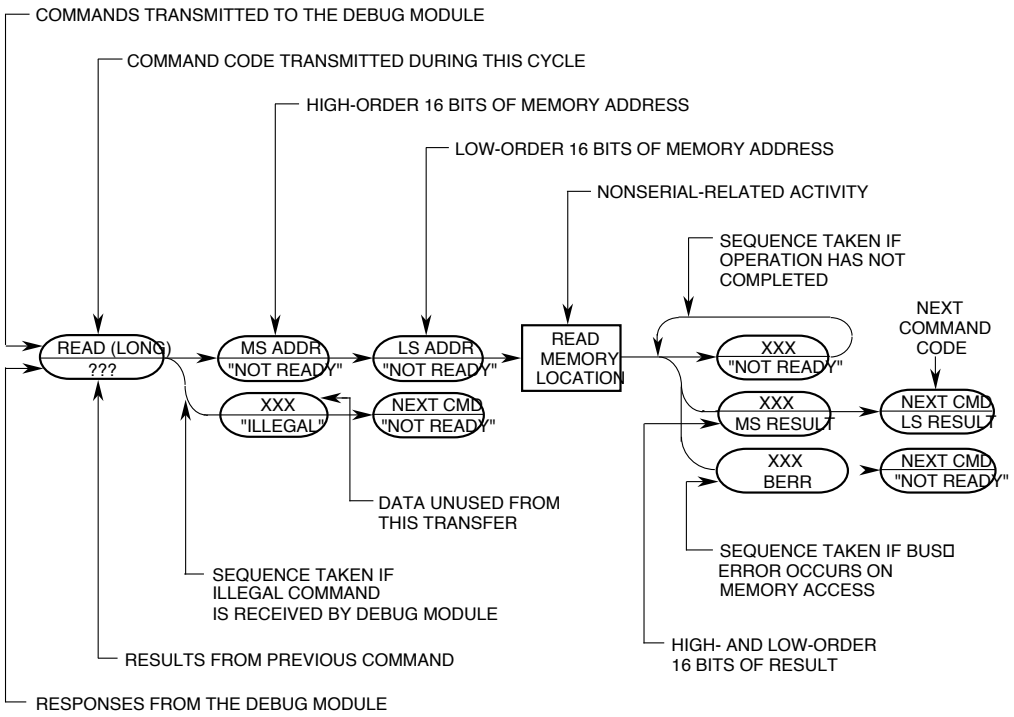


Figure 14-4. Command Sequence Diagram

14.2.3.4 Command Set Descriptions. The BDM command set is summarized in Table 14-3.

Note

All the accompanying valid BDM results are defined with the most significant bit of the 17-bit response (S/C) as 0. Invalid command responses (Not Ready; TEA-terminated bus cycle; Illegal Command) return a 1 in the most significant bit of the 17-bit response (S/C).

Motorola reserves unassigned command opcodes for future expansion. All unused command formats within any revision level performs a NOP and return the ILLEGAL command response.

Command Formats:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$1				$D				$0				$0			

Byte DUMP Command

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X	DATA [7:0]							

Byte DUMP Result

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$1				$D				$4				$0			

Word DUMP Command

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA [15:0]															

Word DUMP Result

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$1				$D				$8				$0			

Long DUMP Command

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA [31:16]															
DATA [15:0]															

Long DUMP Result