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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	M16C/60
Core Size	16-Bit
Speed	20MHz
Connectivity	CANbus, I²C, IEBus, SIO, UART/USART
Peripherals	DMA, POR, PWM, Voltage Detect, WDT
Number of I/O	71
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 27x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30290fahp-u3a

1. Overview

1.1 Features

The M16C/29 Group of single-chip control MCU incorporates the M16C/60 series CPU core, employing the high-performance silicon gate CMOS technology and sophisticated instructions for a high level of efficiency. The M16C/29 Group is housed in 64-pin and 80-pin plastic molded LQFP packages. These single-chip MCUs operate using sophisticated instructions featuring a high level of instruction efficiency. This MCU is capable of executing instructions at high speed and it has one CAN module, makes it suitable for control of cars and LAN system of FA. In addition, the CPU core boasts a multiplier and DMAC for high-speed processing to make adequate for office automation, communication devices, and other high-speed processing applications.

1.1.1 Applications

Automotive body, car audio, LAN system of FA, etc.

1.1.2 Specifications

Table 1.1 lists performance overview of M16C/29 Group 80-pin package.

Table 1.2 lists performance overview of M16C/29 Group 64-pin package.

Table 1.1 Performance Overview of M16C/29 Group (T-ver./V-ver.) (80-Pin Package)

Item		Performance
CPU	Number of basic instructions	91 instructions
	Shortest instruction excution time	50 ns (f(BCLK) = 20MHz, VCC = 3.0 to 5.5 V) (Normal-ver./T-ver.) 100 ns(f(BCLK) = 10MHz, VCC = 2.7 to 5.5 V) (Normal-ver.) 50 ns (f(BCLK) = 20MHz, VCC = 4.2 to 5.5 V, -40 to 105°C) (V-ver.) 62.5 ns (f(BCLK) = 16MHz, VCC = 4.2 to 5.5 V, -40 to 125°C) (V-ver.)
	Operation mode	Single chip mode
	Address space	1 Mbyte
	Memory capacity	ROM/RAM: See **Tables 1.3 to 1.5**
Peripheral Function	Port	Input/Output: 71 lines
	Multifunction timer	TimerA:16 bits x 5 channels, TimerB:16 bits x 3 channels Three-phase Motor Control Timer TimerS (Input Capture/Output Compare): 16 bit base timer x 1 channel (Input/Output x 8 channels)
	Serial I/O	2 channels (UART, clock synchronous serial I/O) 1 channel (UART, clock synchronous serial I/O, I2C bus, or IEbus(1)) 2 channels (Clock synchronous serial I/O) 1 channel (Multi- master I2C bus)
	A/D converter	10 bits x 27 channels
	DMAC	2 channels
	CRC calculation circuit	2 polynomial (CRC-CCITT and CRC-16) with MSB/LSB selectable
	CAN module	1 channel, supporting CAN 2.0B specification
	Watchdog timer	15 bits x 1 channel (with prescaler)
	Interrupt	29 internal and 8 external sources, 4 software sources, interrupt priority level: 7
	Clock generation circuit	4 circuits • Main clock, • Sub-clock (These circuits contain a built-in feedback resistor) • On-chip oscillator(main-clock oscillation stop detect function) • PLL frequency synthesizer
	Oscillation stop detect Function	Main clock oscillation stop, re-oscillation detect function
	Voltage detection circuit	Available (Normal-ver.) / Not available (T-ver., V-ver.)
Electrical Charact-eristics	Power supply voltage	VCC = 3.0 to 5.5 V (f(BCLK) = 20 MHz) (Normal-ver.) VCC = 2.7 to 5.5 V (f(BCLK) = 10 MHz)
		VCC = 3.0 to 5.5 V (T-ver.)
		VCC = 4.2 to 5.5 V (V-ver.)
	Power consumption	18 mA (VCC = 5 V, f(BCLK) = 20 MHz) 25 µA (f(XCIN) = 32 kHz on RAM) 3 µA (VCC = 5 V, f(XCIN) = 32 kHz, in wait mode) 0.8 µA (VCC = 5 V, in stop mode)
Flash memory	Program/erase supply voltage	2.7 to 5.5 V (Normal-ver.), 3.0 to 5.5V (T-ver.), 4.2 to 5.5 V (V-ver.)
	Program and erase endurance	100 times (all space) or 1,000 times (blocks 0 to 5)/ 10,000 times (blocks A and B(2))
Operating ambient temperature		-20 to 85°C/-40 to 85°C(2) (Normal-ver.)
		-40 to 85°C (T-ver.), -40 to 125°C (V-ver.)
Package		80-pin plastic mold LQFP

NOTES:
1. IEBus is a trademark of NEC Electronics Corporation.
2. Refer to **Table 1.6** to **Table 1.8 Product code**.

Table 4.5 SFR Information (5)

Address	Register	Symbol	After reset
0100$_{16}$	CAN0 message box 10: Identifier/DLC		XX$_{16}$
0101$_{16}$			XX$_{16}$
0102$_{16}$			XX$_{16}$
0103$_{16}$			XX$_{16}$
0104$_{16}$			XX$_{16}$
0105$_{16}$			XX$_{16}$
0106$_{16}$	CAN0 message box 10 : Data field		XX$_{16}$
0107$_{16}$			XX$_{16}$
0108$_{16}$			XX$_{16}$
0109$_{16}$			XX$_{16}$
010A$_{16}$			XX$_{16}$
010B$_{16}$			XX$_{16}$
010C$_{16}$			XX$_{16}$
010D$_{16}$			XX$_{16}$
010E$_{16}$	CAN0 message box 10 : Time stamp		XX$_{16}$
010F$_{16}$			XX$_{16}$
0110$_{16}$	CAN0 message box 11 : Identifier/DLC		XX$_{16}$
0111$_{16}$			XX$_{16}$
0112$_{16}$			XX$_{16}$
0113$_{16}$			XX$_{16}$
0114$_{16}$			XX$_{16}$
0115$_{16}$			XX$_{16}$
0116$_{16}$	CAN0 message box 11 : Data field		XX$_{16}$
0117$_{16}$			XX$_{16}$
0118$_{16}$			XX$_{16}$
0119$_{16}$			XX$_{16}$
011A$_{16}$			XX$_{16}$
011B$_{16}$			XX$_{16}$
011C$_{16}$			XX$_{16}$
011D$_{16}$			XX$_{16}$
011E$_{16}$	CAN0 message box 11 : Time stamp		XX$_{16}$
011F$_{16}$			XX$_{16}$
0120$_{16}$	CAN0 message box 12: Identifier/DLC		XX$_{16}$
0121$_{16}$			XX$_{16}$
0122$_{16}$			XX$_{16}$
0123$_{16}$			XX$_{16}$
0124$_{16}$			XX$_{16}$
0125$_{16}$			XX$_{16}$
0126$_{16}$	CAN0 message box 12: Data field		XX$_{16}$
0127$_{16}$			XX$_{16}$
0128$_{16}$			XX$_{16}$
0129$_{16}$			XX$_{16}$
012A$_{16}$			XX$_{16}$
012B$_{16}$			XX$_{16}$
012C$_{16}$			XX$_{16}$
012D$_{16}$			XX$_{16}$
012E$_{16}$	CAN0 message box 12 : Time stamp		XX$_{16}$
012F$_{16}$			XX$_{16}$
0130$_{16}$	CAN0 message box 13 : Identifier/DLC		XX$_{16}$
0131$_{16}$			XX$_{16}$
0132$_{16}$			XX$_{16}$
0133$_{16}$			XX$_{16}$
0134$_{16}$			XX$_{16}$
0135$_{16}$			XX$_{16}$
0136$_{16}$	CAN0 message box 13 : Data field		XX$_{16}$
0137$_{16}$			XX$_{16}$
0138$_{16}$			XX$_{16}$
0139$_{16}$			XX$_{16}$
013A$_{16}$			XX$_{16}$
013B$_{16}$			XX$_{16}$
013C$_{16}$			XX$_{16}$
013D$_{16}$			XX$_{16}$
013E$_{16}$	CAN0 message box 13 : Time stamp		XX$_{16}$
013F$_{16}$			XX$_{16}$

Note 1: The blank areas are reserved and cannot be used by users.

X : Undefined

5. Resets

Hardware reset 1, brown-out detection reset (hardware reset 2), software reset, watchdog timer reset, and oscillation stop detection reset are implemented to reset the MCU.

5.1 Hardware Reset

Hardware reset 1 and brown-out detection reset are available as the hardware reset.

5.1.1 Hardware Reset 1

Pins, CPU, and SFRs are reset by using the $\overline{\text{RESET}}$ pin. When a low-level ("L") signal is applied to the $\overline{\text{RESET}}$ pin while the supply voltage meets the recommended operating condition, pins, CPU, and SFRs are reset (see **Table 5.1** Pin Status When $\overline{\text{RESET}}$ Pin Level is "L"). The oscillation circuit is also reset and the on-chip oscillator starts oscillating as the CPU clock. CPU and SFRs re reset when the signal applied to the $\overline{\text{RESET}}$ pin changes from "L" to high ("H"). The MCU executes a program beginning with the address indicated by the reset vector. The internal RAM is not reset. When an "L" signal is applied to the $\overline{\text{RESET}}$ pin while writing data to the internal RAM, the content of internal RAM is undefined.
Figure 5.1 shows an example of the reset circuit. **Figure 5.2** shows a reset sequence. **Table 5.1** shows status of the other pins while the $\overline{\text{RESET}}$ pin is held "L". **Figure 5.3** shows CPU register states after reset. Refer to **4. Special Function Register (SFR)** about SFR states after reset.

1. Reset on a stable supply voltage
(1) Apply an "L" signal to the $\overline{\text{RESET}}$ pin
(2) Wait *td(ROC)* or more
(3) Apply an "H" signal to the $\overline{\text{RESET}}$ pin

2. Power-on reset
(1) Apply an "L" signal to the $\overline{\text{RESET}}$ pin
(2) Increase the supply voltage until it meets the the recommended performance condition
(3) Wait for *td(P-R)* or more to allow the internal power supply to stabilize
(4) Wait *td(ROC)* or more
(5) Apply an "H" signal to the $\overline{\text{RESET}}$ pin

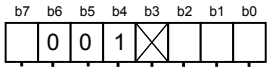
5.1.2 Brown-Out Detection Reset (Hardware Reset 2)

Note

Brown-out detection reset in the M16C/29 Group, T-ver. and V-ver. cannot be used.

Pins, CPU, and SFR are reset by using the on-chip voltage detection circuit, which monitors the voltage applied to V_{CC} pin.
When the VC26 bit in the VCR2 register is set to 1 (reset level detection circuit enabled), pins, CPU, and SFR are reset as soon as the voltage applied to the V_{CC} pin drops to Vdet3 or below.
Then, pins, CPU, and SFR are reset as soon as the voltage applied to the V_{CC} pin reaches Vdet3r or above. The MCU executes the program in an address determined by the reset vector.
The MCU executes the program after detecting Vdet3r and waiting *td(S-R)* ms. The same pins and registers are reset by the hardware reset 1 and brown-out detection reset, and are also placed in the same reset state.
The MCU cannot exit stop mode by brown-out detection reset.

PLL Control Register 0 (1,2)

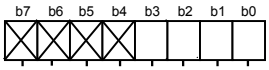


Symbol	Address	After Reset
PLC0	001C16	0001X0102

Bit Symbol	Bit Name	Function	RW
PLC00	PLL multiplying factor select bit (3)	b2 b1 b0 0 0 0: Do not set 0 0 1: Multiply by 2 0 1 0: Multiply by 4 0 1 1: } Do not set 1 0 0: } 1 0 1: } 1 1 0: } 1 1 1: }	RW
PLC01			RW
PLC02			RW
(b3)	Nothing is assigned. If necessary, set to 0. When read, the content is undefined		—
(b4)	Reserved bit	Set to 1	RW
(b6-b5)	Reserved bit	Set to 0	RW
PLC07	Operation enable bit (4)	0: PLL Off 1: PLL On	RW

NOTES:
1. Write to this register after setting the PRC0 bit in the PRCR register to 1 (write enable).
2. When the PM21 bit in the PM2 register is 1 (clock modification disable), writing to this register has no effect.
3. These three bits can only be modified when the PLC07 bit is set to 0 (PLL turned off). The value once written to this bit cannot be modified.
4. Before setting this bit to 1 , set the CM07 bit to 0 (main clock), set bits CM17 to CM16 bits to 002 (main clock undivided mode), and set the CM06 bit to 0 (CM16 and CM17 bits enable).

CAN0 Clock Select Register (1)



Symbol	Address	After Reset
CCLKR	025F16	0016

Bit Symbol	Bit Name	Function	RW
CCLK0	CAN0 clock select bits(2)	b2 b1 b0 0 0 0 No division 0 0 1: Divide-by-2 0 1 0: Divide-by-4 0 1 1: Divide-by-8 1 0 0: Divide-by-16 1 0 1: } Inhibited 1 1 0: } 1 1 1: }	RW
CCLK1			RW
CCLK2			RW
CCLK3	CAN0 CPU interface sleep bit(3)	0: CAN0 CPU interface operating 1: CAN0 CPU interface in sleep	RW
(b7-b4)	Nothing is assigned. If necessary, set to 0. When read, the content is 0		RW

NOTES:
1. Write to this register after setting the PRC0 bit in the PRCR register to 1 (write enable).
2. Configuration of bits CCLK2 to CCLK0 can be done only when the Reset bit in the C0CTLR register is set to 1 (Reset/Initialization mode).
3. Before setting this bit to 1(CAN0 CPU interface in sleep), set the Sleep bit in C0CTLR register to 1 (Sleep mode).

Figure 7.7 PLC0 Register and CCLKR register

13.1.1 Base Timer Reset Register(G1BTRR)

The G1BTRR register provides the capability to reset the base timer when the base timer count value matches the value stored in the G1BTRR register. The G1BTRR register is enabled by the RST4 bit in the G1BCR0 register. This function is identical in operation to the G1PO0 base timer reset that is enabled by the RST1 bit in the G1BCR0 reigster. If the free-running operation is not selected, the channel 0 can be used for a waveform generation when the base timer is reset by the G1BTRR register. Do not enable bits RST1 and RST4 simultaneously.

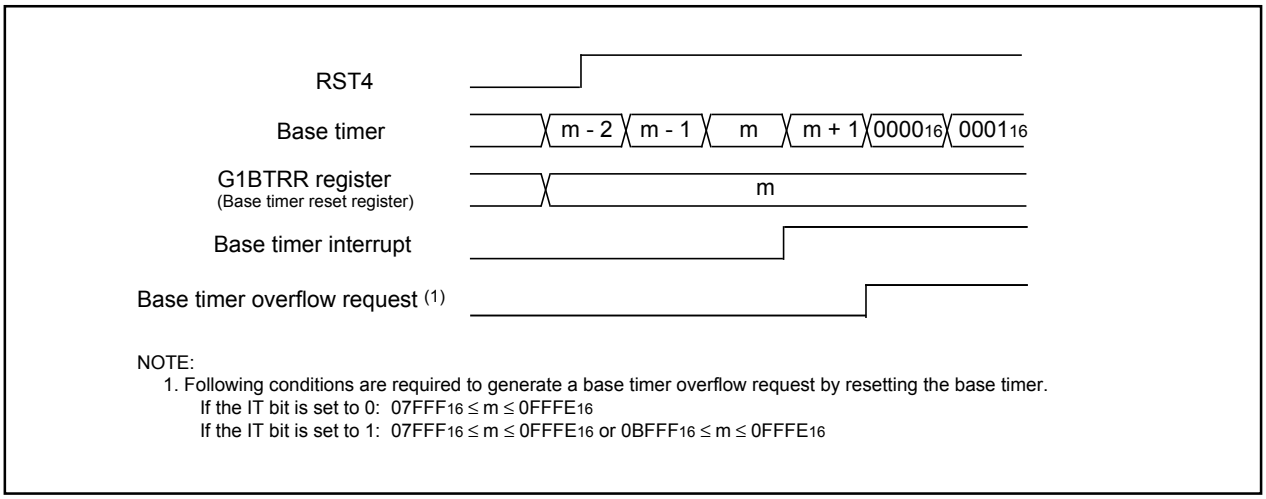


Figure 13.15 Base Timer Reset operation by Base Timer Reset Register

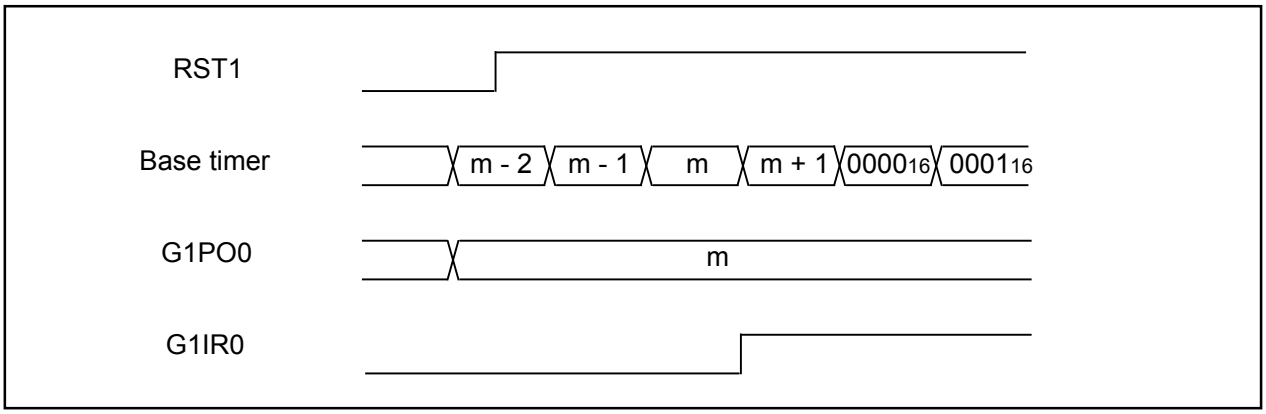


Figure 13.16 Base Timer Reset operation by G1PO0 register

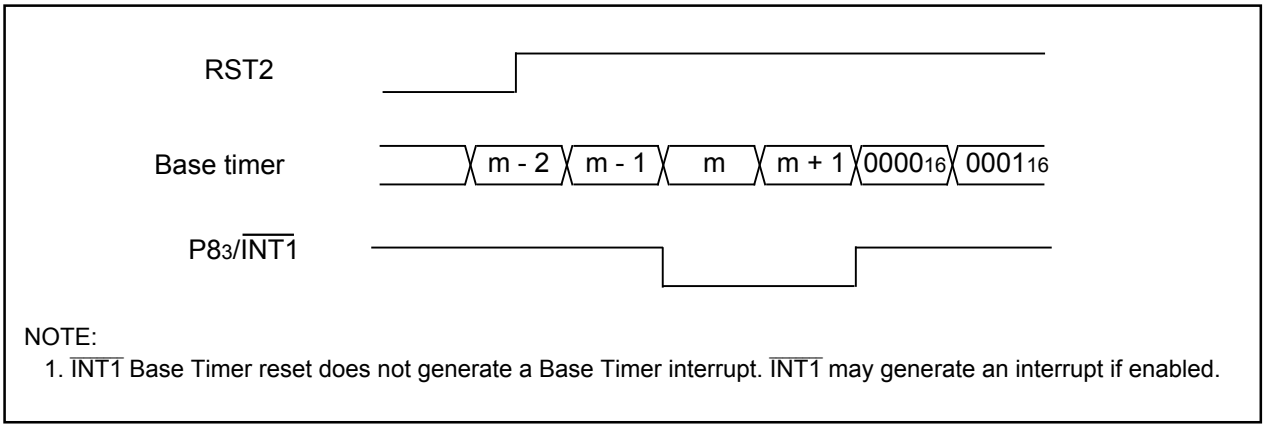


Figure 13.17 Base Timer Reset operation by $\overline{INT1}$

UARTi Transmit/receive Control Rregister 0 (i=0 to 2)

b7	b6	b5	b4	b3	b2	b1	b0

Symbol	Address	After Reset
U0C0 to U2C0	$03A4_{16}$, $03AC_{16}$, $037C_{16}$	00001000_2

Bit Symbol	Bit Name	Function	RW
CLK0	BRG count source select bit(7)	b1 b0 0 0 : $f1_{SIO}$ or $f2_{SIO}$ is selected 0 1 : $f8_{SIO}$ is selected 1 0 : $f32_{SIO}$ is selected 1 1 : Do not set	RW
CLK1			RW
CRS	$\overline{CTS}/\overline{RTS}$ function select bit(3)	Effective when CRD is set to 0 0 : $\overline{CTS}$ function is selected (1) 1 : $\overline{RTS}$ function is selected	RW
TXEPT	Transmit register empty flag	0 : Data present in transmit register (during transmission) 1 : No data present in transmit register (transmission completed)	RO
CRD	$\overline{CTS}/\overline{RTS}$ disable bit	0 : $\overline{CTS}/\overline{RTS}$ function enabled 1 : $\overline{CTS}/\overline{RTS}$ function disabled ($P6_0$, $P6_4$ and $P7_3$ can be used as I/O ports)(6)	RW
NCH	Data output select bit(5)	0 : TxD2/SDA2 and SCLi pins are CMOS output 1 : TxD2/SDA2 and SCLi pins are N-channel open-drain output(4)	RW
CKPOL	CLK polarity select bit	0 : Transmit data is output at falling edge of transfer clock and receive data is input at rising edge 1 : Transmit data is output at rising edge of transfer clock and receive data is input at falling edge	RW
UFORM	Transfer format select bit (2)	0 : LSB first 1 : MSB first	RW

NOTES:
1. Set the corresponding port direction bit for each $\overline{CTSi}$ pin to 0 (input mode).
2. Effective when bits SMD2 to SMD0 in the UMR register to 001_2 (clock synchronous serial I/O mode) or 010_2 (UART mode transfer data 8 bits long). Set the UFORM bit to 1 when bits SMD2 to SMD0 are set to 101_2 (I^2C bus mode) and 0 when they are set to 100_2.
3. $\overline{CTS1}/\overline{RTS1}$ can be used when the CLKMD1 bit in the UCON register is set to 0 (only CLK_1 output) and the RCSP bit in the UCON register is set to 0 ($\overline{CTS0}/\overline{RTS0}$ not separated).
4. SDA2 and SCL2 are effective when i = 2.
5. When bits SMD2 to SMD in the UiMR regiser are set to 000_2 (serial I/O disable), do not set NCH bit to 1 (TxDi/SDA2 and SCL2 pins are N-channel open-drain output).
6. When the U1MAP bit in PACR register is 1 ($P7_3$ to $P7_0$), $P7_0$ functions as $\overline{CTS}/\overline{RTS}$ pin in UART1.
7. When the CLK1 and CLK0 bit settings are changed, set the UiBRG register.

UART Transmit/receive Control Register 2

b7	b6	b5	b4	b3	b2	b1	b0
X							

Symbol	Address	After Reset
UCON	$03B0_{16}$	$X0000000_2$

Bit Symbol	Bit Name	Function	RW
U0IRS	UART0 transmit interrupt cause select bit	0 : Transmit buffer empty (TI = 1) 1 : Transmission completed (TXEPT = 1)	RW
U1IRS	UART1 transmit interrupt cause select	0 : Transmit buffer empty (TI = 1) 1 : Transmission completed (TXEPT = 1)	RW
U0RRM	UART0 continuous receive mode enable bit	0 : Continuous receive mode disabled 1 : Continuous receive mode enable	RW
U1RRM	UART1 continuous receive mode enable bit	0 : Continuous receive mode disabled 1 : Continuous receive mode enabled	RW
CLKMD0	UART1 CLK/CLKS select bit 0	Effective when the CLKMD1 bit is set to 1 0 : Clock output from CLK1 1 : Clock output from CLKS1	RW
CLKMD1	UART1 CLK/CLKS select bit 1 (1)	0 : Output from CLK1 only 1 : Transfer clock output from multiple pins function selected	RW
RCSP	Separate UART0 $\overline{CTS}/\overline{RTS}$ bit	0 : $\overline{CTS}/\overline{RTS}$ shared pin (2) 1 : $\overline{CTS}/\overline{RTS}$ separated ($P6_4$ pin functions as $\overline{CTS0}$ pin)	RW
(b7)	Nothing is assigned. If necessary, set to 0. When read, the content is undefined		—

NOTES:
1. When using multiple transfer clock output pins, make sure the following conditions are met:set the CKDIR bit in the U1MR register to 0 (internal clock)
2. When the U1MAP bit in PACR register is set to 1 ($P7_3$ to $P7_0$), $P7_0$ pin functions as $\overline{CTS0}$ pin.

Figure 14.6 U0C0 to U2C0 and UCON Registers

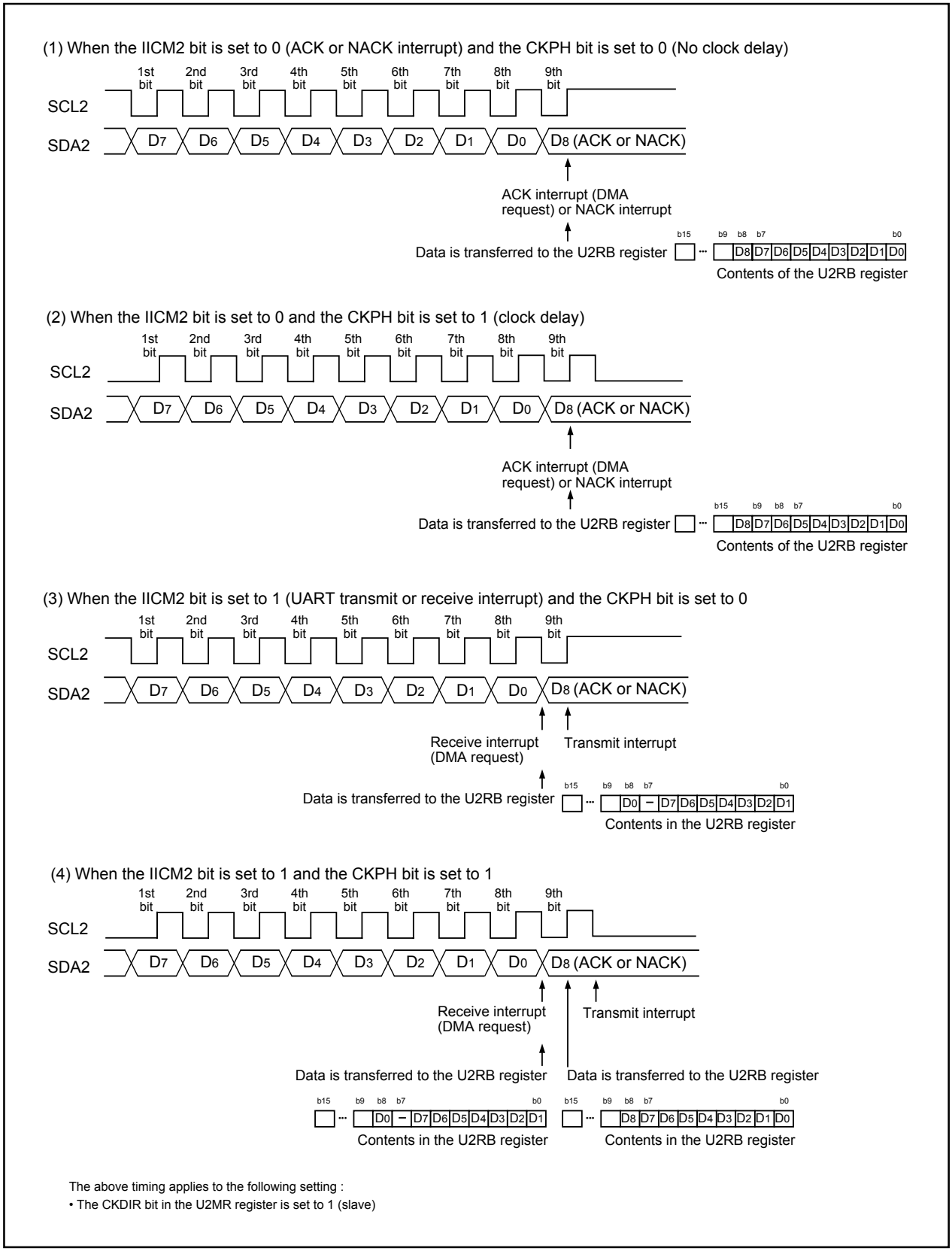
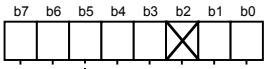


Figure 14.23 Transfer to U2RB Register and Interrupt Timing

A/D Conversion Status Register 0 (1)



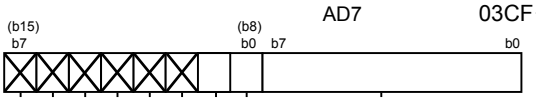
Symbol	Address	After reset
ADSTAT0	03D316	0016

Bit Symbol	Bit Name	Function	RW
ADERR0	AN1 trigger status flag	0: AN1 trigger did not occur during AN0 conversion 1: AN1 trigger occured during AN0 conversion	RW
ADERR1	Conversion termination flag	0: Conversion not terminated 1: Conversion terminated by Timer B0 underflow	RW
(b2)	Nothing is assigned. If necessary, set to 0. When read, its content is 0		—
ADTCSF	Delayed trigger sweep status flag	0: Sweep not in progress 1: Sweep in progress	RO
ADSTT0	AN0 conversion status flag	0: AN0 conversion not in progress 1: AN0 conversion in progress	RO
ADSTT1	AN1 conversion status flag	0: AN1 conversion not in progress 1: AN1 conversion in progress	RO
ADSTRT0	AN0 conversion completion status flag	0: AN0 conversion not completed 1: AN0 conversion completed	RW
ADSTRT1	AN1 conversion completion status flag	0: AN1 conversion not completed 1: AN1 conversion completed	RW

NOTE:
1. ADSTAT0 register is valid only when the DTE bit in the ADTRGCON register is set to 1.

A/D Register i (i=0 to 7)

Symbol	Address	After Reset
AD0	03C116 to 03C016	Undefined
AD1	03C316 to 03C216	Undefined
AD2	03C516 to 03C416	Undefined
AD3	03C716 to 03C616	Undefined
AD4	03C916 to 03C816	Undefined
AD5	03CB16 to 03CA16	Undefined
AD6	03CD16 to 03CC16	Undefined
AD7	03CF16 to 03CE16	Undefined



Function		RW
When the BITS bit in the ADCON1 register is 1 (10-bit mode)	When the BITS bit in the ADCON1 register is 0 (8-bit mode)	RW
Eight low-order bits of A/D conversion result	A/D conversion result	RO
Two high-order bits of A/D conversion result	When read, its content is undefined	RO
Nothing is assigned. If necessary, set to 0. When read, its content is 0		—

Figure 15.4 ADSTAT0 Register and AD0 to AD7 Registers

15.1 Operating Modes

15.1.1 One-Shot Mode

In one-shot mode, analog voltage applied to a selected pin is once converted to a digital code. **Table 15.3** shows the one-shot mode specifications. **Figure 15.6** shows the operation example in one-shot mode. **Figure 15.7** shows registers ADCON0 to ADCON2 in one-shot mode.

Table 15.3 One-shot Mode Specifications

Item	Specification
Function	Bits CH2 to CH0 in the ADCON0 register and registers ADGSEL1 and ADGSEL0 in the ADCON2 register select pins. Analog voltage applied to a selected pin is once converted to a digital code
A/D Conversion Start Condition	• When the TRG bit in the ADCON0 register is 0 (software trigger) Set the ADST bit in the ADCON0 register to 1 (A/D conversion started) • When the TRG bit in the ADCON0 register is 1 (hardware trigger) The $\overline{\text{ADTRG}}$ pin input changes state from “H” to “L” after setting the ADST bit to 1 (A/D conversion started)
A/D Conversion Stop Condition	• A/D conversion completed (If a software trigger is selected, the ADST bit is set to 0 (A/D conversion halted)). • Set the ADST bit to 0
Interrupt Request Generation Timing	A/D conversion completed
Analog Input Pin	Select one pin from AN_0 to AN_7, $AN0_0$ to $AN0_7$, $AN2_0$ to $AN2_7$, $AN3_0$ to $AN3_2$
Readout of A/D Conversion Result	Readout one of registers AD0 to AD7 that corresponds to the selected pin

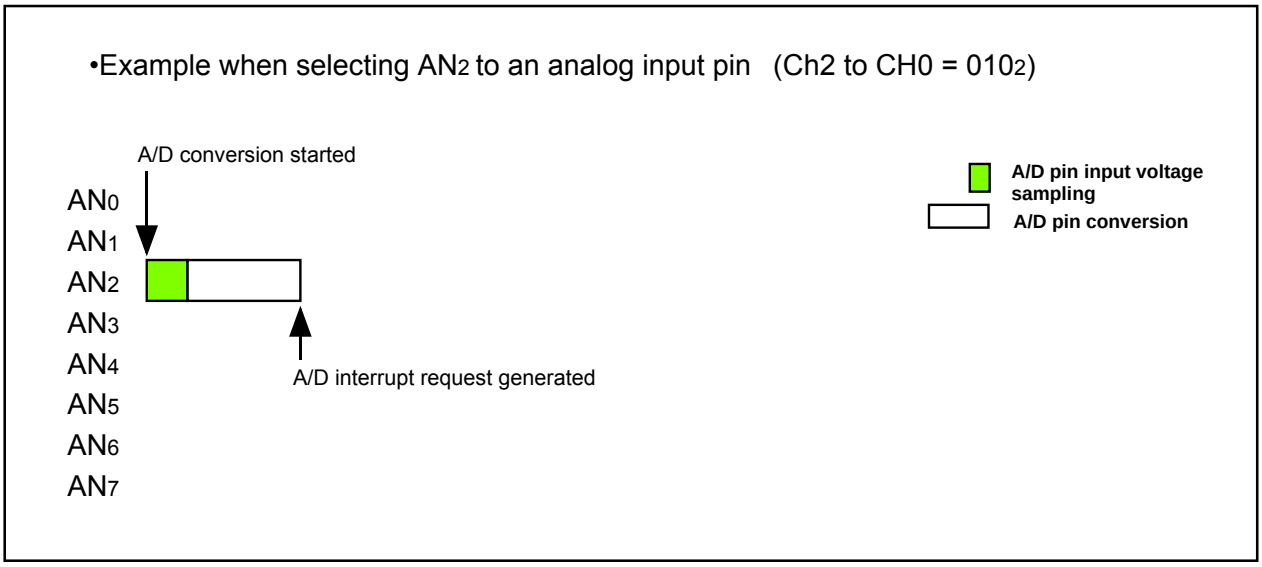


Figure 15.6 Operation Example in One-Shot Mode

15.1.5 Repeat Sweep Mode 1

In repeat sweep mode 1, analog voltage is applied to the all selected pins are converted to a digital code, with mainly used in the selected pins. **Table 15.7** shows the repeat sweep mode 1 specifications. **Figure 15.14** shows the operation example in repeat sweep mode 1. **Figure 15.15** shows registers ADCON0 to ADCON2 in repeat sweep mode 1.

Table 15.7 Repeat Sweep Mode 1 Specifications

Item	Specification
Function	Bits SCAN1 and SCAN0 in the ADCON1 register and bits ADGSEL1 and ADGSEL0 in the ADCON2 register mainly select pins. Analog voltage applied to the all selected pins is repeatedly converted to a digital code Example : When selecting AN_0 Analog voltage is converted to a digital code in the following order $AN_0 \rightarrow AN_1 \rightarrow AN_0 \rightarrow AN_2 \rightarrow AN_0 \rightarrow AN_3$, and so on.
A/D Conversion Start Condition	• When the TRG bit in the ADCON0 register is 0 (software trigger) Set the ADST bit in the ADCON0 register to 1 (A/D conversion started) • When the TRG bit in the ADCON0 register is 1 (hardware trigger) The $\overline{ADTRG}$ pin input changes state from “H” to “L” after setting the ADST bit to 1 (A/D conversion started)
A/D Conversion Stop Condition	Set the ADST bit to 0 (A/D conversion halted)
Interrupt Request Generation Timing	None generated
Analog Input Pins Mainly Used in A/D Conversions	Select from AN_0 (1 pins), AN_0 to AN_1 (2 pins), AN_0 to AN_2 (3 pins), AN_0 to AN_3 (4 pins) (1)
Readout of A/D Conversion Result	Readout one of registers AD0 to AD7 that corresponds to the selected pin

NOTES:

1. $AN0_0$ to $AN0_7$, $AN2_0$ to $AN2_7$, and $AN3_0$ to $AN3_2$ can be used in the same way as AN_0 to AN_7. However, all input pins need to belong to the same group.

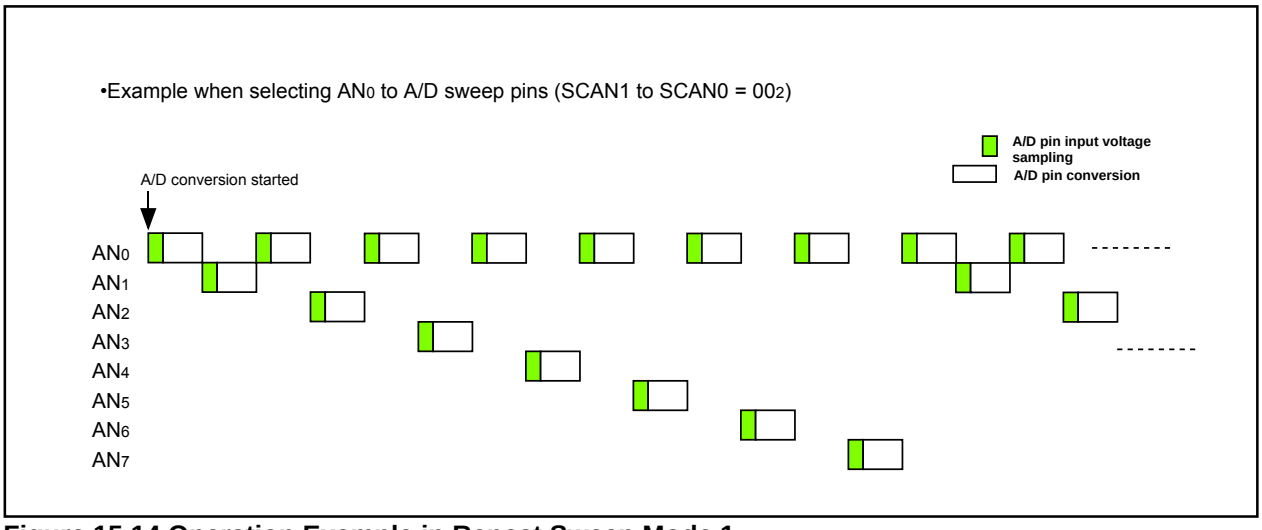


Figure 15.14 Operation Example in Repeat Sweep Mode 1

15.2 Resolution Select Function

The BITS bit in the ADCON1 register determines the resolution. When the BITS bit is set to 1 (10-bit precision), the A/D conversion result is stored into bits 0 to 9 in the ADi register (i=0 to 7). When the BITS bit is set to 0 (8-bit precision), the A/D conversion result is stored into bits 7 to 0 in the ADi register.

15.3 Sample and Hold

When the SMP bit in the ADCON 2 register is set to 1 (with the sample and hold function), A/D conversion rate per pin increases to 28 ϕAD cycles for 8-bit resolution or 33 ϕAD cycles for 10-bit resolution. The sample and hold function is available in one-shot mode, repeat mode, single sweep mode, repeat sweep mode 0 and repeat sweep mode 1. In these modes, start A/D conversion after selecting whether the sample and hold circuit is to be used or not. In simultaneous sample sweep mode, delayed trigger mode 0 or delayed trigger mode, set to use the Sample and Hold function before starting A/D conversion.

15.4 Power Consumption Reducing Function

When the A/D converter is not used, the VCUT bit in the ADCON1 register isolates the resistor ladder of the A/D converter from the reference voltage input pin (V_{REF}). Power consumption is reduced by shutting off any current flow into the resistor ladder from the V_{REF} pin.

When using the A/D converter, set the VCUT bit to 1 (Vref connected) before setting the ADST bit in the ADCON0 register to 1 (A/D conversion started). Do not set the ADST bit and VCUT bit to 1 simultaneously, nor set the VCUT bit to 0 (Vref unconnected) during A/D conversion.

16.5.5 Bit 4: I2C bus Interface Interrupt Request Bit (PIN)

The PIN bit generates an I2C bus interface interrupt request signal. Every one byte data is ransferred, the PIN bit is changed from 1 to 0. At the same time, an I2C bus interface interrupt request is generated. The PIN bit is synchronized with the last clock of the internal transfer clock (when ACK-CLK=1, the last clock is the ACK clock: when the ACK-CLK=0, the last clock is the 8th clock) and it becomes 0. The interrupt request is generated on the falling edge of the PIN bit. When the PIN bit is set to 0, the clock applied to SCL maintains "L" and further clock generation is disabled. When the ACK-CLK bit is set to 1 and the WIT bit in the S3D0 register is set to 1 (enable the I2C bus interface interrupt of data receive completion). The PIN bit is synchronized with the last clock and the falling edge of the ACK clock. Then, the PIN bit is set to 0 and I2C bus interface interrupt request is generated. **Figure 16.11** shows the timing of the I2C bus interface interrupt request generation.

The PIN bit is set to 1 in one of the following conditions:

- •When data is written to the S00 register
- •When data is written to the S20 register (when the WIT bit is set to 1 and the internal WAIT flag is set to 1)
- •When the ES0 bit in the S1D0 register is set to 0 (I2C bus interface disabled)
- •When the IHR bit in the S1D0 register is set to 1(reset)

The PIN bit is set to 0 in one of the following conditions:

- •With completion of 1-byte data transmit (including a case when arbitration lost is detected)
- •With completion of 1-byte data receive
- •When the ALS bit in the S1D0 register is set to 0 (addressing format) and slave address is matched or general call address is received successfully in slave receive mode
- •When the ALS bit is set to 1 (free format) and the address data is received successfully in slave receive mode

16.5.6 Bit 5: Bus Busy Flag (BB)

The BB flag indicates the operating conditions of the bus system. When the BB flag is set to 0, a bus system is not in use and a START condition can be generated. The BB flag is set and reset based on an input signal of the SCL and SDA pins either in master mode or in slave mode. When the START condition is detected, the BB flag is set to 1. On the other hand, when the STOP condition is detected, the BB flag is set to 0. Bits SSC4 to SSC0 in the S2D0 register decide to detect between the START condition and the STOP condition. When the ES0 bit in the S1D0 register is set to 0 (I2C bus interface disabled) or when the IHR bit in the S1D0 register is set to 1 (reset), the BB flag is set to 0. Refer to **16.9 START Condition Generation Method and 16.11 STOP Condition Generation Method**.

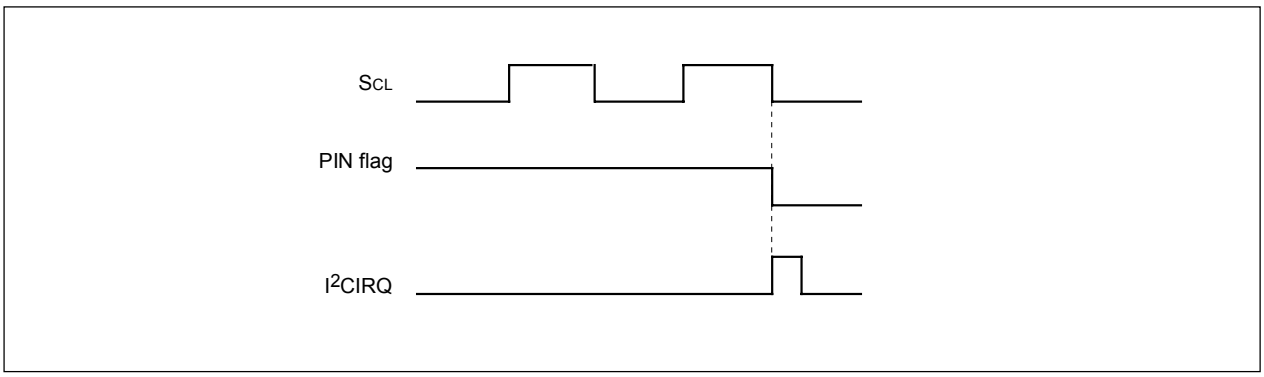
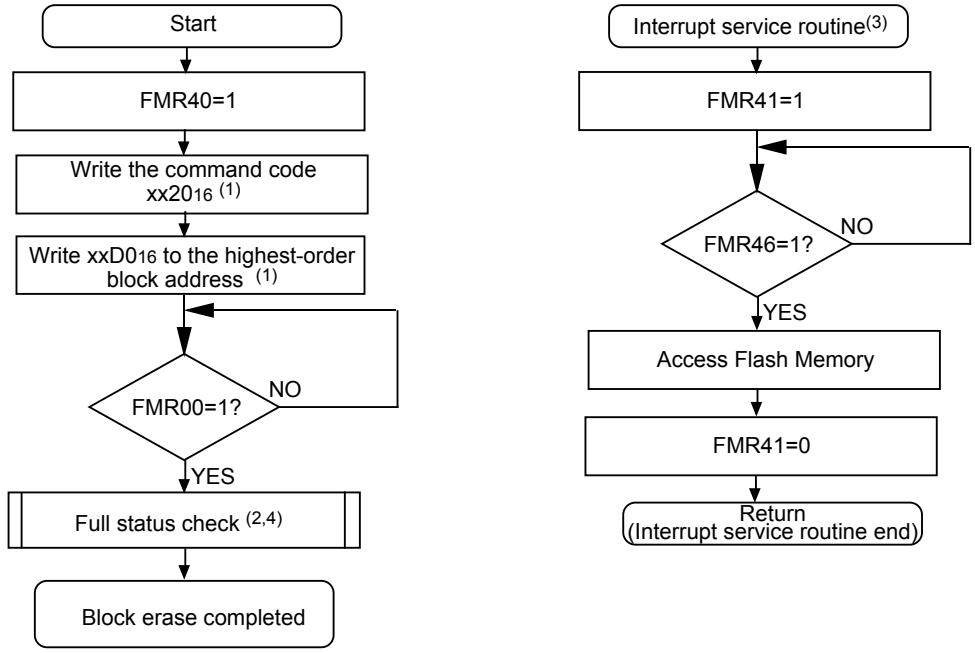
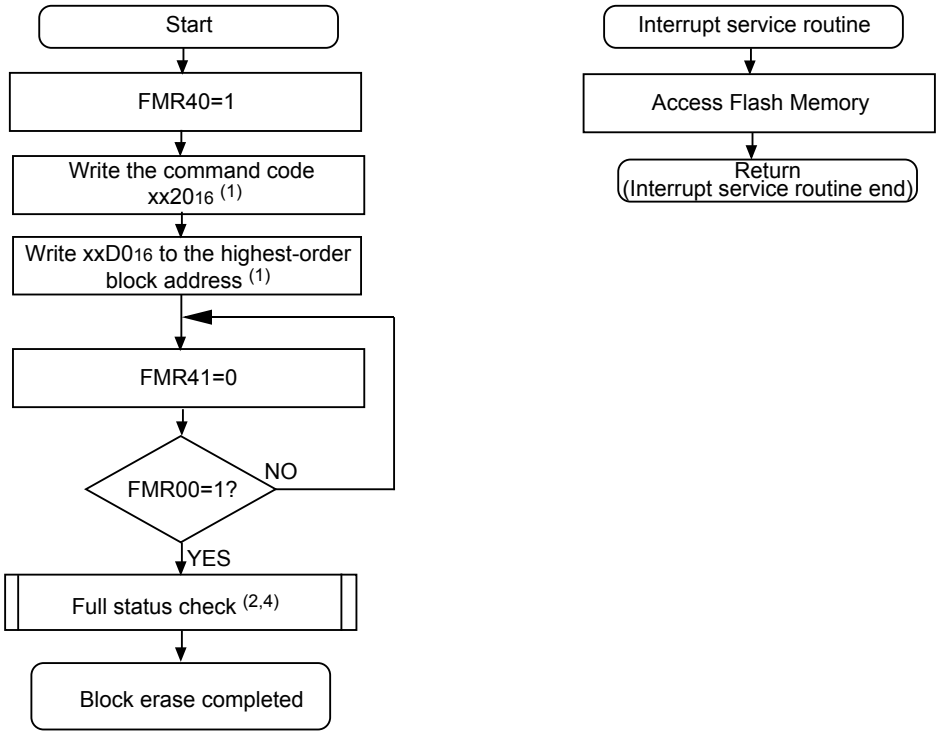


Figure 16.11 Interrupt request signal generation timing

(EW mode 0)



(EW mode 1)



NOTES:
1. Write the command code and data to even address.
2. Execute the clear status register command and block erase command at least 3 times until an erase error is not generated when an erase error is generated.
3. In EW mode 0, allocate an interrupt vector table of an interrupt, to be used, to the RAM area
4. Refer to **Figure 20.14**.

Figure 20.13 Block Erase Command (at use erase suspend)

20.11 CAN I/O Mode

Note

The CAN I/O mode is not available in M16C/29 T-ver./V-ver.

In CAN I/O mode, the user ROM area can be rewritten while the MCU is mounted on-board by using a CAN programmer which is applicable for the M16C/29 group. For more information about CAN programmers, contact the manufacturer of your CAN programmer. For details on how to use, refer to the user's manual included with your CAN programmer.
Table 20.9 lists pin functions for CAN I/O mode. Figures 20.19 and 20.20 show pin connections for CAN I/O mode.

20.11.1 ID code check function

This function determines whether the ID codes sent from the CAN programmer and those written in the flash memory match.(Refer to **20.3 Functions To Prevent Flash Memory from Rewriting**.)

V_{CC} = 5V

Timing Requirements

(V_{CC} = 5V, V_{SS} = 0V, at Topr = – 20 to 85°C / – 40 to 85°C unless otherwise specified)

Table 21.23 Multi-master I^2C bus Line

Symbol	Parameter	Standard clock mode		High-speed clock mode		Unit
		Min.	Max.	Min.	Max.	
tBUF	Bus free time	4.7		1.3		µs
tHD;STA	The hold time in start condition	4.0		0.6		µs
tLOW	The hold time in SCL clock 0 status	4.7		1.3		µs
tR	SCL, SDA signals' rising time		1000	20+0.1Cb	300	ns
tHD;DAT	Data hold time	0		0	0.9	µs
tHIGH	The hold time in SCL clock 1 status	4.0		0.6		µs
tF	SCL, SDA signals' falling time		300	20+0.1Cb	300	ns
tSU;DAT	Data setup time	250		100		ns
tSU;STA	The setup time in restart condition	4.7		0.6		µs
tSU;STO	Stop condition setup time	4.0		0.6		µs

Table 21.43 Flash Memory Version Electrical Characteristics (1) for 100/1000 E/W cycle products

[Program Space and Data Space in U3; Program Space in U7]

Symbol	Parameter		Standard			Unit
			Min.	Typ.(2)	Max.	
-	Program and Erase Endurance(3)		100/1000(4, 11)			cycles
-	Word Program Time (Vcc = 5.0 V, Topr = 25° C)			75	600	µs
-	Block Erase Time (Vcc = 5.0 V, Topr = 25° C)	2-Kbyte Block		0.2	9	s
		8-Kbyte Block		0.4	9	s
		16-Kbyte Block		0.7	9	s
		32-Kbyte Block		1.2	9	s
td(SR-ES)	Duration between Suspend Request and Erase Suspend				8	ms
tPS	Wait Time to Stabilize Flash Memory Circuit				15	µs
-	Data Hold Time (5)		20			years

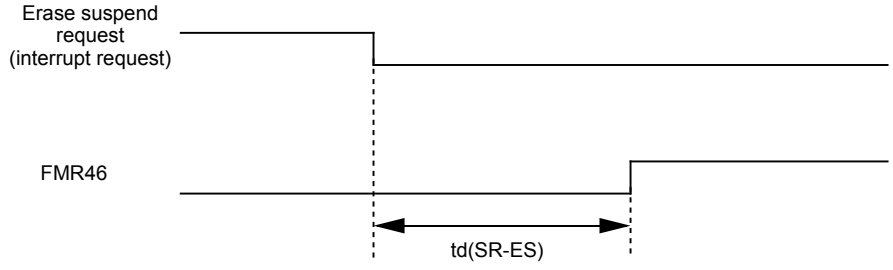
Table 21.44 Flash Memory Version Electrical Characteristics (6) for 10000 E/W cycle products

[Data Space in U7(7)]

Symbol	Parameter	Standard			Unit
		Min.	Typ.(2)	Max.	
-	Program and Erase Endurance(3, 8, 9)	10000(4, 10)			cycles
-	Word Program Time (Vcc = 5.0 V, Topr = 25° C)		100		µs
-	Block Erase Time (Vcc = 5.0V, Topr = 25° C) (2-Kbyte block)		0.3		s
td(SR-ES)	Duration between Suspend Request and Erase Suspend			8	ms
tPS	Wait Time to Stabilize Flash Memory Circuit			15	µs
-	Data Hold Time (5)	20			years

NOTES:

1. Referenced to VCC = 3.0 to 5.5 V at Topr = 0 to 60° C (program space)/ Topr = -40 to 85° C(data space), unless otherwise specified.
2. VCC = 5.0 V; TOPR = 25° C
3. Program and erase endurance is defined as number of program-erase cycles per block.
   If program and erase endurance is *n* cycle (*n* = 100, 1000, 10000), each block can be erased and programmed *n* cycles.
   For example, if a 2-Kbyte block A is erased after programming one-word data to each address 1,024 times, this counts as one program and erase endurance. Data cannot be programmed to the same address more than once without erasing the block. (rewrite prohibited).
4. Number of E/W cycles for which operation is guranteed (1 to minimum value are guranteed).
5. Topr = 55° C
6. Referenced to VCC = 3.0 to 5.5 V at Topr = -40 to 85° C unless otherwise specified.
7. **Table 21.44** applies for data space in U7 when program and erase endurance is more than 1,000 cycles. Otherwise, use **Table 21.43**.
8. To reduce the number of program and erase endurance when working with systems requiring numerous rewrites, write to unused word addresses within the block instead of rewrite. Erase block only after all possible addresses are used. For example, an 8-word program can be written 128 times maximum before erase becomes necessary. Maintaining an equal number of times erasure between block A and block B will also improve efficiency. It is recommended to track the total number of erasure performed per block and to limit the number of erasure.
9. If an erase error is generated during block erase, execute the clear status register command and block erase command at least 3 times until an erase error is not generated.
10. When executing more than 100 times rewrites, set one wait state per block access by setting the FMR17 bit in the FMR1 register to 1 (wait state). When accessing to all other blocks and internal RAM, wait state can be set by the PM17 bit, regardless of the FMR17 bit setting value.
11. The program and erase endurance is 100 cycles for program space and data space in U3; 1,000 cycles for program space in U7.
12. Please contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor for further details on the E/W failure rate.



22.4.6 Rewrite the Interrupt Control Register

(1) The interrupt control register for any interrupt should be modified in places where no requests for that interrupt may occur. Otherwise, disable the interrupt before rewriting the interrupt control register.

(2) To rewrite the interrupt control register for any interrupt after disabling that interrupt, be careful with the instruction to be used.

Changing any bit other than the IR bit

If while executing an instruction, a request for an interrupt controlled by the register being modified occurs, the IR bit in the register may not be set to 1 (interrupt requested), with the result that the interrupt request is ignored. If such a situation presents a problem, use the instructions shown below to modify the register.

Usable instructions: AND, OR, BCLR, BSET

Changing the IR bit

Depending on the instruction used, the IR bit may not always be cleared to 0 (interrupt not requested). Therefore, be sure to use the MOV instruction to clear the IR bit.

(3) When using the I flag to disable an interrupt, refer to the sample program fragments shown below as you set the I flag. (Refer to (2) for details about rewrite the interrupt control registers in the sample program fragments.)

Examples 1 through 3 show how to prevent the I flag from being set to 1 (interrupts enabled) before the interrupt control register is rewrited, due to the internal bus and the instruction queue buffer.

Example 1: Using the NOP instruction to keep the program waiting until the interrupt control register is modified

```
INT_SWITCH1:
      FCLR    I              ; Disable interrupts
      AND.B   #00h, 0055h    ;Set the TA0IC register to 00₁₆
      NOP                    ;
      NOP
      FSET    I              ; Enable interrupts
```

The number of NOP instruction is as follows.
PM20 = 1 (1 wait) : 2, PM20 = 0 (2 waits): 3

Example 2:Using the dummy read to keep the FSET instruction waiting

```
INT_SWITCH2:
      FCLR    I              ; Disable interrupts
      AND.B   #00h, 0055h    ; Set the TA0IC register to 00₁₆
      MOV.W   MEM, R0        ; Dummy read
      FSET    I              ; Enable interrupts
```

Example 3:Using the POPC instruction to changing the I flag

```
INT_SWITCH3:
      PUSHC   FLG
      FCLR    I              ; Disable interrupts
      AND.B   #00h, 0055h    ; Set the TA0IC register to 00₁₆
      POPC    FLG            ; Enable interrupts
```

22.4.7 Watchdog Timer Interrupt

Initialize the watchdog timer after the watchdog timer interrupt occurs.

22.6.2 Timer B

22.6.2.1 Timer B (Timer Mode)

1. The timer remains idle after reset. Set the mode, count source, counter value, etc. using the TBiMR (i = 0 to 2) register and TBi register before setting the TBiS bit in the TABSR register to 1 (count starts).
   Always make sure the TBiMR register is modified while the TBiS bit remains 0 (count stops) regardless whether after reset or not.

2. The counter value can be read out at any time by reading the TBi register. However, if this register is read at the same time the counter is reloaded, the read value is always FFFF16. If the TBi register is read after setting a value in it but before the counter starts counting, the read value is the one that has been set in the register.

22.6.2.2 Timer B (Event Counter Mode)

1. The timer remains idle after reset. Set the mode, count source, counter value, etc. using the TBiMR (i = 0 to 2) register and TBi register before setting the TBiS bit in the TABSR register to 1 (count starts).
   Always make sure the TBiMR register is modified while the TBiS bit remains 0 (count stops) regardless whether after reset or not.

2. The counter value can be read out at any time by reading the TBi register. However, if this register is read at the same time the counter is reloaded, the read value is always FFFF16. If the TBi register is read after setting a value in it but before the counter starts counting, the read value is the one that has been set in the register.

22.6.2.3 Timer B (Pulse Period/pulse Width Measurement Mode)

1. The timer remains idle after reset. Set the mode, count source, etc. using the TBiMR (i = 0 to 2) register before setting the TBiS bit in the TABSR or the TBSR register to 1 (count starts).
   Always make sure the TBiMR register is modified while the TBiS bit remains 0 (count stops) regardless whether after reset or not. To clear the MR3 bit to 0 by writing to the TBiMR register while the TBiS bit is set to 1 (count starts), be sure to write the same value as previously written to bits TM0D0, TM0D1, MR0, MR1, TCK0, and TCK1 and a 0 to the MR2 bit.

2. The IR bit in TBiIC register (i=0 to 2) goes to 1 (interrupt request), when an effective edge of a measurement pulse is input or timer Bi is overflowed. The factor of interrupt request can be determined by use of the MR3 bit in TBiMR register within the interrupt routine.

3. If the source of interrupt cannot be identified by the MR3 bit such as when the measurement pulse input and a timer overflow occur at the same time, use another timer to count the number of times timer B has overflowed.

4. To set the MR3 bit to 0 (no overflow), set TBiMR register with setting the TBiS bit to 1 and counting the next count source after setting the MR3 bit to 1 (overflow).

5. Use the IR bit in TBiIC register to detect only overflows. Use the MR3 bit only to determine the interrupt factor within the interrupt routine.

22.9 A/D Converter

1. Set registers ADCON0 (except bit 6), ADCON1, ADCON2 and ADTRGCON when A/D conversion is stopped (before a trigger occurs).

2. When the VCUT bit in ADCON1 register is changed from 0 (Vref not connected) to 1 (Vref connected), start A/D conversion after passing 1 µs or longer.

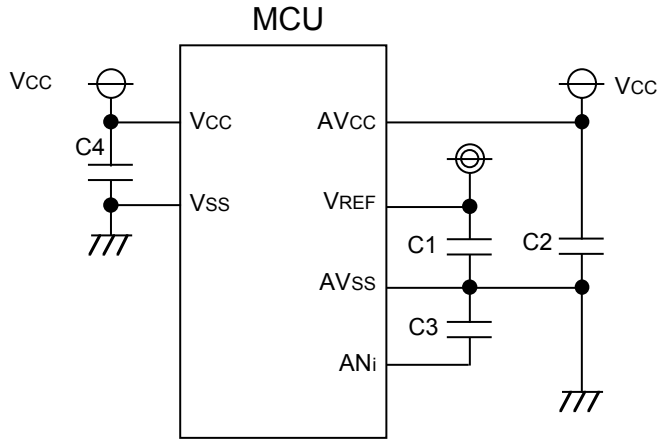
3. To prevent noise-induced device malfunction or latchup, as well as to reduce conversion errors, insert capacitors between the AVCC, VREF, and analog input pins (ANi, AN0i, AN2i(i=0 to 7), and AN3i(i=0 to 2)) each and the AVSS pin. Similarly, insert a capacitor between the VCC1 pin and the VSS pin. **Figure 22.4** is an example connection of each pin.

4. Make sure the port direction bits for those pins that are used as analog inputs are set to 0 (input mode). Also, if the TGR bit in the ADCON0 register is set to 1 (external trigger), make sure the port direction bit for the $\overline{\text{ADTRG}}$ pin is set to 0 (input mode).

5. When using key input interrupts, do not use any of the four AN4 to AN7 pins as analog inputs. (A key input interrupt request is generated when the A/D input voltage goes low.)

6. The ϕAD frequency must be 10 MHz or less. Without sample-and-hold function, limit the ϕAD frequency to 250kHz or more. With the sample and hold function, limit the ϕAD frequency to 1MHz or more.

7. When changing an A/D operation mode, select analog input pin again in bits CH2 to CH0 in the ADCON0 register and bits SCAN1 to SCAN0 in the ADCON1 register.



ANi: ANi, AN0i, AN2i (i=0 to 7), and AN3i (i=0 to 2)

NOTES:
1. C1 ≥ 0.47 µF, C2 ≥ 0.47 µF, C3 ≥ 100 pF, C4 ≥ 0.1 µF (reference)
2. Use thick and shortest possible wiring to connect capacitors.

Figure 22.4 Use of capacitors to reduce noise