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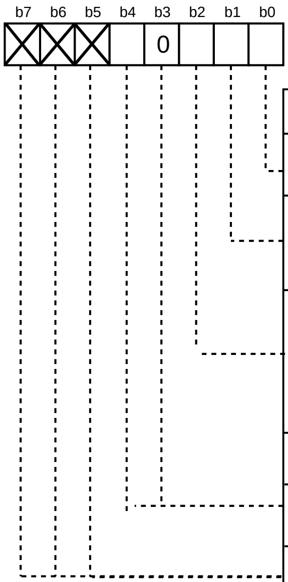
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	M16C/60
Core Size	16-Bit
Speed	20MHz
Connectivity	CANbus, I²C, IEBus, SIO, UART/USART
Peripherals	DMA, POR, PWM, Voltage Detect, WDT
Number of I/O	71
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 27x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30290fahp-u7a

Processeor Mode Register 2 [1]



Symbol: PM2 Address: $001E_{16}$ After Reset: $XXX00000_2$

Bit Symbol	Bit Name	Function	RW
PM20	Specifying wait when accessing SFR[2]	0: 2 waits 1: 1 wait	RW
PM21	System clock protective bit[3,4]	0: Clock is protected by PRCR register 1: Clock modification disabled	RW
PM22	WDT count source protective bit[3,5]	0: CPU clock is used for the watchdog timer count source 1: On-chip oscillator clock is used for the watchdog timer count source	RW
(b3)	Reserved bit	Set to 0	RW
PM24	$P8_5$/$\overline{NMI}$ configuration bit(6,7)	0: $P8_5$ function ($\overline{NMI}$ disabled) 1: $\overline{NMI}$ function	RW
(b7-b5)	Nothing is assigned. When write, set to 0. When read, thecontent is undefined		—

NOTES:
1. Write to this register after setting the PRC1 bit in the PRCR register to 1 (write enable).
2. The PM20 bit becomes effective when PLC07 bit in the PLC0 register is set to 1 (PLL on). Change the PM20 bit when the PLC07 bit is set to 0 (PLL off). Set the PM20 bit to 0 (2 waits) when PLL clock > 16MHz.
3. Once this bit is set to 1, it cannot be cleared to 0 by program.
4. Writting to the following bits has no effect when the PM21 bit is set to 1:
   - CM02 bit in the CM0 register
   - CM05 bit in the CM0 register (main clock is not halted)
   - CM07 bit in the CM0 register (CPU clock source does not change)
   - CM10 bit in the CM1 register (stop mode is not entered)
   - CM11 bit in the CM1 register (CPU clock source does not change)
   - CM20 bit in the CM2 register (oscillation stop, re-oscillation detection function settings do not change)
   - All bits in the PLC0 register (PLL frequency synthesizer setting do not change)

   Do not execute WAIT instruction when the PM21 bit is set to 1.
5. Setting the PM22 bit to 1 results in the following conditions:
   - The on-chip oscillator continues oscillating even if the CM21 bit in the CM2 register is set to "0" (main clock or PLL clock) (system clock of count source selected by the CM21 bit is valid)
   - The on-chip oscillator starts oscillating, and the on-chip oscillator clock becomes the watchdog timer count source.
   - The CM10 bit in the CM1 register cannnot be written. (Writing 1 has no effect, stop mode is not entered.)
   - The watchdog timer does not stop in wait mode.
6. For $\overline{NMI}$ function, the PM24 bit must be set to 1($\overline{NMI}$ function). Once this bit is set to 1, it cannot be set to 0 by program.
7. $\overline{SD}$ input is valid regardless of the PM24 setting.

Figure 6.2 PM2 Register

Rev.	Date	Description	
		Page	Summary
		122	“Figure 12.3.9 PFCR register and TPRC register” is deleted.
		125	Figure 12.3.1.2.1 and the section 12.3.1.2.4 are partly revised.
		126	Section “Three-phase/Port Output Switch Function” and “Figure 12.3.2.1 PFCR register and TPRC register” are added.
		166	“UART 2 special mode register 2” in Figure 14.1.8 is partly revised.
		167	“UART 2 special mode register 3” in Figure 14.1.9 is partly revised.
		210	Note 1 in Table 15.1.1.1 is deleted.
		213	Figure 15.4 is partly revised.
		214	Figure 15.5 is partly revised.
		219	Section “15.1.3 Single Sweep mode” is partly revised.
		221	Section “15.1.4 Repeat Sweep mode 0” is partly revised.
		223	Section “15.1.5 Repeat Sweep mode 1” is partly revised.
		225	Section “15.1.6 Simultaneous Sample Sweep Mode”, Table 15.1.6.1, and Figure 15.1.6.1 are partly revised.
		228	Section “15.1.7 Delayed Trigger Mode 0” and Table 15.1.7.1 are partly revised.
		229	Figure 15.1.7.1 is partly revised.
		230, 231	Figure 15.1.7.2 and 15.1.7.3 are partly revised.
		232	Figure 15.1.7.3 is deleted.
		235	Section “15.1.8 Delayed Trigger Mode 1” and Table 15.1.8.1 are partly revised.
		241	Figure 15.5.1 is partly revised.
		276 to 300	Chapter “17. CAN Module” is revised.
		301	Chapter “18. CRC Calculation Circuit” is partly revised.
		303	Figure 18.3 is partly revised.
		304	Chapter “19. Programmable I/O ports” is partly revised.
		305	Section “19.5 Pin Assignment Control Register” is partly revised.
		313	“Pull-up control register” in Figure 19.3.1 is partly revised.
		320	Table 20.4 and 20.5 and Note 6 and 10 are partly revised.
		321	Note 3 in Table 20.6 is added.
		342	Table 20.43 and 20.44 and Note 10 are partly revised.
		343	Note 3 in Table 20.45 is added.
		360 to 372	Section “20.3 V version” is deleted.
		373	Table 21.1 is partly revised.
		282	Section “•FMR01 Bit”, “•FMR02 Bit” and “•FMSTP Bit” are partly revised.
		383	Section “•FMR16 Bit”, “• FMR17 Bit” and “FMR41 Bit” are partly revised.
		384	Figure 21.5.1 is revised.
		387	Figure 21.5.1.3 is partly revised.
		392	Section “21.4.2 EW1 Mode” is partly revised.
			Section “21.6.4 How to Access” is partly revised.
			Section “21.7.5. Block Erase” is partly revised.