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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	M16C/60
Core Size	16-Bit
Speed	20MHz
Connectivity	CANbus, I²C, IEBus, SIO, UART/USART
Peripherals	DMA, POR, PWM, Voltage Detect, WDT
Number of I/O	71
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 27x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30290fahp-u9a

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

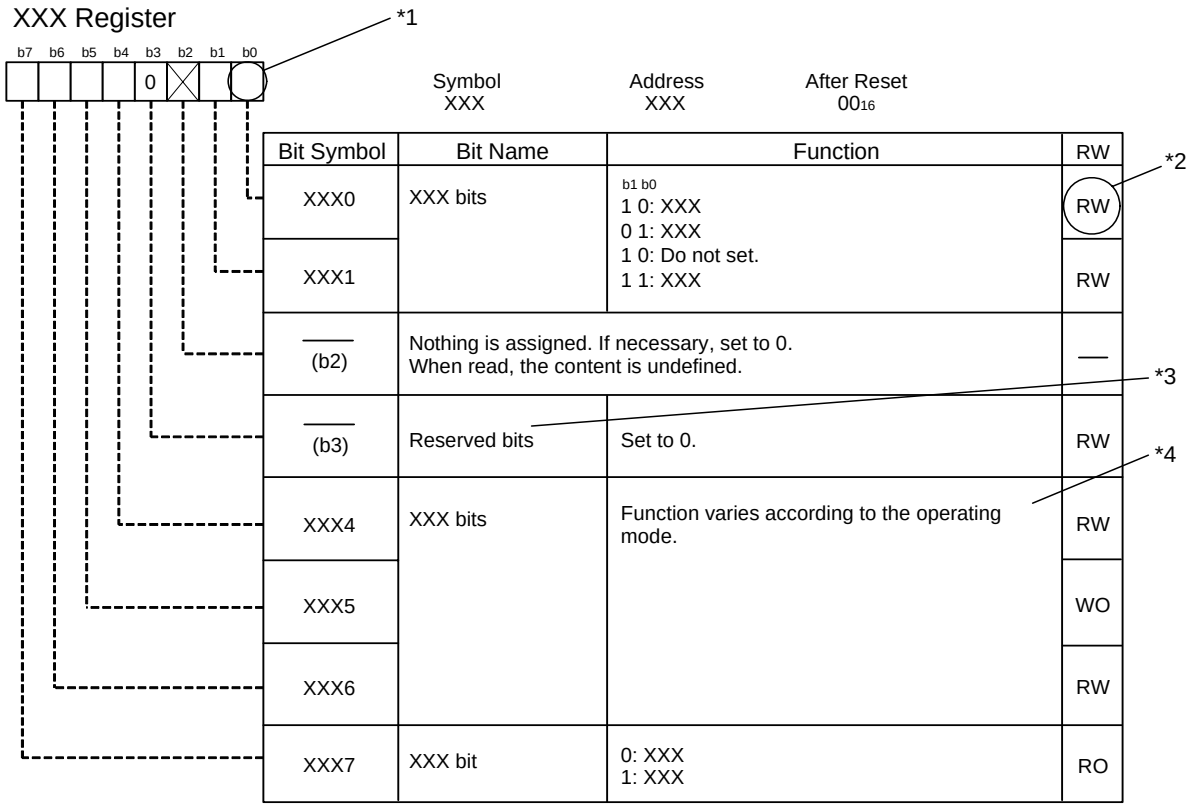
5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

3. Register Notation

The symbols and terms used in register diagrams are described below.



*1

Blank: Set to 0 or 1 according to the application.
0: Set to 0.
1: Set to 1.
X: Nothing is assigned.

*2

RW: Read and write.
RO: Read only.
WO: Write only.
–: Nothing is assigned.

*3

- Reserved bit
  Reserved bit. Set to specified value.

*4

- Nothing is assigned
  Nothing is assigned to the bit. As the bit may be used for future functions, if necessary, set to 0.
- Do not set to a value
  Operation is not guaranteed when a value is set.
- Function varies according to the operating mode.
  The function of the bit varies with the peripheral function mode. Refer to the register diagram for information on the individual modes.

Quick Reference to Pages Classified by Address

Address	Register	Symbol	Page
0100₁₆ 0101₁₆ 0102₁₆ 0103₁₆ 0104₁₆ 0105₁₆	CAN0 message box 10: Identifer/DLC		289
0106₁₆ 0107₁₆ 0108₁₆ 0109₁₆ 010A₁₆ 010B₁₆ 010C₁₆ 010D₁₆	CAN0 message box 10: Data field		289
010E₁₆ 010F₁₆	CAN0 message box 10: time stamp		289
0110₁₆ 0111₁₆ 0112₁₆ 0113₁₆ 0114₁₆ 0115₁₆	CAN0 message box 11: Identifier/DLC		289
0116₁₆ 0117₁₆ 0118₁₆ 0119₁₆ 011A₁₆ 011B₁₆ 011C₁₆ 011D₁₆	CAN0 message box 11: Data field		289
011E₁₆ 011F₁₆	CAN0 message box 11: time stamp		289
0120₁₆ 0121₁₆ 0122₁₆ 0123₁₆ 0124₁₆ 0125₁₆	CAN0 message box 12: Identifier/DLC		289
0126₁₆ 0127₁₆ 0128₁₆ 0129₁₆ 012A₁₆ 012B₁₆ 012C₁₆ 012D₁₆	CAN0 message box 12: Data field		289
012E₁₆ 012F₁₆	CAN0 message box 12: time stamp		289
0130₁₆ 0131₁₆ 0132₁₆ 0133₁₆ 0134₁₆ 0135₁₆	CAN0 message box 13: Identifier/DLC		289
0136₁₆ 0137₁₆ 0138₁₆ 0139₁₆ 013A₁₆ 013B₁₆ 013C₁₆ 013D₁₆	CAN0 message box 13: Data field		289
013E₁₆ 013F₁₆	CAN0 message box 13: time stamp		289

Address	Register	Symbol	Page
0140₁₆ 0141₁₆ 0142₁₆ 0143₁₆ 0144₁₆ 0145₁₆	CAN0 message box 14: Identifier/DLC		289
0146₁₆ 0147₁₆ 0148₁₆ 0149₁₆ 014A₁₆ 014B₁₆ 014C₁₆ 014D₁₆	CAN0 message box 14: Data field		289
014E₁₆ 014F₁₆	CAN0 message box 14: time stamp		289
0150₁₆ 0151₁₆ 0152₁₆ 0153₁₆ 0154₁₆ 0155₁₆	CAN0 message box 15: Identifier/DLC		289
0156₁₆ 0157₁₆ 0158₁₆ 0159₁₆ 015A₁₆ 015B₁₆ 015C₁₆ 015D₁₆	CAN0 message box 15: Data field		289
015E₁₆ 015F₁₆	CAN0 message box 15: time stamp		289
0160₁₆ 0161₁₆ 0162₁₆ 0163₁₆ 0164₁₆ 0165₁₆	CAN0 global mask register	C0GMR	291
0166₁₆ 0167₁₆ 0168₁₆ 0169₁₆ 016A₁₆ 016B₁₆	CAN0 local mask A register	C0LMAR	291
016C₁₆ 016D₁₆ 016E₁₆ 016F₁₆ 0170₁₆ 0171₁₆	CAN0 local mask B register	C0LMBR	291
0172₁₆			
0173₁₆			
0174₁₆			
0175₁₆			
0176₁₆			
0177₁₆			
0178₁₆			
0179₁₆			
017A₁₆			
017B₁₆			
017C₁₆			
017D₁₆			
017E₁₆			
017F₁₆			

Note: The blank areas are reserved and cannot be accessed by users.

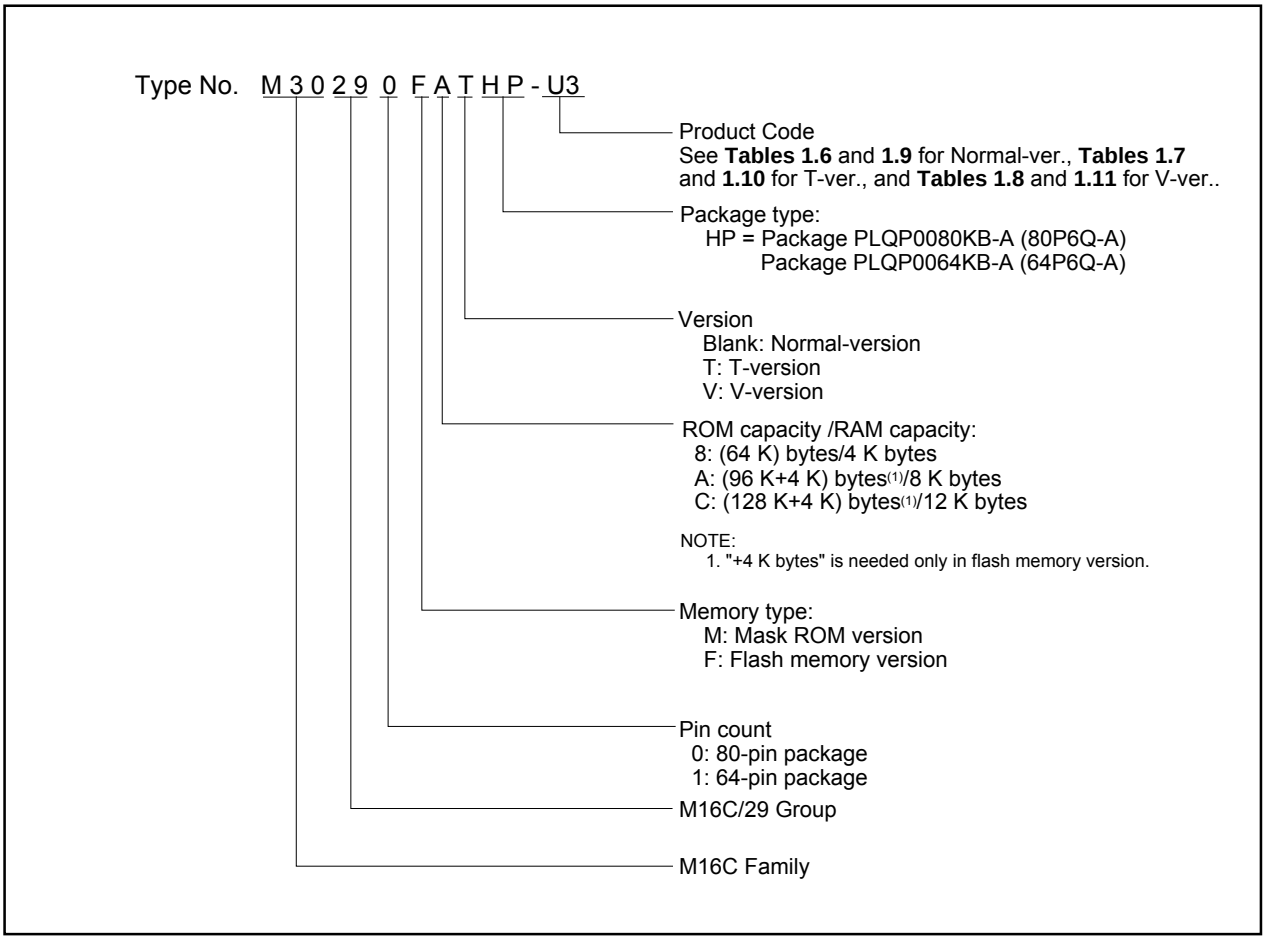


Figure 1.3 Type No., Memory Size, and Package

Table 1.6 Product Codes of Flash Memory Version -M16C/29 Group, Normal-ver.

Product Code	Package	Internal ROM (User Program Space: Blocks 0 to 5)		Internal ROM (Data Space: Blocks A and B)		Operating Ambient Temperature
		Program and Erase Endurance	Temperature Range	Program and Erase Endurance	Temperature Range	
U3	Lead-free	100	0 to 60°C	100	0 to 60°C	-40 to 85°C
U5						-20 to 85°C
U7		1,000		10,000	-40 to 85°C	-40 to 85°C
U9					-20 to 85°C	-20 to 85°C

Table 1.7 Product Codes of Flash Memory Version -M16C/29 Group, T-ver.

Product Code	Package	Internal ROM (User Program Space: Blocks 0 to 5)		Internal ROM (Data Space: Blocks A and B)		Operating Ambient Temperature
		Program and Erase Endurance	Temperature Range	Program and Erase Endurance	Temperature Range	
U3	Lead-free	100	0 to 60°C	100	-40 to 85°C	-40 to 85°C
U7		1,000		10,000		

Table 1.8 Product Codes of Flash Memory Version -M16C/29 Group, V-ver.

Product Code	Package	Internal ROM (User Program Space: Blocks 0 to 5)		Internal ROM (Data Space: Blocks A and B)		Operating Ambient Temperature
		Program and Erase Endurance	Temperature Range	Program and Erase Endurance	Temperature Range	
U3	Lead-free	100	0 to 60°C	100	-40 to 125°C	-40 to 125°C
U7		1,000		10,000		

Table 1.9 Product Codes of Mask ROM Version -M16C/29 Group, Normal-ver.

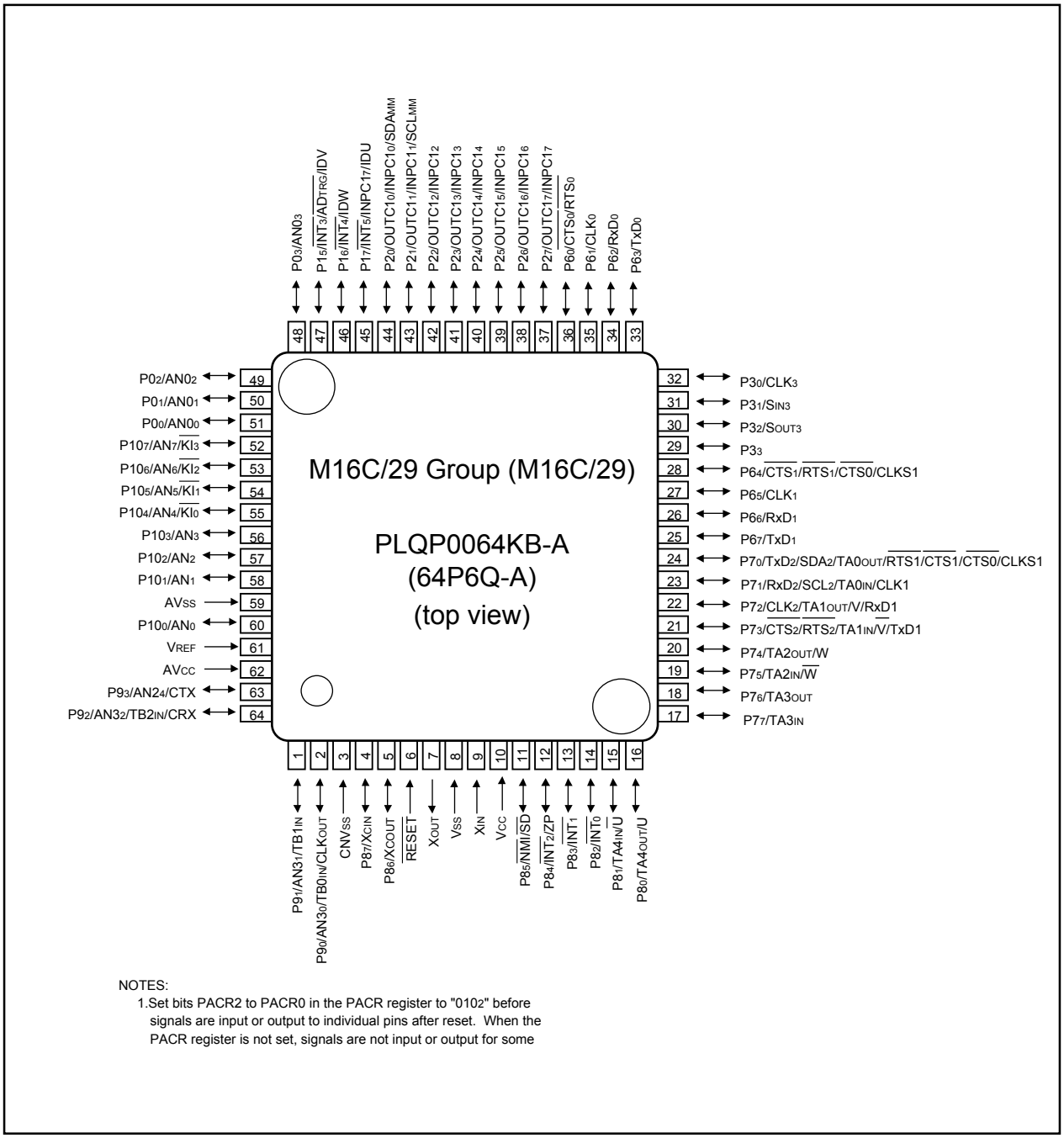
Product Code	Package	Operating Ambient Temperature
U3	Lead-free	-40 to 85°C
U5		-20 to 85°C

Table 1.10 Product Code of Mask ROM Version -M16C/29 Group, T-ver.

Product Code	Package	Operating Ambient Temperature
U0	Lead-free	-40 to 85°C

Table 1.11 Product Code of Mask ROM Version -M16C/29 Group, V-ver.

Product Code	Package	Operating Ambient Temperature
U0	Lead-free	-40 to 125°C



NOTES:
1.Set bits PACR2 to PACR0 in the PACR register to "010₂" before signals are input or output to individual pins after reset. When the PACR register is not set, signals are not input or output for some

Figure 1.9 Pin Assignment (Top View) of 64-Pin Package

Table 4.11 SFR Information (11)

Address	Register	Symbol	After reset
03C0₁₆	A/D register 0	AD0	XX₁₆
03C1₁₆			XX₁₆
03C2₁₆	A/D register 1	AD1	XX₁₆
03C3₁₆			XX₁₆
03C4₁₆	A/D register 2	AD2	XX₁₆
03C5₁₆			XX₁₆
03C6₁₆	A/D register 3	AD3	XX₁₆
03C7₁₆			XX₁₆
03C8₁₆	A/D register 4	AD4	XX₁₆
03C9₁₆			XX₁₆
03CA₁₆	A/D register 5	AD5	XX₁₆
03CB₁₆			XX₁₆
03CC₁₆	A/D register 6	AD6	XX₁₆
03CD₁₆			XX₁₆
03CE₁₆	A/D register 7	AD7	XX₁₆
03CF₁₆			XX₁₆
03D0₁₆			
03D1₁₆			
03D2₁₆	A/D trigger control register	ADTRGCON	XXXX0000₂
03D3₁₆	A/D status register 0	ADSTAT0	00000X00₂
03D4₁₆	A/D control register 2	ADCON2	00₁₆
03D5₁₆			
03D6₁₆	A/D control register 0	ADCON0	00000XXX₂
03D7₁₆	A/D control register 1	ADCON1	00₁₆
03D8₁₆			
03D9₁₆			
03DA₁₆			
03DB₁₆			
03DC₁₆			
03DD₁₆			
03DE₁₆			
03DF₁₆			
03E0₁₆	Port P0 register	P0	XX₁₆
03E1₁₆	Port P1 register	P1	XX₁₆
03E2₁₆	Port P0 direction register	PD0	00₁₆
03E3₁₆	Port P1 direction register	PD1	00₁₆
03E4₁₆	Port P2 register	P2	XX₁₆
03E5₁₆	Port P3 register	P3	XX₁₆
03E6₁₆	Port P2 direction register	PD2	00₁₆
03E7₁₆	Port P3 direction register	PD3	00₁₆
03E8₁₆			
03E9₁₆			
03EA₁₆			
03EB₁₆			
03EC₁₆	Port P6 register	P6	XX₁₆
03ED₁₆	Port P7 register	P7	XX₁₆
03EE₁₆	Port P6 direction register	PD6	00₁₆
03EF₁₆	Port P7 direction register	PD7	00₁₆
03F0₁₆	Port P8 register	P8	XX₁₆
03F1₁₆	Port P9 register	P9	XX₁₆
03F2₁₆	Port P8 direction register	PD8	00₁₆
03F3₁₆	Port P9 direction register	PD9	000X0000₂
03F4₁₆	Port P10 register	P10	XX₁₆
03F5₁₆			
03F6₁₆	Port P10 direction register	PD10	00₁₆
03F7₁₆			
03F8₁₆			
03F9₁₆			
03FA₁₆			
03FB₁₆			
03FC₁₆	Pull-up control register 0	PUR0	00₁₆
03FD₁₆	Pull-up control register 1	PUR1	00₁₆
03FE₁₆	Pull-up control register 2	PUR2	00₁₆
03FF₁₆	Port control register	PCR	00₁₆

Note 1: The blank areas are reserved and cannot be used by users.

X : Undefined

7.7 System Clock Protective Function

When the main clock is selected for the CPU clock source, this function protects the clock from modifications in order to prevent the CPU clock from becoming halted by run-away.

If the PM21 bit in the PM2 register is set to 1 (clock modification disabled), the following bits are protected against writes:

- Bits CM02, CM05, and CM07 in CM0 register
- Bits CM10 and CM11 in CM1 register
- CM20 bit in CM2 register
- All bits in the PLC0 register

Before the system clock protective function can be used, the following register settings must be made while the CM05 bit in the CM0 register is 0 (main clock oscillating) and CM07 bit is 0 (main clock selected for the CPU clock source):

(1) Set the PRC1 bit in the PRCR register to 1 (enable writes to PM2 register).

(2) Set the PM21 bit in the PM2 register to 1 (disable clock modification).

(3) Set the PRC1 bit in the PRCR register to 0 (disable writes to PM2 register).

Do not execute the WAIT instruction when the PM21 bit is 1.

7.8 Oscillation Stop and Re-oscillation Detect Function

The oscillation stop and re-oscillation detect function detects the re-oscillation after stop of main clock oscillation circuit. When the oscillation stop and re-oscillation detection occurs, the oscillation stop detect function is reset or oscillation stop and re-oscillation detection interrupt is generated, depending on the CM27 bit set in the CM2 register. The oscillation stop detect function is enabled or disabled by the CM20 bit in the CM2 register. **Table 7.8** lists a specification overview of the oscillation stop and re-oscillation detect function.

Table 7.8 Specification Overview of Oscillation Stop and Re-oscillation Detect Function

Item	Specification
Oscillation stop detectable clock and frequency bandwidth	$f(X_{IN}) \geq 2$ MHz
Enabling condition for oscillation stop, re-oscillation detection function	Set CM20 bit to 1(enable)
Operation at oscillation stop, re-oscillation detection	•Reset occurs (when CM27 bit =0) •Oscillation stop, re-oscillation detection interrupt occurs(when CM27 bit =1)

9.3.1 I Flag

The I flag enables or disables the maskable interrupt. Setting the I flag to 1 (= enabled) enables the maskable interrupt. Setting the I flag to 0 (= disabled) disables all maskable interrupts.

9.3.2 IR Bit

The IR bit is set to 1 (= interrupt requested) when an interrupt request is generated. Then, when the interrupt request is accepted and the CPU branches to the corresponding interrupt vector, the IR bit is cleared to 0 (= interrupt not requested).
The IR bit can be cleared to 0 in a program. Note that do not write 1 to this bit.

9.3.3 ILVL2 to ILVL0 Bits and IPL

Interrupt priority levels can be set using bits ILVL2 to ILVL0.
Table 9.3 shows the settings of interrupt priority levels and **Table 9.4** shows the interrupt priority levels enabled by the IPL.

The following are conditions under which an interrupt is accepted:
· I flag = 1
· IR bit = 1
· interrupt priority level > IPL

The I flag, IR bit, bits ILVL2 to ILVL0, and IPL are independent of each other. In no case do they affect one another.

Table 9.3 Settings of Interrupt Priority Levels

ILVL2 to ILVL0 bits	Interrupt priority level	Priority order
000_2	Level 0 (interrupt disabled)	———
001_2	Level 1	Low ↓
010_2	Level 2	
011_2	Level 3	
100_2	Level 4	
101_2	Level 5	
110_2	Level 6	
111_2	Level 7	High

Table 9.4 Interrupt Priority Levels Enabled by IPL

IPL	Enabled interrupt priority levels
000_2	Interrupt levels 1 and above are enabled
001_2	Interrupt levels 2 and above are enabled
010_2	Interrupt levels 3 and above are enabled
011_2	Interrupt levels 4 and above are enabled
100_2	Interrupt levels 5 and above are enabled
101_2	Interrupt levels 6 and above are enabled
110_2	Interrupt levels 7 and above are enabled
111_2	All maskable interrupts are disabled

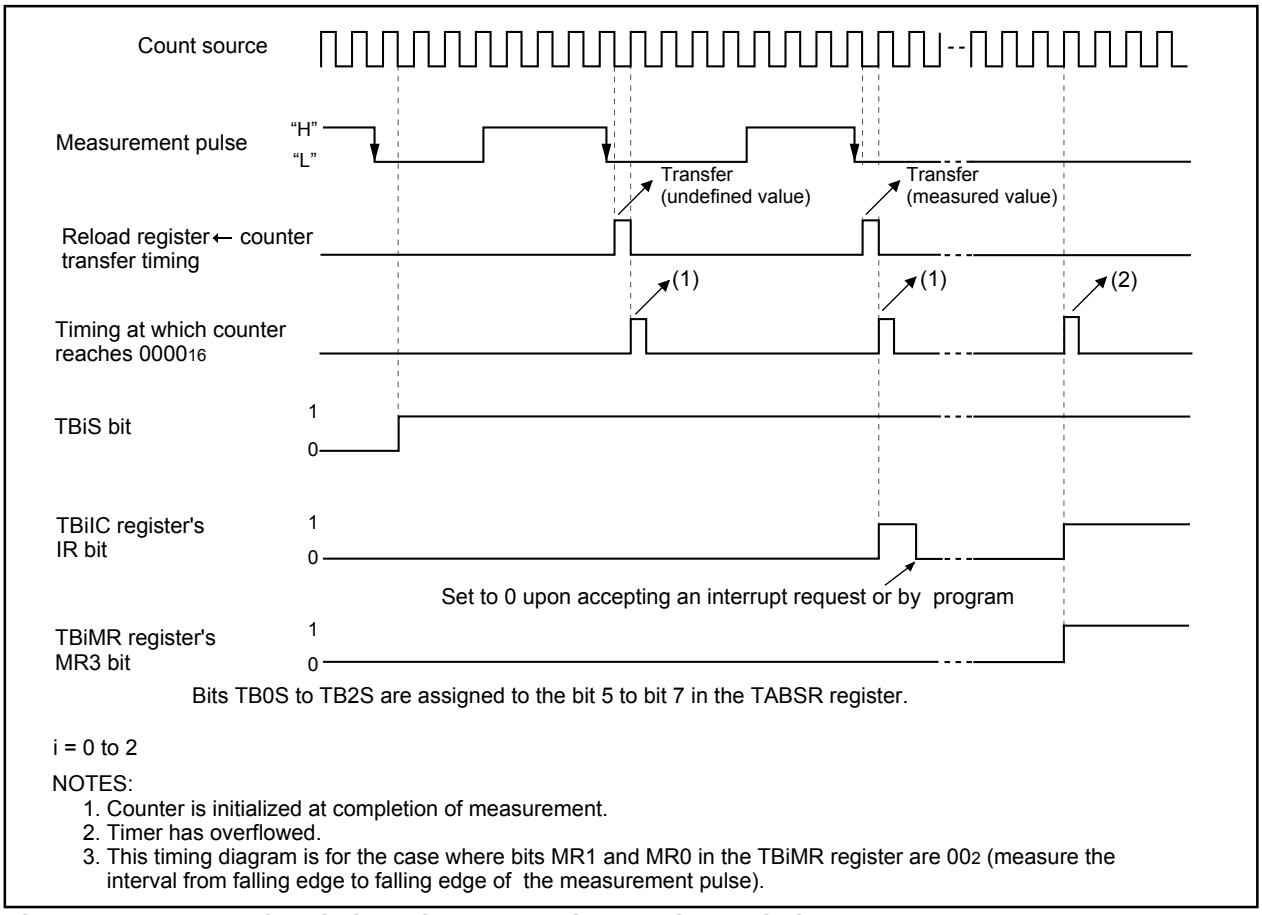


Figure 12.21 Operation timing when measuring a pulse period

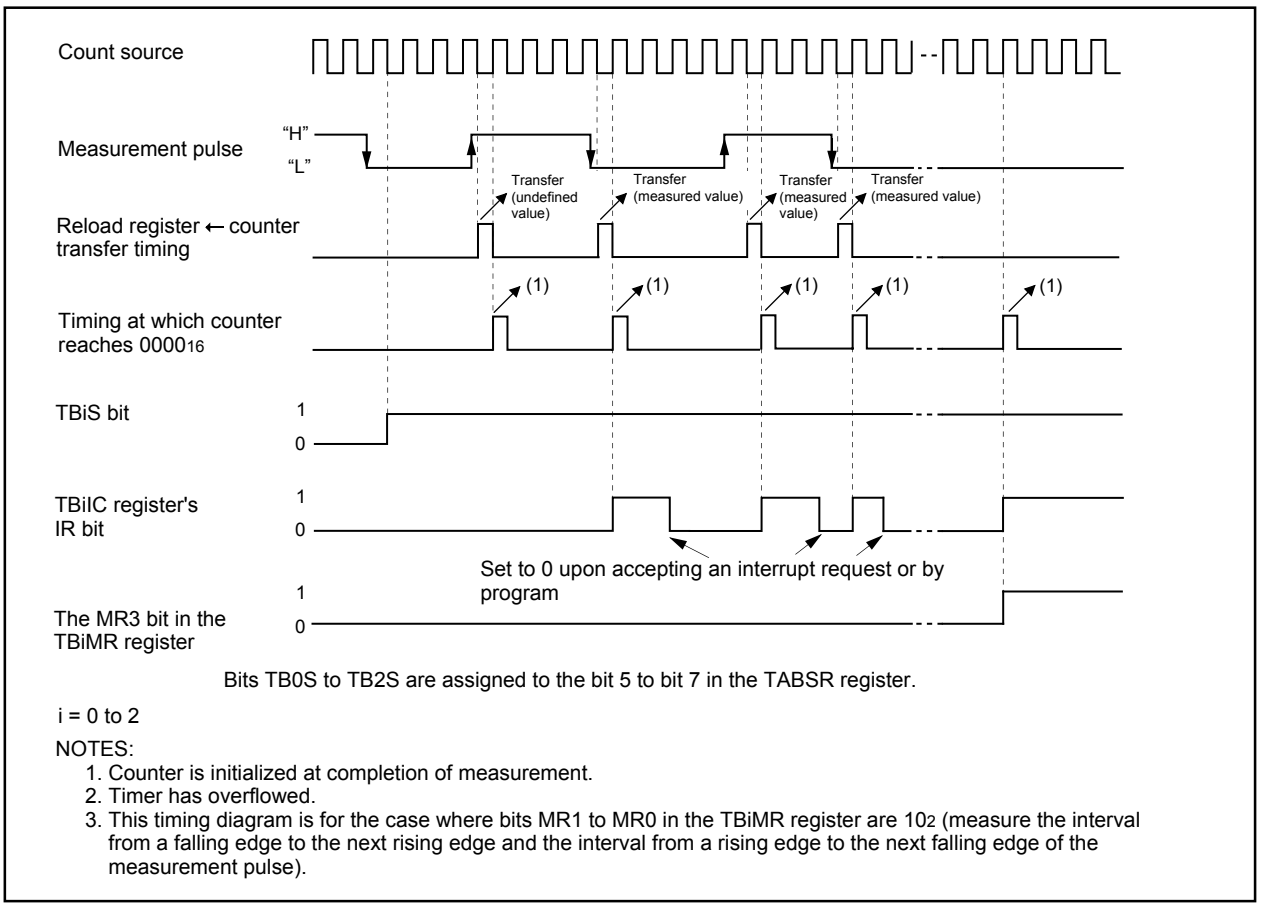
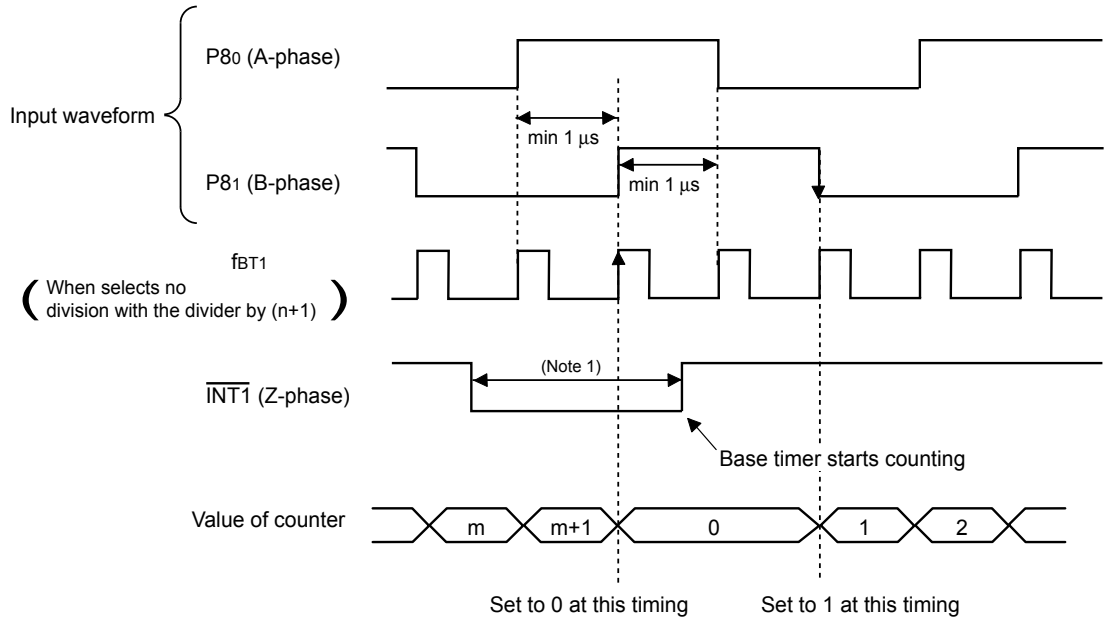
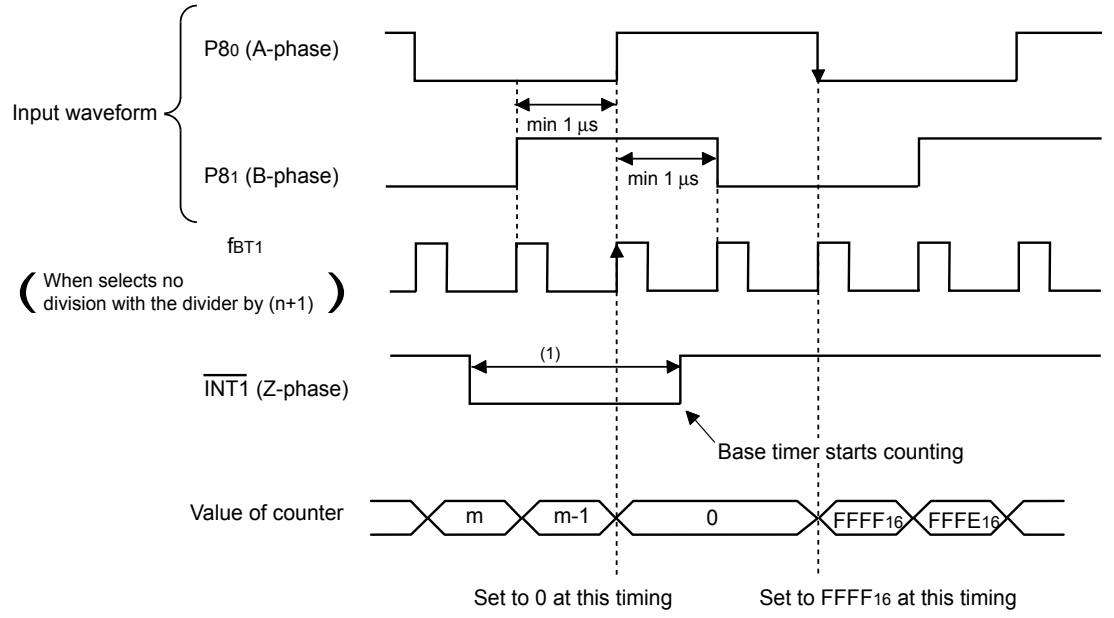


Figure 12.22 Operation timing when measuring a pulse width

(1) When the base timer is reset while the base timer increments the counter



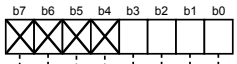
(2) When the base timer is reset while the base timer decrements the counter



NOTE:
1. 1.5 f_{BT1} clock cycle or more are required.

Figure 13.14 Base Timer Operation in Two-phase Pulse Signal Processing Mode

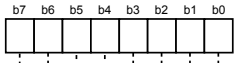
UARTi Transmit/receive Control Register 1 (i=0, 1)



Symbol: U0C1, U1C1 | Address: 03A5$_{16}$,03AD$_{16}$ | After Reset: 00000010$_2$

Bit Symbol	Bit Name	Function	RW
TE	Transmit enable bit	0 : Transmission disabled 1 : Transmission enabled	RW
TI	Transmit buffer empty flag	0 : Data present in UiTB register 1 : No data present in UiTB register	RO
RE	Receive enable bit	0 : Reception disabled 1 : Reception enabled	RW
RI	Receive complete flag	0 : No data present in UiRB register 1 : Data present in UiRB register	RO
— (b7-b4)	Nothing is assigned. If necessary, set to 0. When read, the content is 0		—

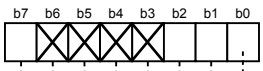
UART2 Transmit/receive Control Register 1



Symbol: U2C1 | Address: 037D$_{16}$ | After Reset: 00000010$_2$

Bit Symbol	Bit Name	Function	RW
TE	Transmit enable bit	0 : Transmission disabled 1 : Transmission enabled	RW
TI	Transmit buffer empty flag	0 : Data present in U2TB register 1 : No data present in U2TB register	RO
RE	Receive enable bit	0 : Reception disabled 1 : Reception enabled	RW
RI	Receive complete flag	0 : No data present in U2RB register 1 : Data present in U2RB register	RO
U2IRS	UART2 transmit interrupt cause select bit	0 : Transmit buffer empty (TI = 1) 1 : Transmit is completed (TXEPT = 1)	RW
U2RRM	UART2 continuous receive mode enable bit	0 : Continuous receive mode disabled 1 : Continuous receive mode enabled	RW
U2LCH	Data logic select bit	0 : No reverse 1 : Reverse	RW
U2ERE	Error signal output enable bit	0 : Output disabled 1 : Output enabled	RW

Pin Assignment Control Register (1)



Symbpl: PACR | Address: 025D$_{16}$ | After Reset: 00$_{16}$

Bit Symbol	Bit Name	Function	RW
PACR0	Pin enabling bit	010 : 64 pin 011 : 80 pin All other values are reserved. Do not use.	RW
PACR1			RW
PACR2			RW
— (b6-b3)	Reserved bits	Nothing is assigned. If necessary, set to 0. When read, the content is 0	—
U1MAP	UART1 pin remapping bit	UART1 pins assigned to 0 : P67 to P6$_4$ 1 : P7$_3$ to P7$_0$	RW

NOTE:
1. Set the PACR register by the next instruction after setting the PRC2 bit in the PRCR register to 1(write enable).

Figure 14.7 U0C1 to U2C1 Register, and PACR Register

17.10 Reception and Transmission

Configuration of CAN Reception and Transmission Mode

Table 17.3 shows configuration of CAN reception and transmission mode.

Table 17.3 Configuration of CAN Reception and Transmission Mode

TrmReq	RecReq	Remote	RspLock	Communication mode of the slot
0	0	–	–	Communication environment configuration mode: configure the communication mode of the slot.
0	1	0	0	Configured as a reception slot for a data frame.
1	0	1	0	Configured as a transmission slot for a remote frame. (At this time the RemActive = 1.) After completion of transmission, this functions as a reception slot for a data frame. (At this time the RemActive = 0.) However, when an ID that matches on the CAN bus is detected before remote frame transmission, this immediately functions as a reception slot for a data frame.
1	0	0	0	Configured as a transmission slot for a data frame.
0	1	1	1/0	Configured as a reception slot for a remote frame. (At this time the RemActive = 1.) After completion of reception, this functions as a transmission slot for a data frame. (At this time the RemActive = 0.) However, transmission does not start as long as RspLock bit remains 1; thus no automatic response. Response (transmission) starts when the RspLock bit is set to 0.

TrmReq, RecReq, Remote, RspLock, RemActive, RspLock: Bits in the C0MCTLj register (j = 0 to 15)

When configuring a slot as a reception slot, note the following points.

(1) Before configuring a slot as a reception slot, be sure to set the C0MCTLj register (j = 0 to 15) to 00_{16}.

(2) A received message is stored in a slot that matches the condition first according to the result of reception mode configuration and acceptance filtering operation. Upon deciding in which slot to store, the smaller the number of the slot is, the higher priority it has.

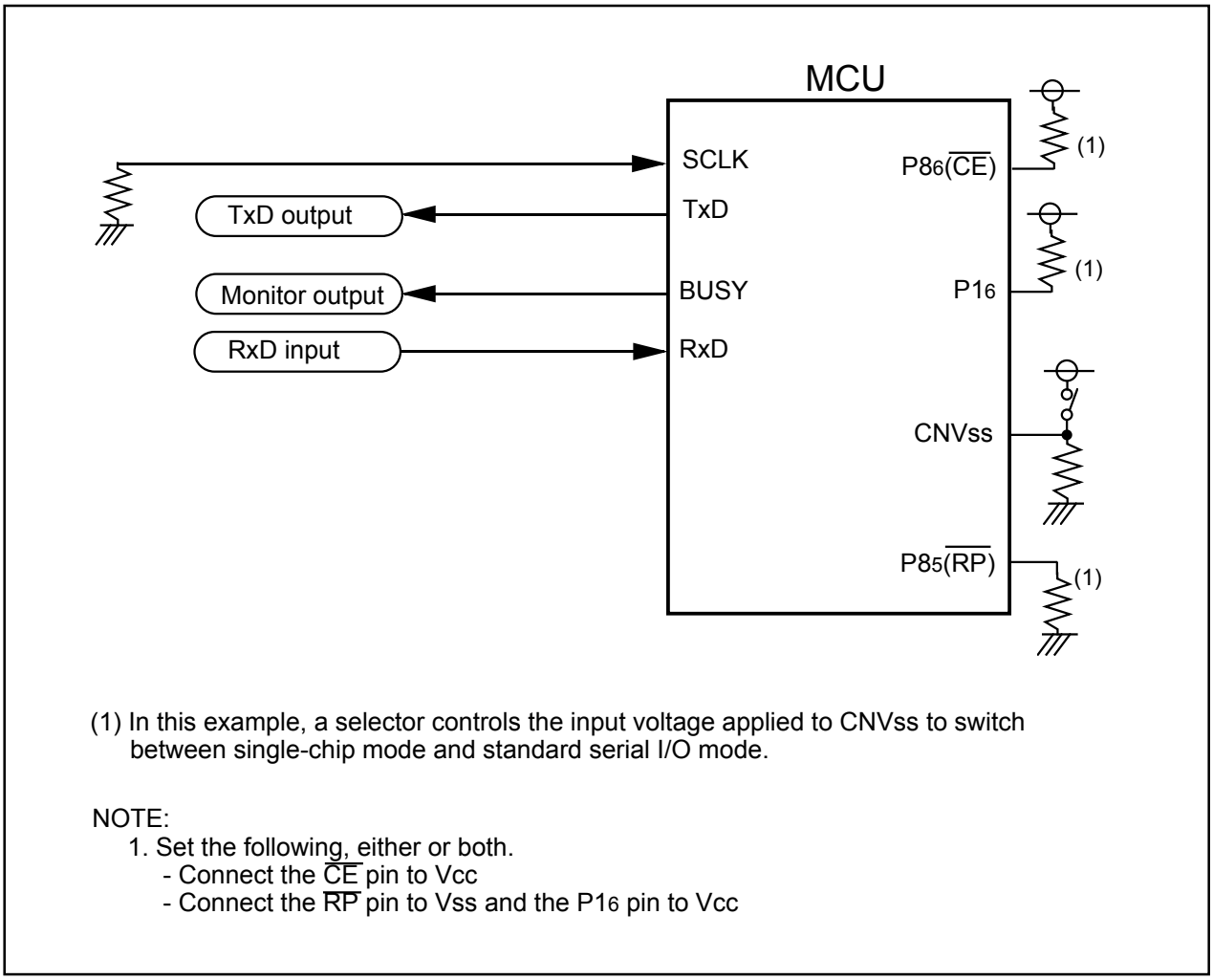
(3) In normal CAN operating mode, when a CAN module transmits a message of which ID matches, the CAN module never receives the transmitted data. In loop back mode, however, the CAN module receives back the transmitted data. In this case, the module does not return ACK.

When configuring a slot as a transmission slot, note the following points.

(1) Before configuring a slot as a transmission slot, be sure to set the C0MCTLj registers to 00_{16}.

(2) Set the TrmReq bit in the C0MCTLj register to 0 (not transmission slot) before rewriting a transmission slot.

(3) A transmission slot should not be rewritten when the TrmActive bit in the C0MCTLj register is 1 (transmitting).
If it is rewritten, an undefined data will be transmitted.



(1) In this example, a selector controls the input voltage applied to CNVss to switch between single-chip mode and standard serial I/O mode.

NOTE:
1. Set the following, either or both.
   - Connect the $\overline{CE}$ pin to Vcc
   - Connect the $\overline{RP}$ pin to Vss and the P16 pin to Vcc

Figure 20.18 Circuit Application in Standard Serial I/O Mode 2

Table 21.4 Flash Memory Version Electrical Characteristics (1) for 100/1000 E/W cycle products

[Program Space and Data Space in U3 and U5: Program Space in U7 and U9]

Symbol	Parameter		Standard			Unit
			Min.	Typ.(2)	Max.	
-	Program and Erase Endurance(3)		100/1000(4, 11)			cycles
-	Word Program Time (Vcc=5.0V, Topr=25° C)			75	600	µs
-	Block Erase Time (Vcc=5.0V, Topr=25° C)	2-Kbyte Block		0.2	9	s
		8-Kbyte Block		0.4	9	s
		16-Kbyte Block		0.7	9	s
		32-Kbyte Block		1.2	9	s
td(SR-ES)	Duration between Suspend Request and Erase Suspend				8	ms
tPS	Wait Time to Stabilize Flash Memory Circuit				15	µs
-	Data Hold Time (5)		20			years

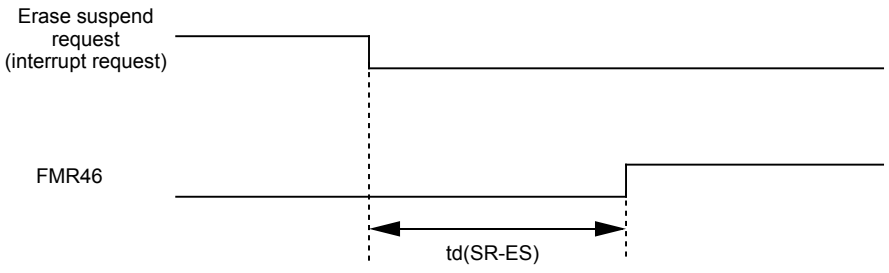
Table 21.5 Flash Memory Version Electrical Characteristics (6) 10000 E/W cycle products (Option)

[Data Space in U7 and U9(7)]

Symbol	Parameter	Standard			Unit
		Min.	Typ.(2)	Max.	
-	Program and Erase Endurance(3, 8, 9)	10000(4, 10)			cycles
-	Word Program Time (Vcc= 5.0 V, Topr = 25° C)		100		µs
-	Block Erase Time (Vcc= 5.0 V, Topr = 25° C) (2-Kbyte block)		0.3		s
td(SR-ES)	Duration between Suspend Request and Erase Suspend			8	ms
tPS	Wait Time to Stabilize Flash Memory Circuit			15	µs
-	Data Hold Time (5)	20			years

NOTES:

1. Referenced to Vcc= 2.7 to 5.5 V at Topr = 0 to 60° C (program space), unless otherwise specified.
2. Vcc= 5.0 V; Topr= 25° C
3. Program and erase endurance is defined as number of program-erase cycles per block.
   If program and erase endurance is *n* cycle (*n* = 100, 1000, 10000), each block can be erased and programmed *n* cycles.
   For example, if a 2-Kbyte block A is erased after programming one-word data to each address 1,024 times, this counts as one program and erase endurance. Data cannot be programmed to the same address more than once without erasing the block. (rewrite prohibited).
4. Number of E/W cycles for which operation is guranteed (1 to minimum value are guaranteed).
5. Topr= 55° C
6. Referenced to Vcc= 2.7 to 5.5 V at Topr= -40 to 85° C(U7) / -20 to 85° C (U9) unless otherwise specifie.
7. **Table 21.5** applies for data space in U7 and U9 when program and erase endurance is more than 1,000 cycles. Otherwise, use **Table 21.4**.
8. To reduce the number of program and erase endurance when working with systems requiring numerous rewrites, write to unused word addresses within the block instead of rewrite. Erase block only after all possible addresses are used. For example, an 8-word program can be written 128 times maximum before erase becomes necessary. Maintaining an equal number of times erasure between block A and block B will also improve efficiency. It is recommended to track the total number of erasure performed per block and to limit the number of erasure.
9. If an erase error is generated during block erase, execute the clear status register command and block erase command at least 3 times until an erase error is not generated.
10. When executing more than 100 times rewrites, set one wait state per block access by setting the FMR17 bit in the FMR1 register 1 to 1 (wait state). When accessing to all other blocks and internal RAM, wait state can be set by the PM17 bit, regardless of the FMR17 bit setting value.
11. The program and erase endurance is 100 cycles for program space and data space in U3 and U5; 1,000 cycles for program space in U7 and U9.
12. Please contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor for further details on the E/W failure rate.



VCC = 3V

Timing Requirements

(VCC = 3V, VSS = 0V, at Topr = – 20 to 85°C / – 40 to 85°C unless otherwise specified)

Table 21.27 Timer A Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	150		ns
$t_{w(TAH)}$	TAiIN input HIGH pulse width	60		ns
$t_{w(TAL)}$	TAiIN input LOW pulse width	60		ns

Table 21.28 Timer A Input (Gating Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	600		ns
$t_{w(TAH)}$	TAiIN input HIGH pulse width	300		ns
$t_{w(TAL)}$	TAiIN input LOW pulse width	300		ns

Table 21.29 Timer A Input (External Trigger Input in One-shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	300		ns
$t_{w(TAH)}$	TAiIN input HIGH pulse width	150		ns
$t_{w(TAL)}$	TAiIN input LOW pulse width	150		ns

Table 21.30 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAiIN input HIGH pulse width	150		ns
$t_{w(TAL)}$	TAiIN input LOW pulse width	150		ns

Table 21.31 Timer A Input (Counter Increment/decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(UP)}$	TAiOUT input cycle time	3000		ns
$t_{w(UPH)}$	TAiOUT input HIGH pulse width	1500		ns
$t_{w(UPL)}$	TAiOUT input LOW pulse width	1500		ns
$t_{su(UP-TIN)}$	TAiOUT input setup time	600		ns
$t_{h(TIN-UP)}$	TAiOUT input hold time	600		ns

Table 21.32 Timer A Input (Two-phase Pulse Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	2		µs
$t_{su(TAIN-TAOUT)}$	TAiOUT input setup time	500		ns
$t_{su(TAOUT-TAIN)}$	TAiIN input setup time	500		ns

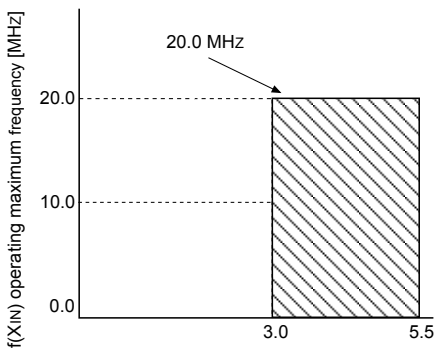
Table 21.41 Recommended Operating Conditions (Note 1)

Symbol	Parameter			Standard			Unit
				Min.	Typ.	Max.	
V_{CC}	Supply Voltage			3.0		5.5	V
AV_{CC}	Analog Supply Voltage				V_{CC}		V
V_{SS}	Supply Voltage				0		V
AV_{SS}	Analog Supply Voltage				0		V
V_{IH}	Input High ("H") Voltage	$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_7$, $P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_7$, $P9_0$ to $P9_3$, $P9_5$ to $P9_7$, $P10_0$ to $P10_7$		0.7V_{CC}		V_{CC}	V
		XIN, $\overline{RESET}$, CNVSS		0.8V_{CC}		V_{CC}	V
		SDA_{MM}, SCL_{MM}	When I^2C bus input level is selected	0.7V_{CC}		V_{CC}	V
			When SMBUS input level is selected	1.4		V_{CC}	V
V_{IL}	Input Low ("L") Voltage	$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_7$, $P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_7$, $P9_0$ to $P9_3$, $P9_5$ to $P9_7$, $P10_0$ to $P10_7$		0		0.3V_{CC}	V
		XIN, $\overline{RESET}$, CNVSS		0		0.2V_{CC}	V
		SDA_{MM}, SCL_{MM}	When I^2C bus input level is selected	0		0.3V_{CC}	V
			When SMBUS input level is selected	0		0.6	V
$I_{OH(peak)}$	Peak Output High ("H") Current	$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_7$, $P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_7$, $P9_0$ to $P9_3$, $P9_5$ to $P9_7$, $P10_0$ to $P10_7$				-10.0	mA
$I_{OH(avg)}$	Average Output High ("H") Current	$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_7$, $P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_7$, $P9_0$ to $P9_3$, $P9_5$ to $P9_7$, $P10_0$ to $P10_7$				-5.0	mA
$I_{OL(peak)}$	Peak Output Low ("L") Current	$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_7$, $P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_7$, $P9_0$ to $P9_3$, $P9_5$ to $P9_7$, $P10_0$ to $P10_7$				10.0	mA
$I_{OL(avg)}$	Average Output Low ("L") Current	$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_7$, $P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_7$, $P9_0$ to $P9_3$, $P9_5$ to $P9_7$, $P10_0$ to $P10_7$				5.0	mA
f(X_{IN})	Main Clock Input Oscillation Frequency(4)			0		20	MHz
f(X_{CIN})	Sub Clock Oscillation Frequency				32.768	50	kHz
f_1(ROC)	On-chip Oscillator Frequency 1			0.5	1	2	MHz
f2(ROC)	On-chip Oscillator Frequency 2			1	2	4	MHz
f3(ROC)	On-chip Oscillator Frequency 3			8	16	26	MHz
f(PLL)	PLL Clock Oscillation Frequency(4)			10		20	MHz
f(BCLK)	CPU Operation Clock Frequency			0		20	MHz
t_{SU}(PLL)	Wait Time to Stabilize PLL Frequency Synthesizer		V_{CC}=5.0V			20	ms
			V_{CC}=3.0V			50	ms

NOTES:

1. Referenced to V_{CC} = 3.0 to 5.5V at Topr = -40 to 85 ° C unless otherwise specified.
2. The mean output current is the mean value within 100ms.
3. The total $I_{OL(peak)}$ for all ports must be 80mA or less. The total $I_{OH(peak)}$ for all ports must be -80mA or less.
4. Relationship among main clock oscillation frequency, PLL clock oscillation frequency and supply voltage.

Main clock input oscillation frequency



PLL clock oscillation frequency

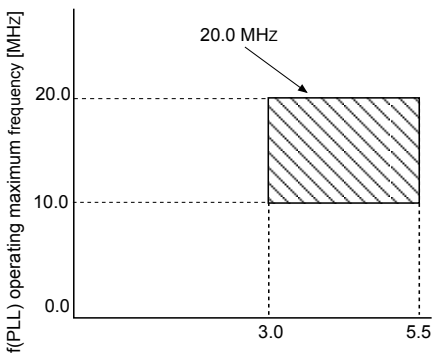


Table 21.43 Flash Memory Version Electrical Characteristics (1) for 100/1000 E/W cycle products

[Program Space and Data Space in U3; Program Space in U7]

Symbol	Parameter		Standard			Unit
			Min.	Typ.(2)	Max.	
-	Program and Erase Endurance(3)		100/1000(4, 11)			cycles
-	Word Program Time (Vcc = 5.0 V, Topr = 25° C)			75	600	µs
-	Block Erase Time (Vcc = 5.0 V, Topr = 25° C)	2-Kbyte Block		0.2	9	s
		8-Kbyte Block		0.4	9	s
		16-Kbyte Block		0.7	9	s
		32-Kbyte Block		1.2	9	s
td(SR-ES)	Duration between Suspend Request and Erase Suspend				8	ms
tPS	Wait Time to Stabilize Flash Memory Circuit				15	µs
-	Data Hold Time (5)		20			years

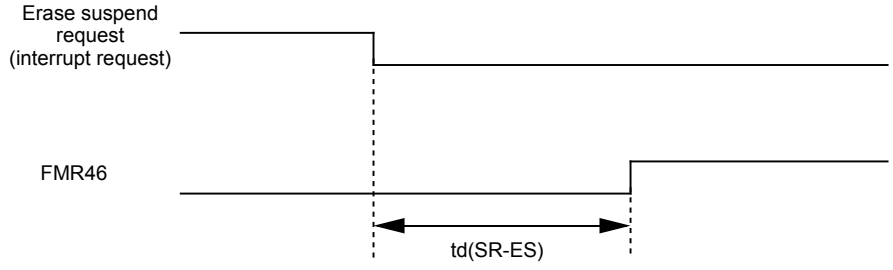
Table 21.44 Flash Memory Version Electrical Characteristics (6) for 10000 E/W cycle products

[Data Space in U7(7)]

Symbol	Parameter	Standard			Unit
		Min.	Typ.(2)	Max.	
-	Program and Erase Endurance(3, 8, 9)	10000(4, 10)			cycles
-	Word Program Time (Vcc = 5.0 V, Topr = 25° C)		100		µs
-	Block Erase Time (Vcc = 5.0V, Topr = 25° C) (2-Kbyte block)		0.3		s
td(SR-ES)	Duration between Suspend Request and Erase Suspend			8	ms
tPS	Wait Time to Stabilize Flash Memory Circuit			15	µs
-	Data Hold Time (5)	20			years

NOTES:

1. Referenced to VCC = 3.0 to 5.5 V at Topr = 0 to 60° C (program space)/ Topr = -40 to 85° C(data space), unless otherwise specified.
2. VCC = 5.0 V; TOPR = 25° C
3. Program and erase endurance is defined as number of program-erase cycles per block.
   If program and erase endurance is *n* cycle (*n* = 100, 1000, 10000), each block can be erased and programmed *n* cycles.
   For example, if a 2-Kbyte block A is erased after programming one-word data to each address 1,024 times, this counts as one program and erase endurance. Data cannot be programmed to the same address more than once without erasing the block. (rewrite prohibited).
4. Number of E/W cycles for which operation is guranteed (1 to minimum value are guranteed).
5. Topr = 55° C
6. Referenced to VCC = 3.0 to 5.5 V at Topr = -40 to 85° C unless otherwise specified.
7. **Table 21.44** applies for data space in U7 when program and erase endurance is more than 1,000 cycles. Otherwise, use **Table 21.43**.
8. To reduce the number of program and erase endurance when working with systems requiring numerous rewrites, write to unused word addresses within the block instead of rewrite. Erase block only after all possible addresses are used. For example, an 8-word program can be written 128 times maximum before erase becomes necessary. Maintaining an equal number of times erasure between block A and block B will also improve efficiency. It is recommended to track the total number of erasure performed per block and to limit the number of erasure.
9. If an erase error is generated during block erase, execute the clear status register command and block erase command at least 3 times until an erase error is not generated.
10. When executing more than 100 times rewrites, set one wait state per block access by setting the FMR17 bit in the FMR1 register to 1 (wait state). When accessing to all other blocks and internal RAM, wait state can be set by the PM17 bit, regardless of the FMR17 bit setting value.
11. The program and erase endurance is 100 cycles for program space and data space in U3; 1,000 cycles for program space in U7.
12. Please contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor for further details on the E/W failure rate.



M16C/29 Group
Hardware Manual

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