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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	M16C/60
Core Size	16-Bit
Speed	20MHz
Connectivity	CANbus, I²C, IEBus, SIO, UART/USART
Peripherals	DMA, POR, PWM, Voltage Detect, WDT
Number of I/O	71
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 27x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30290fchp-u7a

Table 4.4 SFR Information (4)

Address	Register	Symbol	After reset
00C0₁₆	CAN0 message box 6: Identifier/DLC		XX₁₆
00C1₁₆			XX₁₆
00C2₁₆			XX₁₆
00C3₁₆			XX₁₆
00C4₁₆			XX₁₆
00C5₁₆			XX₁₆
00C6₁₆	CAN0 message box 6 : Data field		XX₁₆
00C7₁₆			XX₁₆
00C8₁₆			XX₁₆
00C9₁₆			XX₁₆
00CA₁₆			XX₁₆
00CB₁₆			XX₁₆
00CC₁₆			XX₁₆
00CD₁₆			XX₁₆
00CE₁₆	CAN0 message box 6 : Time stamp		XX₁₆
00CF₁₆			XX₁₆
00D0₁₆	CAN0 message box 7 : Identifier/DLC		XX₁₆
00D1₁₆			XX₁₆
00D2₁₆			XX₁₆
00D3₁₆			XX₁₆
00D4₁₆			XX₁₆
00D5₁₆			XX₁₆
00D6₁₆	CAN0 message box 7 : Data field		XX₁₆
00D7₁₆			XX₁₆
00D8₁₆			XX₁₆
00D9₁₆			XX₁₆
00DA₁₆			XX₁₆
00DB₁₆			XX₁₆
00DC₁₆			XX₁₆
00DD₁₆			XX₁₆
00DE₁₆	CAN0 message box 7 : Time stamp		XX₁₆
00DF₁₆			XX₁₆
00E0₁₆	CAN0 message box 8: Identifier/DLC		XX₁₆
00E1₁₆			XX₁₆
00E2₁₆			XX₁₆
00E3₁₆			XX₁₆
00E4₁₆			XX₁₆
00E5₁₆			XX₁₆
00E6₁₆	CAN0 message box 8: Data field		XX₁₆
00E7₁₆			XX₁₆
00E8₁₆			XX₁₆
00E9₁₆			XX₁₆
00EA₁₆			XX₁₆
00EB₁₆			XX₁₆
00EC₁₆			XX₁₆
00ED₁₆			XX₁₆
00EE₁₆	CAN0 message box 8 : Time stamp		XX₁₆
00EF₁₆			XX₁₆
00F0₁₆	CAN0 message box 9 : Identifier/DLC		XX₁₆
00F1₁₆			XX₁₆
00F2₁₆			XX₁₆
00F3₁₆			XX₁₆
00F4₁₆			XX₁₆
00F5₁₆			XX₁₆
00F6₁₆	CAN0 message box 9 : Data field		XX₁₆
00F7₁₆			XX₁₆
00F8₁₆			XX₁₆
00F9₁₆			XX₁₆
00FA₁₆			XX₁₆
00FB₁₆			XX₁₆
00FC₁₆			XX₁₆
00FD₁₆			XX₁₆
00FE₁₆	CAN0 message box 9 : Time stamp		XX₁₆
00FF₁₆			XX₁₆

Note 1: The blank areas are reserved and cannot be used by users.

X : Undefined

5.5.2. Limitations on Stop Mode

When all the conditions below are met, the low voltage detection interrupt is generated and the MCU exits stop mode as soon as the CM10 bit in the CM1 register is set to 1 (all clocks stopped).

- the VC27 bit in the VCR2 register is set to 1 (low voltage detection circuit enabled)
- the D40 bit in the D4INT register is set to 1 (low voltage detection interrupt enabled)
- the D41 bit in the D4INT register is set to 1 (low voltage detection interrupt is used to exit stop mode)
- the voltage applied to the Vcc pin is higher than Vdet4 (the VC13 bit in the VCR1 register is 1)

Set the CM10 bit to 1 when the VC13 bit is set to set to 0 (Vcc < Vdet4), if the MCU is configured to enter stop mode when voltage applied to the Vcc pin drops Vdet4 or below and to exit stop mode when the voltage applied rises to Vdet4 or above.

5.5.3. Limitations on WAIT Instruction

When all the conditions below are met, the low voltage detection interrupt is generated and the MCU exits wait mode as soon as WAIT instruction is executed.

- the CM02 bit in the CM0 register is set to 1 (stop peripheral function clock)
- the VC27 bit in the VCR2 register is set to 1 (low voltage detection circuit enabled)
- the D40 bit in the D4INT register is set to 1 (low voltage detection interrupt enabled)
- the D41 bit in the D4INT register is set to 1 (low voltage detection interrupt is used to exit wait mode)
- the voltage applied to the Vcc pin is higher than Vdet4 (the VC13 bit in the VCR1 register is 1)

Execute the WAIT instruction when the VC13 bit is set to set to 0 (Vcc < Vdet4), if the MCU is configured to enter wait mode when voltage applied to the Vcc pin drops Vdet4 or below and to exit wait mode when the voltage applied rises to Vdet4 or above.

The following describes the clocks generated by the clock generation circuit.

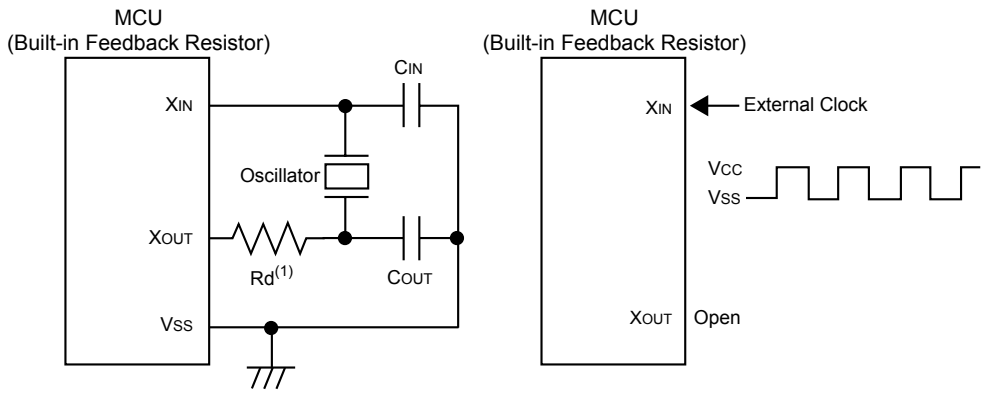
7.1 Main Clock

The main clock is generated by the main clock oscillation circuit. This clock is used as the clock source for the CPU and peripheral function clocks. The main clock oscillator circuit is configured by connecting a resonator between the XIN and XOUT pins. The main clock oscillator circuit contains a feedback resistor, which is disconnected from the oscillator circuit during stop mode in order to reduce the amount of power consumed in the chip. The main clock oscillator circuit may also be configured by feeding an exter nally generated clock to the XIN pin. **Figure 7.8** shows the examples of main clock connection circuit.

The power consumption in the chip can be reduced by setting the CM05 bit in the CM0 register to 1 (main clock oscillator circuit turned off) after switching the clock source for the CPU clock to a sub clock or on-chip oscillator clock. In this case, XOUT goes “H”. Furthermore, because the internal feedback resistor remains on, XIN is pulled “H” to XOUT via the feedback resistor.

During stop mode, all clocks including the main clock are turned off. Refer to “power control”.

If the main clock is not used, it is recommended to connect the XIN pin to VCC to reduce power consumption during reset.



NOTE:
1. Insert a damping resistor if required. Resistance value varies depending on the oscillator setting. Use resistance value recommended by the oscillator manufacturer. If the oscillator manufacturer recommends that a feedback resistor be added to the chip externally, insert a feedback resistor between XIN and XOUT.
2. The external clock should not be stopped when it is connected to the XIN pin and the main clock is selected as the CPU clock.

Figure 7.8 Examples of Main Clock Connection Circuit

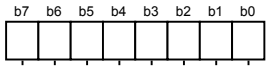
One-shot Start Flag

Symbol	Address	After Reset
ONSF	038216	0016

Bit Symbol	Bit Name	Function	RW
TA0OS	Timer A0 one-shot start flag	The timer starts counting by setting this bit to 1 while bits TMOD1 and TMOD0 in the TAiMR register (i = 0 to 4) = 102 (= one-shot timer mode) and the MR2 bit in the TAiMR register = 0 (=TAiOS bit enabled). When read, its content is 0	RW
TA1OS	Timer A1 one-shot start flag		RW
TA2OS	Timer A2 one-shot start flag		RW
TA3OS	Timer A3 one-shot start flag		RW
TA4OS	Timer A4 one-shot start flag		RW
TAZIE	Z-phase input enable bit	0: Z-phase input disabled 1: Z-phase input enabled	RW
TA0TGL	Timer A0 event/trigger select bit	b7 b6 0 0: Input on TA0IN is selected (1) 0 1: TB2 overflow is selected (2) 1 0: TA4 overflow is selected (2) 1 1: TA1 overflow is selected (2)	RW
TA0TGH			RW

NOTES:
1. Make sure the PD7_1 bit in the PD7 register is set to 0 (input mode).
2. Overflow or underflow.

Trigger Select Register

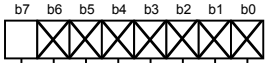


Symbol	Address	After Reset
TRGSR	038316	0016

Bit Symbol	Bit Name	Function	RW
TA1TGL	Timer A1 event/trigger select bit	b1 b0 0 0: Input on TA1IN is selected (1) 0 1: TB2 is selected (2) 1 0: TA0 is selected (2) 1 1: TA2 is selected (2)	RW
TA1TGH			RW
TA2TGL	Timer A2 event/trigger select bit	b3 b2 0 0: Input on TA2IN is selected (1) 0 1: TB2 is selected (2) 1 0: TA1 is selected (2) 1 1: TA3 is selected (2)	RW
TA2TGH			RW
TA3TGL	Timer A3 event/trigger select bit	b5 b4 0 0: Input on TA3IN is selected (1) 0 1: TB2 is selected (2) 1 0: TA2 is selected (2) 1 1: TA4 is selected (2)	RW
TA3TGH			RW
TA4TGL	Timer A4 event/trigger select bit	b7 b6 0 0: Input on TA4IN is selected (1) 0 1: TB2 is selected (2) 1 0: TA3 is selected (2) 1 1: TA0 is selected (2)	RW
TA4TGH			RW

NOTES:
1. Make sure the port direction bits for the TA1IN to TA4IN pins are set to 0 (input mode).
2. Overflow or underflow.

Clock Prescaler Reset Flag



Symbol	Address	After Reset
CPSRF	038116	0XXXXXXX2

Bit Symbol	Bit Name	Function	RW
—— (b6-b0)	Nothing is assigned. If necessary, set to 0. When read, their contents are undefined		—
CPSR	Clock prescaler reset flag	Setting this bit to 1 initializes the prescaler for the timekeeping clock. (When read, its content is 0)	RW

Figure 12.6 ONSF Register, TRGSR Register, and CPSRF Register

12.1.2.1 Counter Initialization by Two-Phase Pulse Signal Processing

This function initializes the timer count value to 0 by Z-phase (counter initialization) input during two-phase pulse signal processing.

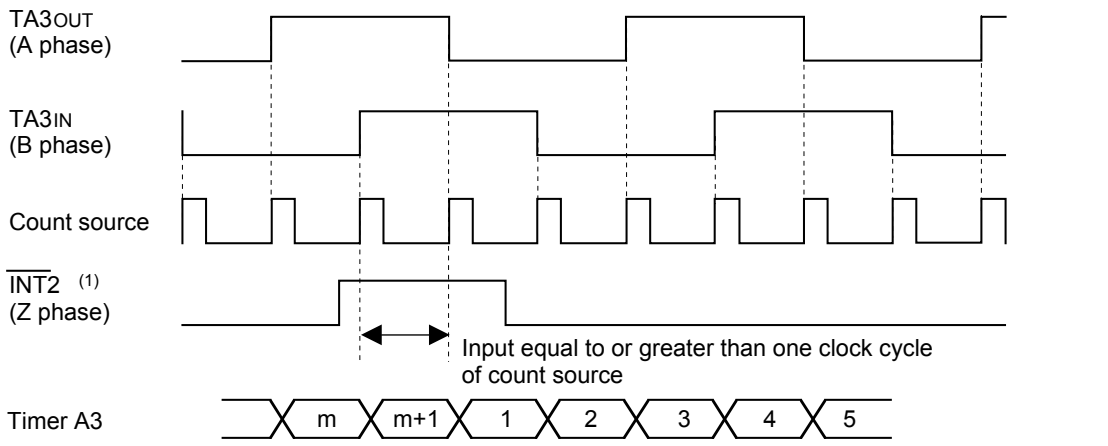
This function can only be used in timer A3 event counter mode during two-phase pulse signal processing, free-running type, x4 processing, with Z-phase entered from the $\overline{INT2}$ pin.

Counter initialization by Z-phase input is enabled by writing 0000_{16} to the TA3 register and setting the TAZIE bit in ONSF register to 1 (Z-phase input enabled).

Counter initialization is accomplished by detecting Z-phase input edge. The active edge can be chosen to be the rising or falling edge by using the POL bit in the INT2IC register. The Z-phase pulse width applied to the $\overline{INT2}$ pin must be equal to or greater than one clock cycle of the timer A3 count source.

The counter is initialized at the next count timing after recognizing Z-phase input. **Figure 12.10** shows the relationship between the two-phase pulse (A phase and B phase) and the Z phase.

If timer A3 overflow or underflow coincides with the counter initialization by Z-phase input, a timer A3 interrupt request is generated twice in succession. Do not use the timer A3 interrupt when using this function.



NOTE:
1. This timing diagram is for the case where the POL bit in the INT2IC register is set to 1 (rising edge).

Figure 12.10 Two-phase Pulse (A phase and B phase) and the Z Phase

13.2 Interrupt Operation

The IC/OC interrupt contains several request causes. **Figure 13.18** shows the IC/OC interrupt block diagram and **Table 13.4** shows the IC/OC interrupt assignation.

When either the base timer reset request or base timer overflow request is generated, the IR bit in the BTIC register corresponding to the IC/OC base timer interrupt is set to 1 (with an interrupt request). Also when an interrupt request in each eight channels (channel i) is generated, the bit i in the G1IR register is set to 1 (with an interrupt request). At this time, if the bit i in the G1IE0 register is 1 (IC/OC interrupt 0 request enabled), the IR bit in the ICOC0IC register corresponding to the IC/OC interrupt 0 is set to 1 (with an interrupt request). And if the bit i in the G1IE1 register is 1 (IC/OC interrupt 1 request enabled), the IR bit in the ICOC1IC register corresponding to the IC/OC interrupt 1 is set to 1(with an interrupt request).

Additionally, because each bit in the G1IR register is not automatically set to 0 even if the interrupt is acknowledged, set to 0 by program. If these bits are left as 1, all IC/OC channel interrupt causes, which are generated after setting the IR bit to 1, will be disabled.

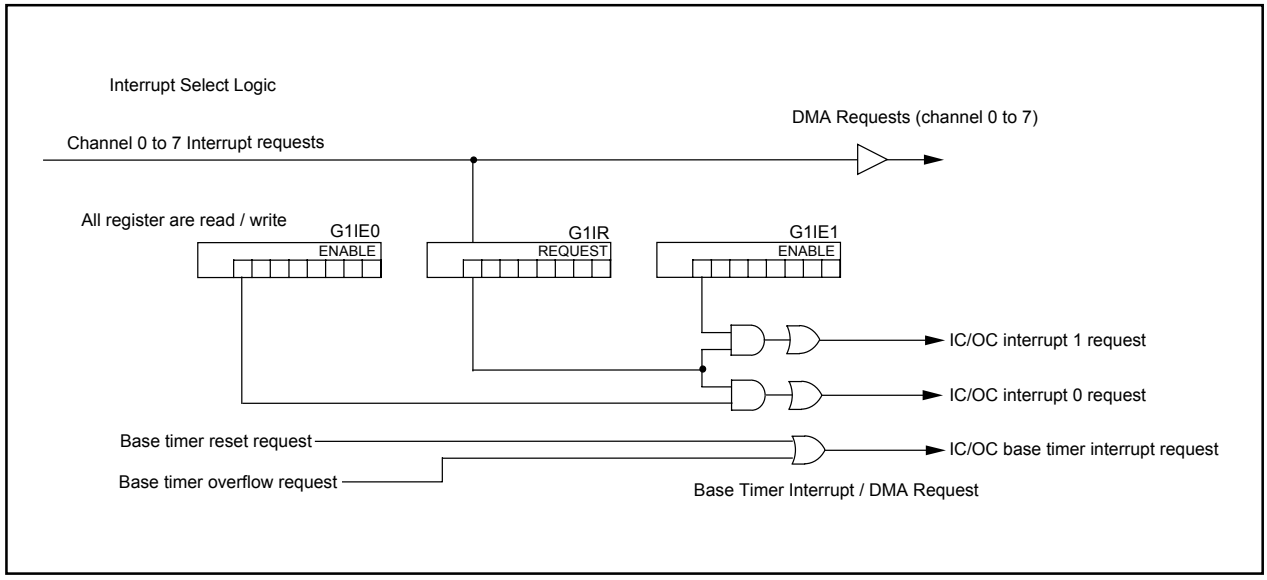


Figure 13.18 IC/OC Interrupt and DMA request generation

Table 13.4 Interrupt Assignment

Interrupt	Interrupt control register
IC/OC base timer interrupt	BTIC(0047_{16})
IC/OC interrupt 0	ICOC0IC(0045_{16})
IC/OC interrupt 1	ICOC0IC(0046_{16})

13.3 DMA Support

Each of the interrupt sources - the eight IC/OC channel interrupts and the one Base Timer interrupt - are capable of generating a DMA request.

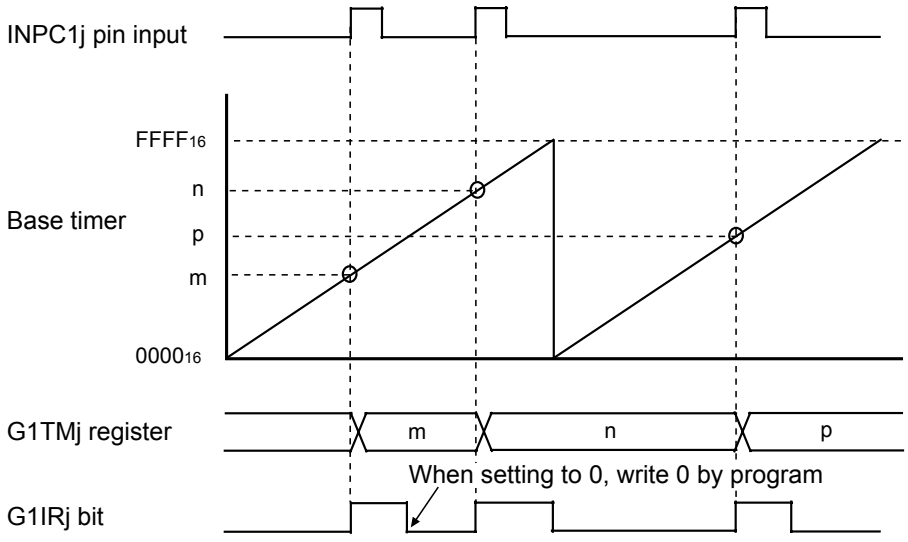
Table 13.6 Register Settings Associated with the Time Measurement Function

Register	Bit	Function
G1TMCRj	CTS1 to CTS0	Select time measurement trigger
	DF1 to DF0	Select the digital filter function
	GT, GOC, GSC	Select the gate function
	PR	Select the prescaler function
G1TPRk	-	Setting value of prescaler
G1FS	FSCj	Set to 1 (time measurement function)
G1FE	IFEj	Set to 1 (channel j function enabled)

j = 0 to 7 k = 6, 7

Bit configurations and function varys with channels used.

Registers associated with the time measurement function must be set after setting registers associated with the base timer.



j = 0 to 7
G1IRj bit: Bits in the G1IR register

The above applies to the following condition.

- Bits CTS1 to CTS0 in the G1TMCRj registers are set to 01_2 (rising edge). The PR bit is set to 0 (no prescaler used) and the GT bit is set to 0 (no gate function used).
- Bits RTS4, RTS2, and RTS1 in registers G1BCR0 and G1BCR1 are set to 0 (no base timer reset). Bits UD1 to UD0 bits are set to 00_2 (counter increment mode).

Set the base timer to 0000_{16} (setting the RST1 bit to 1, and bits RST4 and RST2 to 0), when the base timer value matches the G1PO0 register setting. The base timer is set to 0000_{16} after it reaches *the G1PO0 register value + 2*.

Figure 13.19 Time Measurement Function (1)

Table 14.3 lists pin functions for the case where the multiple transfer clock output pin select function is deselected. **Table 14.4** lists the P6$_4$ pin functions during clock synchronous serial I/O mode.
Note that for a period from when the UARTi operation mode is selected to when transfer starts, the TxDi pin outputs an “H”. (If the N-channel open-drain output is selected, this pin is in a high-impedance state.)

Table 14.3 Pin Functions (When Not Select Multiple Transfer Clock Output Pin Function)(1)

Pin Name	Function	Method of Selection
TxDi (i = 0 to 2) (P6$_3$, P6$_7$, P7$_0$)	Serial data output	(Outputs dummy data when performing reception only)
RxDi (P6$_2$, P6$_6$, P7$_1$)	Serial data input	Set the PD6_2 bit and PD6_6 bit in the PD6 register, and PD7_1 bit in the PD7 register to 0 (Can be used as an input port when performing transmission only)
CLKi (P6$_1$, P6$_5$, P7$_2$)	Transfer clock output	Set the CKDIR bit in the UiMR register to 0
	Transfer clock input	Set the CKDIR bit in the UiMR register to 1 Set the PD6_1 bit and PD6_5 bit in the PD6 register, and the PD7_2 bit in the PD7 register to 0
$\overline{\text{CTS}}$i/$\overline{\text{RTS}}$i (P6$_0$, P6$_4$, P7$_3$)	$\overline{\text{CTS}}$ input	Set the CRD bit in the UiC0 register to 0 Set the CRS bit in the UiC0 register to 0 Set the PD6_0 bit and PD6_4 bit in the PD6 register is set to 0, the PD7_3 bit in the PD7 register to 0
	$\overline{\text{RTS}}$ output	Set the CRD bit in the UiC0 register to 0 Set the CRS bit in the UiC0 register to 1
	I/O port	Set the CRD bit in the UiC0 register to 1

NOTE:
1: When the U1MAP bit in PACR register is 1 (P7$_3$ to P7$_0$), UART1 pin is assgined to P7$_3$ to P7$_0$.

Table 14.4 P6$_4$ Pin Functions(1)

Pin Function	Bit Set Value					
	U1C0 register		UCON register			PD6 register
	CRD	CRS	RCSP	CLKMD1	CLKMD0	PD6_4
P6$_4$	1	—	0	0	—	Input: 0, Output: 1
$\overline{\text{CTS}}_1$	0	0	0	0	—	0
$\overline{\text{RTS}}_1$	0	1	0	0	—	—
$\overline{\text{CTS}}_0$(2)	0	0	1	0	—	0
CLKS$_1$	—	—	—	1(3)	1	—

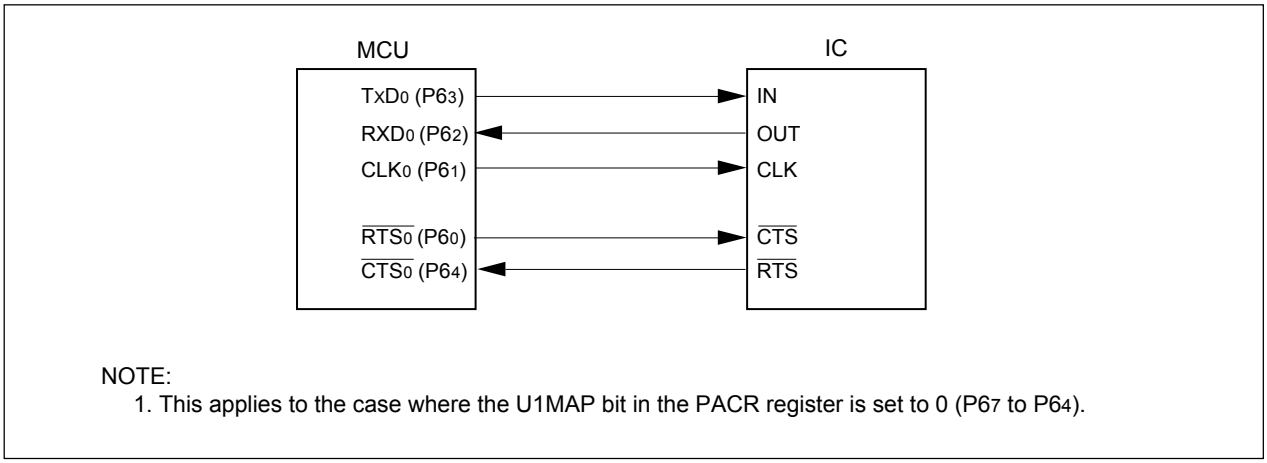
NOTES:
1. When the U1MAP bit in PACR register is 1 (P7$_3$ to P7$_0$), this table lists the P7$_0$ functions.
2. In addition to this, set the CRD bit in the U0C0 register to 0 ($\overline{\text{CT0}}_0$/$\overline{\text{RT0}}_0$ enabled) and the CRS bit in the U0C0 register to 1 ($\overline{\text{RTS}}_0$ selected).
3. When the CLKMD1 bit is set to 1 and the CLKMD0 bit is set to 0, the following logic levels are output:
   • High if the CLKPOL bit in the U1C0 register is set to 0
   • Low if the CLKPOL bit in the U1C0 register is set to 1

14.1.1.7 $\overline{CTS}/\overline{RTS}$ separate function (UART0)

This function separates $\overline{CTS}_0/\overline{RTS}_0$, outputs $\overline{RTS}_0$ from the $P6_0$ pin, and accepts as input the $\overline{CTS}_0$ from the $P6_4$ pin or $P7_0$ pin. To use this function, set the register bits as shown below.

- The CRD bit in the U0C0 register is set to 0 (enables UART0 $\overline{CTS}/\overline{RTS}$)
- The CRS bit in the U0C0 register is set to 1 (outputs UART0 $\overline{RTS}$)
- The CRD bit in the U1C0 register is set to 0 (enables UART1 $\overline{CTS}/\overline{RTS}$)
- The CRS bit in the U1C0 register is set to 0 (inputs UART1 $\overline{CTS}$)
- The RCSP bit in the UCON register is set to 1 (inputs $\overline{CTS}_0$ from the $P6_4$ pin or $P7_0$ pin)
- The CLKMD1 bit in the UCON register is set to 0 ($CLKS_1$ not used)

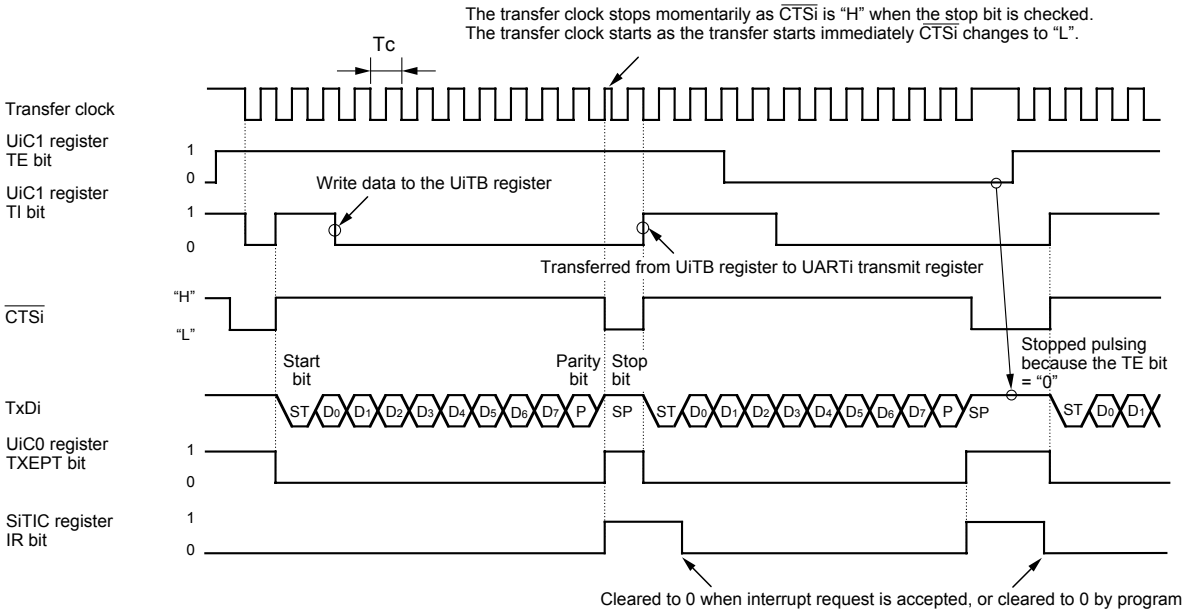
Note that when using the $\overline{CTS}/\overline{RTS}$ separate function, UART1 $\overline{CTS}/\overline{RTS}$ separate function cannot be used.



NOTE:
1. This applies to the case where the U1MAP bit in the PACR register is set to 0 ($P6_7$ to $P6_4$).

Figure 14.15 CTS/RTS separate function usage

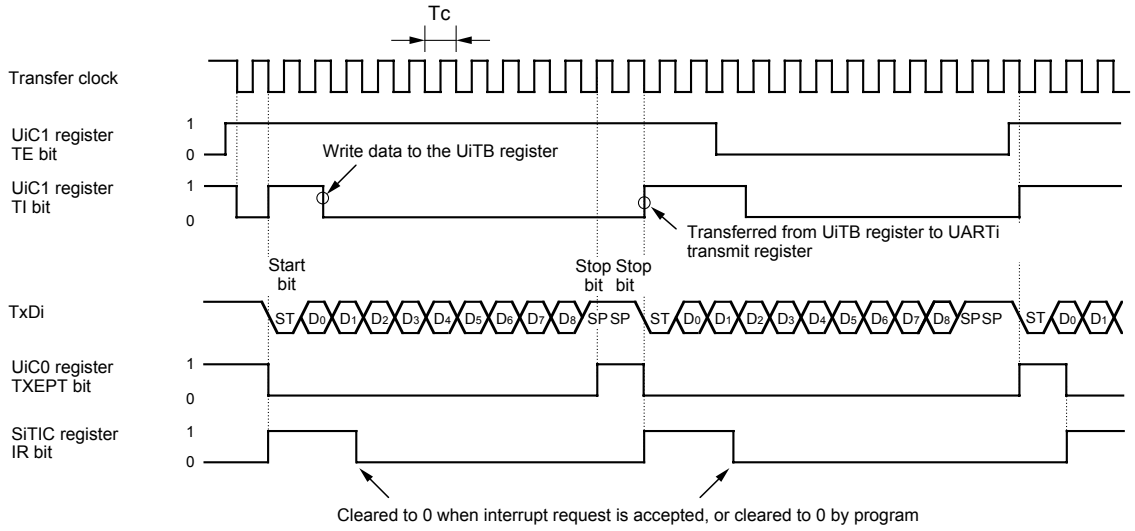
• Example of transmit timing when transfer data is 8-bit long (parity enabled, one stop bit)



The above timing diagram applies to the case where the register bits are set as follows:
- Set the PRYE bit in the UiMR register to 1 (parity enabled)
- Set the STPS bit in the UiMR register to 0 (1 stop bit)
- Set the CRD bit in the UiC0 register to 0 (CTS/RTS enabled), the CRS bit to 0 (CTS selected).
- Set the UiIRS bit to 1 (an interrupt request occurs when transmit completed):
  U0IRS bit is the UCON register bit 0, U1IRS bit is the UCON register bit 1, and U2IRS bit is the U2C1 register bit 4

Tc = 16 (n + 1) / fj or 16 (n + 1) / fEXT
fj: frequency of UiBRG count source (f1SIO, f2SIO, f8SIO, f32SIO)
fEXT: frequency of UiBRG count source (external clock)
n: value set to UiBRG
i = 0 to 2

• Example of transmit timing when transfer data is 9-bit long (parity disabled, two stop bits)



The above timing diagram applies to the case where the register bits are set as follows:
- Set the PRYE bit in the UiMR register to 0 (parity disabled)
- Set the STPS bit in the UiMR register to 1 (2 stop bits)
- Set the CRD bit in the UiC0 register to 1 (CTS/RTS disabled)
- Set the UiIRS bit to 0 (an interrupt request occurs when transmit buffer becomes empty):
  U0IRS bit is the UCON register bit 0, U1IRS bit is the UCON register bit 1, and U2IRS bit is the U2C1 register bit 4

Tc = 16 (n + 1) / fj or 16 (n + 1) / fEXT
fj: frequency of UiBRG count source (f1SIO, f2SIO, f8SIO, f32SIO)
fEXT: frequency of UiBRG count source (external clock)
n: value set to UiBRG
i = 0 to 2

Figure 14.16 Typical transmit timing in UART mode (UART0, UART1)

16.1 I2C0 Data Shift Register (S00 register)

The S00 register is an 8-bit data shift register to store a received data and to write a transmit data. When a transmit data is written to the S00 register, the transmit data is synchronized with a SCL clock and the data is transferred from bit 7. Then, every one bit of the data is transmitted, the register's content is shifted for one bit to the left. When the SCL clock and the data is imported into the S00 register from bit 0. Every one bit of the data is imported, the register's content is shifted for one bit to the left. **Figure 16.9** shows the timing to store the receive data to the S00 register.

The S00 register can be written when the ES0 bit in the S1D0 register is set to 1 (I2C0 bus interface enabled). If the S00 register is written when the ES0 bit is set to 1 and the MST bit in the S10 register is set to 1 (master mode), the bit counter is reset and the SCL clock is output. Write to the S00 register when the START condition is generatedor when an "L" signal is applied to the SCL pin. The S00 register can be read anytime regardless of the ES0 bit value.

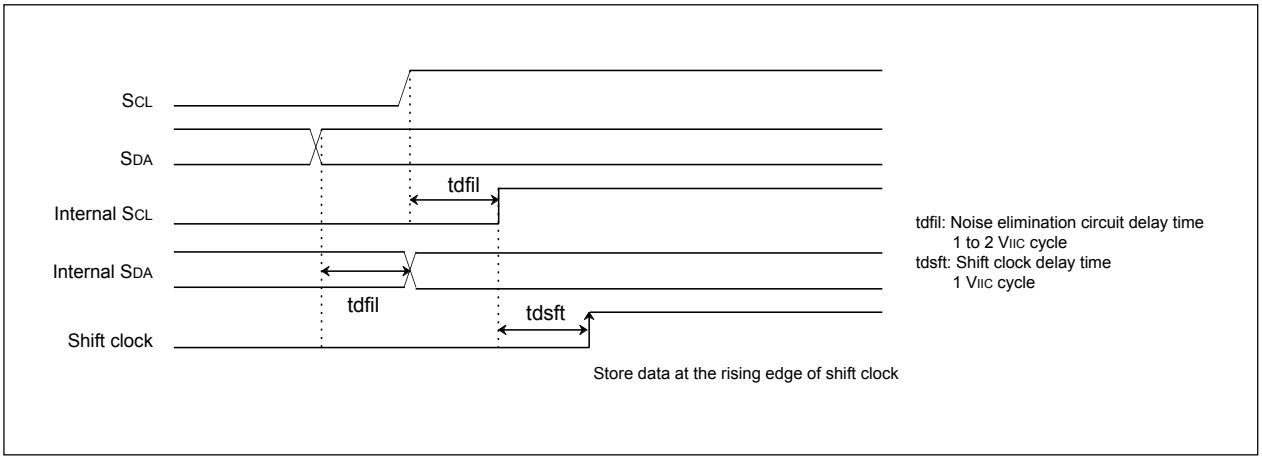


Figure 16.9 The Receive Data Storing Timing of S00 Register

16.2 I2C0 Address Register (S0D0 register)

The S0D0 register consists of bits SAD6 to SAD0, total of 7. At the addressing is formatted, slave address is detected automatically and the 7-bit received address data is compared with the contents of bits SAD6 to SAD0.

17.1.3.3 C0STR Register

Figure 17.8 shows the C0STR register.

CAN0 Status Register

b7	b6	b5	b4	b3	b2	b1	b0

Symbol	Address	After Reset
C0STR	021216	0016

Bit Symbol	Bit Name	Function	RW
MBOX	Active slot bits(1)	b3 b2 b1 b0 0 0 0 0: Slot 0 0 0 0 1: Slot 1 0 0 1 0: Slot 2 ⋮ 1 1 1 0: Slot 14 1 1 1 1: Slot 15	RO
TrmSucc	Successful transmission flag(1)	0: No [successful] transmission 1: The CAN module has transmitted a message successfully	RO
RecSucc	Successful reception flag (1)	0: No [successful] reception 1: CAN module received a message successfully	RO
TrmState	Transmission flag (Transmitter)	0: CAN module is idle or receiver 1: CAN module is transmitter	RO
RecState	Reception flag (Receiver)	0: CAN module is idle or transmitter 1: CAN module is receiver	RO

NOTE:
1. These bits can be changed only when a slot which an interrupt is enabled by the C0ICR register is transmitted or received successfully.

(b15)							(b8)
b7	b6	b5	b4	b3	b2	b1	b0
X							

Symbol	Address	After Reset
C0STR	021316	X0000001₂

Bit Symbol	Bit Name	Function	RW
State_Reset	Reset state flag	0: Operation mode 1: Reset mode	RO
State_ LoopBack	Loop back state flag	0: Loop back mode disabled 1: Loop back mode enabled	RO
State_ MsgOrder	Message order state flag	0: Word access 1: Byte access	RO
State_ BasicCAN	Basic CAN mode state flag	0: Basic CAN mode disabled 1: Basic CAN mode enabled	RO
State_ BusError	Bus error state flag	0: No error has occurred. 1: A CAN bus error has occurred.	RO
State_ ErrPass	Error passive state flag	0: The CAN module is not in error passive state. 1: The CAN module is in error passive state.	RO
State_ BusOff	Error bus off state flag	0: The CAN module is not in error bus off state. 1: The CAN module is in error bus off state.	RO
— (b7)	Nothing is assigned. If necessary, set to 0. When read, the content is undefined		—

Figure 17.8 C0STR Register

17.2.4 CAN Interface Sleep Mode

The CAN interface sleep mode is activated by setting the CCLK3 bit in the CCLKR register to 1. It should never be activated but only via the CAN sleep mode.

Entering the CAN interface sleep mode instantly stops the clock supply to the CPU Interface in the module and thereby reduces power dissipation.

17.2.5 Bus Off State

The bus off state is entered according to the fault confinement rules of the CAN specification. When returning to the CAN operating mode from the bus off state, the module has the following two cases.

In this time, the value of any CAN registers, except registers C0STR, C0RECR, and C0TECR, does not change.

(1) When 11 consecutive recessive bits are detected 128 times

The module enters instantly into error active state and the CAN communication becomes possible immediately.

(2) When the RetBusOff bit in the C0CTLR register = 1 (Force return from buss off)

The module enters instantly into error active state, and the CAN communication becomes possible again after 11 consecutive recessive bits are detected.

17.11 CAN Interrupts

The CAN module provides the following CAN interrupts.

- CAN0 Successful Reception Interrupt
- CAN0 Successful Transmission Interrupt
- CAN0 Error Interrupt
  - Error Passive State
  - Error BusOff State
  - Bus Error (this feature can be disabled separately)
- CAN0 Wake-up Interrupt

When the CPU detects the CAN0 successful reception/transmission interrupt request, the MBOX bit in the C0STR register must be read to determine which slot has generated the interrupt request.

18. CRC Calculation Circuit

The Cyclic Redundancy Check (CRC) calculation detects errors in blocks of data. The MCU uses a generator polynomial of CRC_CCITT ($X^{16} + X^{12} + X^5 + 1$) or CRC-16 ($X^{16} + X^{15} + X^2 + 1$) to generate CRC code.

The CRC code is a 16-bit code generated for a block of a given data length in multiples of bytes. The code is updated in the CRC data register everytime one byte of data is transferred to a CRC input register. The data register must be initialized before use. Generation of CRC code for one byte of data is completed in two machine cycles.

Figure 18.1 shows the block diagram of the CRC circuit. **Figure 18.2** shows the CRC-related registers. **Figure 18.3** shows the calculation example using the CRC_CCITT operation.

18.1 CRC Snoop

The CRC circuit includes the ability to snoop reads and writes to certain SFR addresses. This can be used to accumulate the CRC value on a stream of data without using extra bandwidth to explicitly write data into the CRCIN register. All SFR addresses after 0020_{16} are subject to the CRC snoop. The CRC snoop is useful to snoop the writes to a UART TX buffer, or the reads from a UART RX buffer.

To snoop an SFR address, the target address is written to the CRC snoop Address Register (CRCSAR). The two most significant bits of this register enable snooping on reads or writes to the target address. If the target SFR is written to by the CPU or DMA, and the CRC snoop write bit is set (CRCSW=1), the CRC will latch the data into the CRCIN register. The new CRC code will be set in the CRCD register.

Similarly, if the target SFR is read by the CRC or DMA, and the CRC snoop read bit is set (CRCSR=1), the CRC will latch the data from the target into the CRCIN register and calculate the CRC.

The CRC circuit can only calculate CRC codes on data byte at a time. Therefore, if a target SFR is accessed in word (16 bit), only one low-order byte data is stored into the CRCIN register.

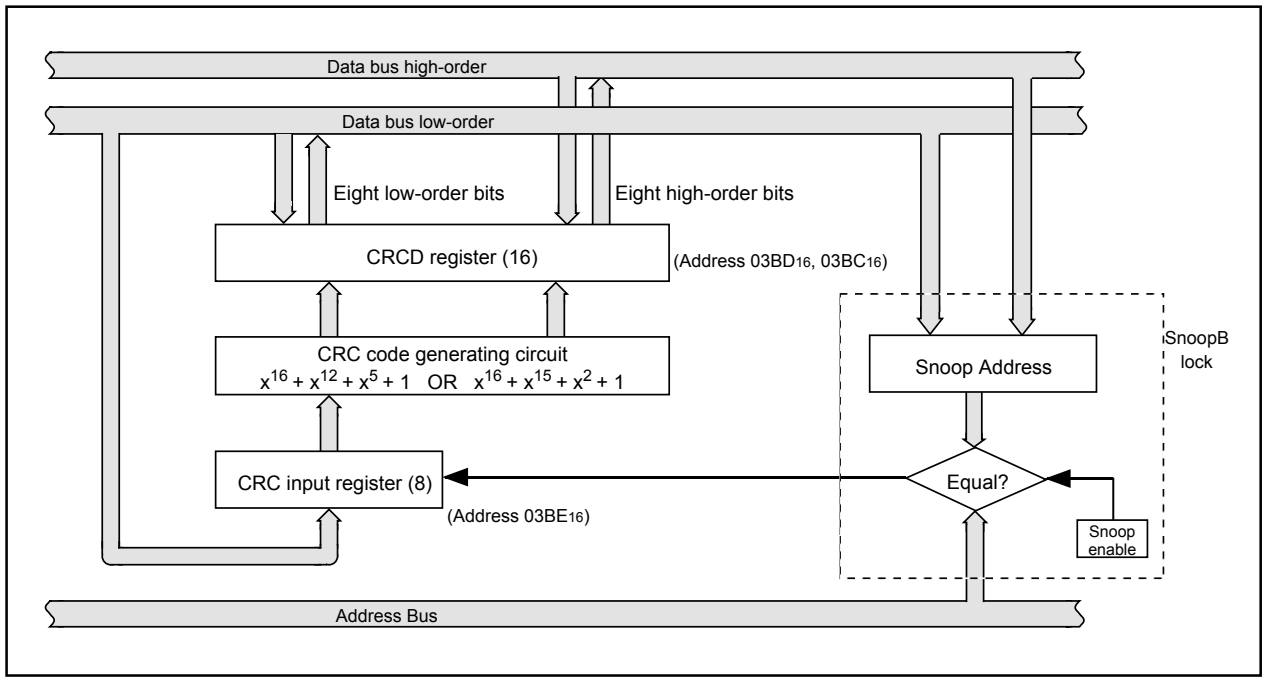


Figure 18.1 CRC circuit block diagram

20.11 CAN I/O Mode

Note

The CAN I/O mode is not available in M16C/29 T-ver./V-ver.

In CAN I/O mode, the user ROM area can be rewritten while the MCU is mounted on-board by using a CAN programmer which is applicable for the M16C/29 group. For more information about CAN programmers, contact the manufacturer of your CAN programmer. For details on how to use, refer to the user's manual included with your CAN programmer.
Table 20.9 lists pin functions for CAN I/O mode. Figures 20.19 and 20.20 show pin connections for CAN I/O mode.

20.11.1 ID code check function

This function determines whether the ID codes sent from the CAN programmer and those written in the flash memory match.(Refer to **20.3 Functions To Prevent Flash Memory from Rewriting**.)

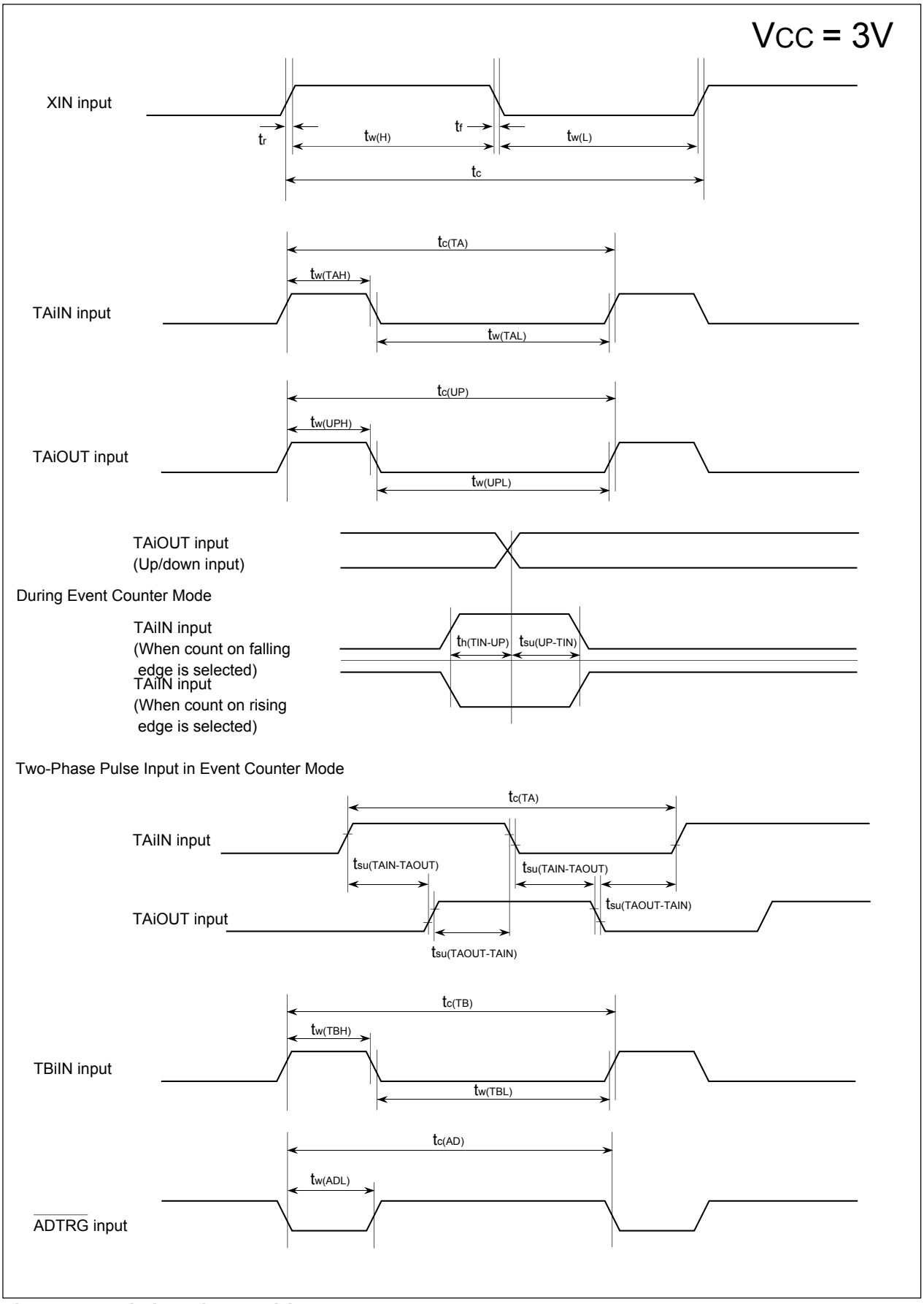


Figure 21.4 Timing Diagram (1)

V_{CC} = 5V

Table 21.47 Electrical Characteristics (2) (Note 1)

Symbol	Parameter	Measurement Condition			Standard			Unit
					Min.	Typ.	Max.	
I_{CC}	Power Supply Current (V_{CC}=4.2 to 5.5V)	Output pins are left open and other pins are connected to V_{SS}	Mask ROM	f(BCLK) = 20 MHz, main clock, no division		18	25	mA
				On-chip oscillation, $f_{2(ROC)}$ selected, f(BCLK) = 1 MHz		2		mA
			Flash memory	f(BCLK) = 20 MHz, main clock, no division		18	25	mA
				On-chip oscillation, $f_{2(ROC)}$ selected, f(BCLK) = 1 MHz		2		mA
			Flash memory program	f(BCLK) = 10 MHz, Vcc = 5.0 V		11		mA
			Flash memory erase	f(BCLK) = 10 MHz, Vcc = 5.0 V		11		mA
			Mask ROM	f(BCLK) = 32 kHz, In low-power consumption mode, Program running on ROM(3)		25		µA
				On-chip oscillation, $f_{2(ROC)}$ selected, f(BCLK) = 1 MHz, In wait mode		50		µA
			Flash memory	f(BCLK) = 32 kHz, In low-power consumption mode, Program running on RAM(3)		25		µA
				f(BCLK) = 32 kHz, In low-power consumption mode, Program running on flash memory(3)		450		µA
				On-chip oscillation, $f_{2(ROC)}$ selected, f(BCLK) = 1 MHz, In wait mode		50		µA
			Mask ROM, Flash memory	f(BCLK) = 32 kHz, In wait mode(2), Oscillation capacity high		8.5		µA
				f(BCLK) = 32 kHz, In wait mode(2), Oscillation capacity low		3		µA
				While clock stops, Topr = 25° C		0.8	3	µA

NOTES:

1. Referenced to V_{CC} = 4.2 to 5.5 V, V_{SS} = 0 V at Topr = -40 to 85 ° C, f(BCLK) = 20 MHz unless otherwise specified.
2. With one timer operates, using f_{C32}.
3. This indicates the memory in which the program to be executed exists.

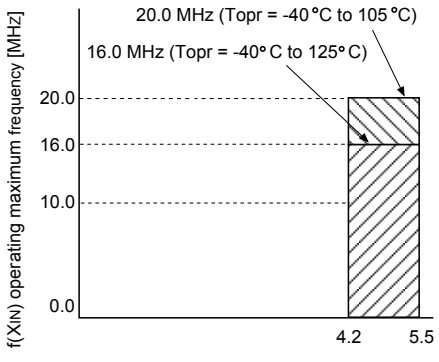
Table 21.79 Recommended Operating Conditions (1)

Symbol	Parameter			Standard			Unit
				Min.	Typ.	Max.	
V_{CC}	Supply Voltage			4.2		5.5	V
AVcc	Analog Supply Voltage				Vcc		V
V_{SS}	Supply Voltage				0		V
AVss	Analog Supply Voltage				0		V
V_{IH}	Input High ("H") Voltage	$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_7$, $P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_7$, $P9_0$ to $P9_3$, $P9_5$ to $P9_7$, $P10_0$ to $P10_7$		0.7 Vcc		Vcc	V
		XIN, $\overline{RESET}$, CNVSS		0.8 Vcc		Vcc	V
		SDAMM, SCLMM	When I^2C bus input level is selected	0.7 Vcc		Vcc	V
			When SMBUS input level is selected	1.4		Vcc	V
V_{IL}	Input Low ("L") Voltage	$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_7$, $P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_7$, $P9_0$ to $P9_3$, $P9_5$ to $P9_7$, $P10_0$ to $P10_7$		0		0.3Vcc	V
		XIN, $\overline{RESET}$, CNVSS		0		0.2Vcc	V
		SDAMM, SCLMM	When I^2C bus input level is selected	0		0.3Vcc	V
			When SMBUS input level is selected	0		0.6	V
$I_{OH(peak)}$	Peak Output High ("H") Current	$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_7$, $P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_7$, $P9_0$ to $P9_3$, $P9_5$ to $P9_7$, $P10_0$ to $P10_7$				-10.0	mA
$I_{OH(avg)}$	Average Output High ("H") Current	$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_7$, $P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_7$, $P9_0$ to $P9_3$, $P9_5$ to $P9_7$, $P10_0$ to $P10_7$				-5.0	mA
$I_{OL(peak)}$	Peak Output Low ("L") Current	$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_7$, $P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_7$, $P9_0$ to $P9_3$, $P9_5$ to $P9_7$, $P10_0$ to $P10_7$				10.0	mA
$I_{OL(avg)}$	Average Output Low ("L") Current	$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_7$, $P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_7$, $P9_0$ to $P9_3$, $P9_5$ to $P9_7$, $P10_0$ to $P10_7$				5.0	mA
f(X_{IN})	Main Clock Input Oscillation Frequency(4)		Topr = -40 to 105 ° C	0		20	MHz
			Topr = -40 to 125 ° C	0		16	MHz
f(X_{CIN})	Sub Clock Oscillation Frequency				32.768	50	kHz
f_1(ROC)	On-chip Oscillator Frequency 1			0.5	1	2	MHz
f2(ROC)	On-chip Oscillator Frequency 2			1	2	4	MHz
f3(ROC)	On-chip Oscillator Frequency 3			8	16	26	MHz
f(PLL)	PLL Clock Oscillation Frequency(4)		Topr = -40 to 105 ° C	10		20	MHz
			Topr = -40 to 125 ° C	10		16	MHz
f(BCLK)	CPU Operation Clock Frequency		Topr = -40 to 105 ° C	0		20	MHz
			Topr = -40 to 125 ° C	0		16	MHz
t_{SU}(PLL)	Wait Time to Stabilize PLL Frequency Synthesizer		Vcc = 5.0 V			20	MHz

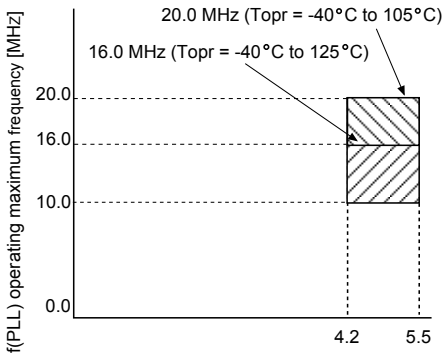
NOTES:

1. Referenced to Vcc = 4.2 to 5.5 V at Topr = -40 to 125 ° C unless otherwise specified.
2. The mean output current is the mean value within 100ms.
3. The total $I_{OL(peak)}$ for all ports must be 80 mA or less. The total $I_{OH(peak)}$ for all ports must be -80 mA or less.
4. Relationship among main clock oscillation frequency, PLL clock oscillation frequency and supply voltage.

Main clock input oscillation frequency



PLL clock oscillation frequency



22.3 Protection

Set the PRC2 bit to 1 (write enabled) and then write to any address, and the PRC2 bit will be cleared to 0 (write protected). The registers protected by the PRC2 bit should be changed in the next instruction after setting the PRC2 bit to 1. Make sure no interrupts or DMA transfers will occur between the instruction in which the PRC2 bit is set to 1 and the next instruction.