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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	M16C/60
Core Size	16-Bit
Speed	20MHz
Connectivity	CANbus, I²C, IEBus, SIO, UART/USART
Peripherals	DMA, POR, PWM, Voltage Detect, WDT
Number of I/O	71
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 27x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30290fcthp-u3a

1. Overview

1.1 Features

The M16C/29 Group of single-chip control MCU incorporates the M16C/60 series CPU core, employing the high-performance silicon gate CMOS technology and sophisticated instructions for a high level of efficiency. The M16C/29 Group is housed in 64-pin and 80-pin plastic molded LQFP packages. These single-chip MCUs operate using sophisticated instructions featuring a high level of instruction efficiency. This MCU is capable of executing instructions at high speed and it has one CAN module, makes it suitable for control of cars and LAN system of FA. In addition, the CPU core boasts a multiplier and DMAC for high-speed processing to make adequate for office automation, communication devices, and other high-speed processing applications.

1.1.1 Applications

Automotive body, car audio, LAN system of FA, etc.

Table 1.6 Product Codes of Flash Memory Version -M16C/29 Group, Normal-ver.

Product Code	Package	Internal ROM (User Program Space: Blocks 0 to 5)		Internal ROM (Data Space: Blocks A and B)		Operating Ambient Temperature
		Program and Erase Endurance	Temperature Range	Program and Erase Endurance	Temperature Range	
U3	Lead-free	100	0 to 60°C	100	0 to 60°C	-40 to 85°C
U5						-20 to 85°C
U7		1,000		10,000	-40 to 85°C	-40 to 85°C
U9					-20 to 85°C	-20 to 85°C

Table 1.7 Product Codes of Flash Memory Version -M16C/29 Group, T-ver.

Product Code	Package	Internal ROM (User Program Space: Blocks 0 to 5)		Internal ROM (Data Space: Blocks A and B)		Operating Ambient Temperature
		Program and Erase Endurance	Temperature Range	Program and Erase Endurance	Temperature Range	
U3	Lead-free	100	0 to 60°C	100	-40 to 85°C	-40 to 85°C
U7		1,000		10,000		

Table 1.8 Product Codes of Flash Memory Version -M16C/29 Group, V-ver.

Product Code	Package	Internal ROM (User Program Space: Blocks 0 to 5)		Internal ROM (Data Space: Blocks A and B)		Operating Ambient Temperature
		Program and Erase Endurance	Temperature Range	Program and Erase Endurance	Temperature Range	
U3	Lead-free	100	0 to 60°C	100	-40 to 125°C	-40 to 125°C
U7		1,000		10,000		

Table 1.9 Product Codes of Mask ROM Version -M16C/29 Group, Normal-ver.

Product Code	Package	Operating Ambient Temperature
U3	Lead-free	-40 to 85°C
U5		-20 to 85°C

Table 1.10 Product Code of Mask ROM Version -M16C/29 Group, T-ver.

Product Code	Package	Operating Ambient Temperature
U0	Lead-free	-40 to 85°C

Table 1.11 Product Code of Mask ROM Version -M16C/29 Group, V-ver.

Product Code	Package	Operating Ambient Temperature
U0	Lead-free	-40 to 125°C

Table 4.7 SFR Information (7)

Address	Register	Symbol	After reset
0200₁₆	CAN0 message control register 0	C0MCTL0	00₁₆
0201₁₆	CAN0 message control register 1	C0MCTL1	00₁₆
0202₁₆	CAN0 message control register 2	C0MCTL2	00₁₆
0203₁₆	CAN0 message control register 3	C0MCTL3	00₁₆
0204₁₆	CAN0 message control register 4	C0MCTL4	00₁₆
0205₁₆	CAN0 message control register 5	C0MCTL5	00₁₆
0206₁₆	CAN0 message control register 6	C0MCTL6	00₁₆
0207₁₆	CAN0 message control register 7	C0MCTL7	00₁₆
0208₁₆	CAN0 message control register 8	C0MCTL8	00₁₆
0209₁₆	CAN0 message control register 9	C0MCTL9	00₁₆
020A₁₆	CAN0 message control register 10	C0MCTL10	00₁₆
020B₁₆	CAN0 message control register 11	C0MCTL11	00₁₆
020C₁₆	CAN0 message control register 12	C0MCTL12	00₁₆
020D₁₆	CAN0 message control register 13	C0MCTL13	00₁₆
020E₁₆	CAN0 message control register 14	C0MCTL14	00₁₆
020F₁₆	CAN0 message control register 15	C0MCTL15	00₁₆
0210₁₆ 0211₁₆	CAN0 control register	C0CTLR	X0000001₂ XX0X0000₂
0212₁₆ 0213₁₆	CAN0 status register	C0STR	00₁₆ X0000001₂
0214₁₆ 0215₁₆	CAN0 slot status register	C0SSTR	00₁₆ 00₁₆
0216₁₆ 0217₁₆	CAN0 interrupt control register	C0ICR	00₁₆ 00₁₆
0218₁₆ 0219₁₆	CAN0 extended ID register	C0IDR	00₁₆ 00₁₆
021A₁₆ 021B₁₆	CAN0 configuration register	C0CONR	XX₁₆ XX₁₆
021C₁₆	CAN0 receive error count register	C0RECR	00₁₆
021D₁₆	CAN0 transmit error count register	C0TECR	00₁₆
021E₁₆ 021F₁₆	CAN0 time stamp register	C0TSR	00₁₆ 00₁₆
≈			≈
0242₁₆ 0243₁₆	CAN0 acceptance filter support register	C0AFS	XX₁₆ XX₁₆
≈			≈
025A₁₆	Three-phase protect control register	TPRC	00₁₆
025B₁₆			
025C₁₆	On-chip oscillator control register	ROCR	00000101₂
025D₁₆	Pin assignment control register	PACR	00₁₆
025E₁₆	Peripheral clock select register	PCLKR	00000011₂
025F₁₆	CAN0 clock select register	CCLKR	00₁₆
≈			≈
02E0₁₆	I^2C0 data-shift register	S00	XX₁₆
02E1₁₆			
02E2₁₆	I^2C0 address register	S0D0	00₁₆
02E3₁₆	I^2C0 control register 0	S1D0	00₁₆
02E4₁₆	I^2C0 clock control register	S20	00₁₆
02E5₁₆	I^2C0 start/stop condition control register	S2D0	00011010₂
02E6₁₆	I^2C0 control register 1	S3D0	00110000₂
02E7₁₆	I^2C0 control register 2	S4D0	00₁₆
02E8₁₆	I^2C0 status register	S10	0001000X₂
≈			≈
02FD₁₆			
02FE₁₆			
02FF₁₆			

Note 1: The blank areas are reserved and cannot be used by users.

X : Undefined

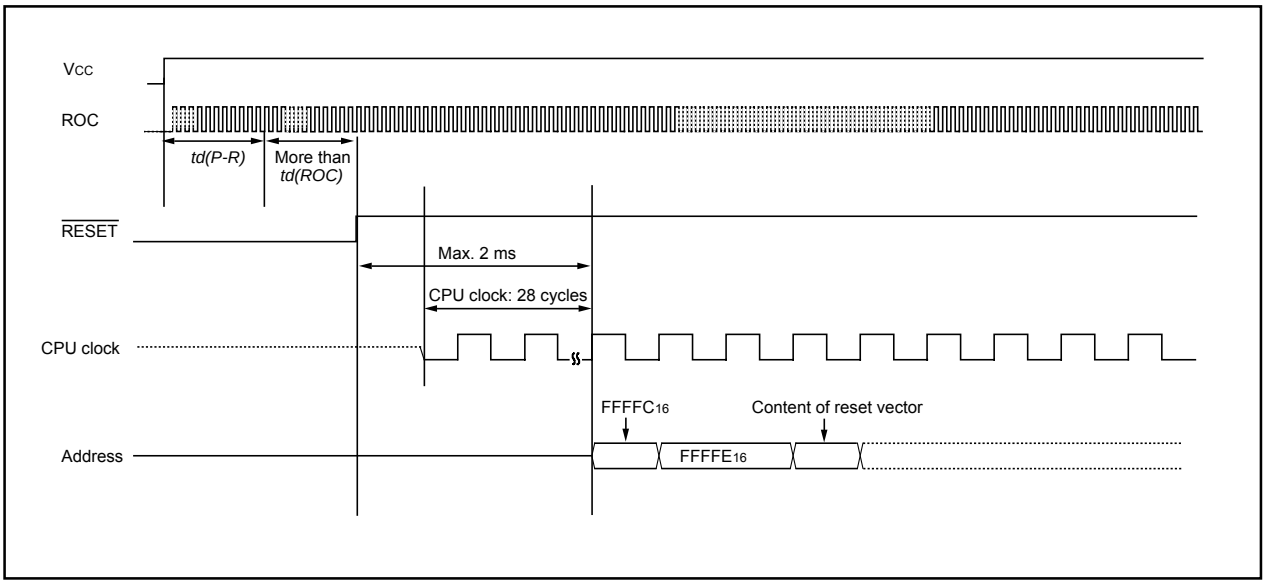


Figure 5.2 Reset Sequence

Table 5.1 Pin Status When $\overline{\text{RESET}}$ Pin Level is "L"

Pin name	Status
P0 to P3, P6 to P10	Input port (high impedance)

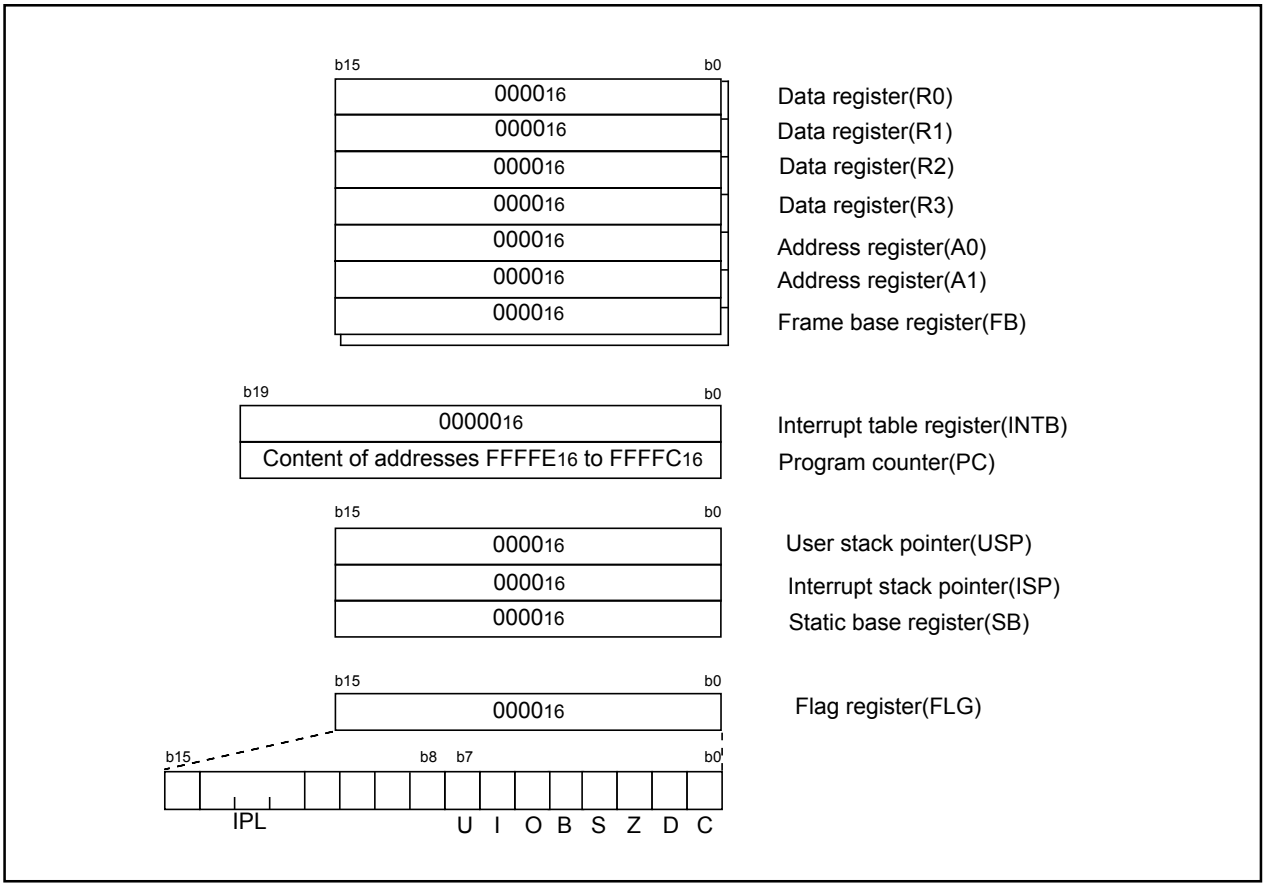


Figure 5.3 CPU Register Status After Reset

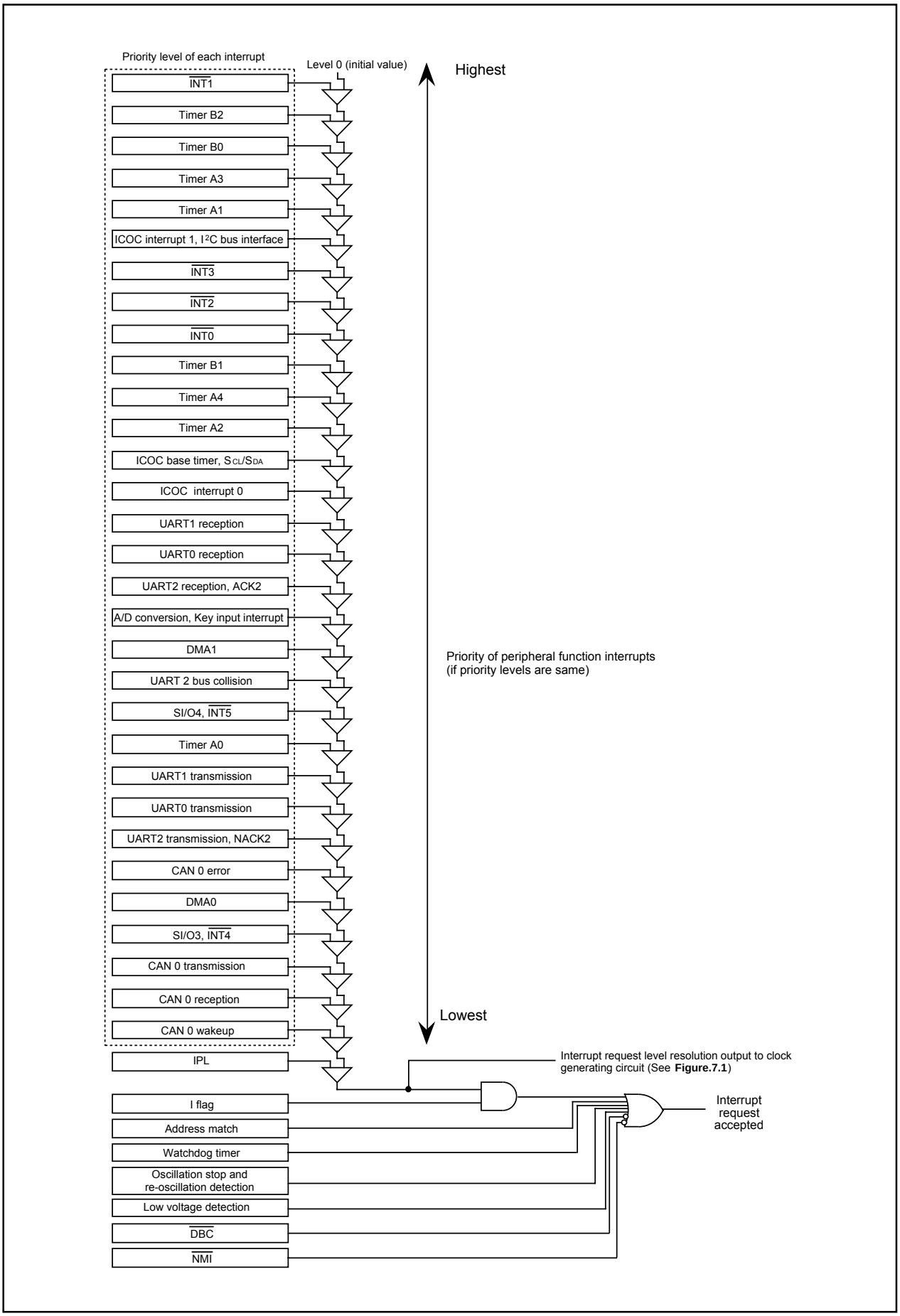


Figure 9.10 Interrupts Priority Select Circuit

10. Watchdog Timer

The watchdog timer is the function of detecting when the program is out of control. Therefore, we recommend using the watchdog timer to improve reliability of a system. The watchdog timer contains a 15-bit counter which counts down the clock derived by dividing the CPU clock using the prescaler. Whether to generate a watchdog timer interrupt request or apply a watchdog timer reset as an operation to be performed when the watchdog timer underflows after reaching the terminal count can be selected using the PM12 bit in the PM1 register. The PM12 bit can only be set to 1 (reset). Once this bit is set to 1, it cannot be set to 0 (watchdog timer interrupt) in a program. Refer to **5.3 Watchdog Timer Reset** for the details of watchdog timer reset.

When the main clock source is selected for CPU clock, on-chip oscillator clock, PLL clock, the WDC7 bit in the WDC register value for prescaler can be chosen to be 16 or 128. If a sub-clock is selected for CPU clock, the prescaler is always 2 no matter how the WDC7 bit is set. The period of watchdog timer can be calculated as given below. The period of watchdog timer is, however, subject to an error due to the prescaler.

With main clock source chosen for CPU clock, on-chip oscillator clock, PLL clock

$$\text{Watchdog timer period} = \frac{\text{Prescaler dividing (16 or 128) X Watchdog timer count (32768)}}{\text{CPU clock}}$$

With sub-clock chosen for CPU clock

$$\text{Watchdog timer period} = \frac{\text{Prescaler dividing (2) X Watchdog timer count (32768)}}{\text{CPU clock}}$$

For example, when CPU clock is set to 16 MHz and the divide-by-N value for the prescale ris set to 16, the watchdog timer period is approx. 32.8 ms.

The watchdog timer is initialized by writing to the WDTS register. The prescaler is initialized after reset. Note that the watchdog timer and the prescaler both are inactive after reset, so that the watchdog timer is activated to start counting by writing to the WDTS register.

Write the WDTS register with shorter cycle than the watchdog timer cycle. Set the WDTS register also in the beginning of the watchdog timer interrupt routine.

In stop mode and wait mode, the watchdog timer and prescaler are stopped. Counting is resumed from the held value when the modes or state are released.

Figure 10.1 shows the block diagram of the watchdog timer. Figure 10.2 shows the watchdog timer-related registers.

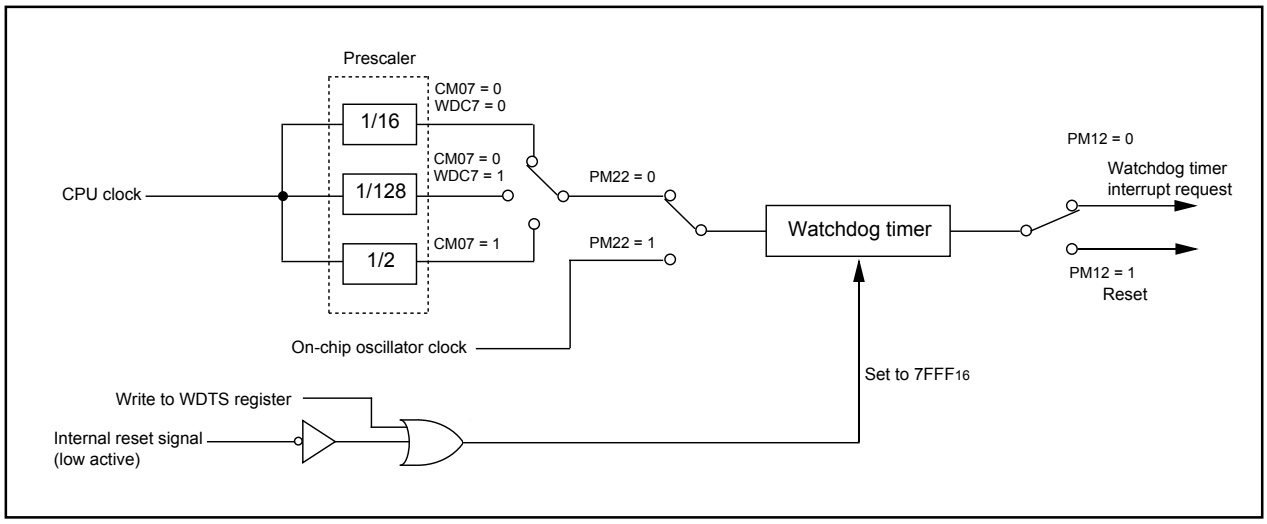


Figure 10.1 Watchdog Timer Block Diagram

12.2.4 A/D Trigger Mode

A/D trigger mode is used together with simultaneous sample sweep mode or delayed trigger mode 0 of A/D conversion to start A/D conversion. It is used in timer B0 and timer B1 only. In this mode, the timer starts counting by one trigger until the count value becomes 0000_{16}. **Figure 12.23** shows the TBiMR register in A/D trigger mode and **Figure 12.24** shows the TB2SC register.

Table 12.9 Specifications in A/D Trigger Mode

Item	Specification
Count Source	f_1, f_2, f_8, f_{32}, and f_{C32}
Count Operation	• Decrement • When the timer underflows, reload register contents are reloaded before stopping counting • When a trigger is generated during the count operation, the count is not affected
Divide Ratio	1/(n+1) n: Setting value of TBi register (i=0,1) 0000_{16}-$FFFF_{16}$
Count Start Condition	When the TBiS (i=0,1) bit in the TABSR register is 1(count started), TBiEN(i=0,1) in TB2SC register is 1 (A/D trigger mode) and the following trigger is generated.(Selection based on bits TB2SEL in the TB2SC) • Timer B2 interrupt • Underflow of Timer B2 interrupt generation frequency counter setting
Count Stop Condition	• After the count value is 0000_{16} and reload register contents are reloaded • Set the TBiS bit to 0 (count stopped)
Interrupt Request Generation Timing	Timer underflows (1)
TBiIN Pin Function	I/O port
Read From Timer	Count value can be read by reading TBi register
Write To Timer (2)	• When writing in the TBi register during count stopped. Value is written to both reload register and counter • When writing in the TBi register during count. Value is written to only reload register (Transfered to counter when reloaded next)

NOTES:
1: A/D conversion is started by the timer underflow. For details refer to **15. A/D Converter**.
2: When using in delayed trigger mode 0, set the larger value than the value of the timer B0 register to the timer B1 register.

13.5.2 Phase-Delayed Waveform Output Mode

Output signal level of the OUTC1j pin is inversed every time the base timer value matches the G1POj register value (j=0 to 7). **Table 13.9** lists specifications of phase-delayed waveform mode. **Figure 13.23** shows an example of phase-delayed waveform mode operation.

Table 13.9 Phase-delayed Waveform Output Mode Specifications

Item	Specification
Output waveform	• Free-running operation (bits RST1, RST2, and RST4 in registers G1BCR1 and G1BCR0 are set to 0 (no reset)) Cycle : $\frac{65536 \times 2}{f_{BT1}}$ "H" and "L" width : $\frac{65536}{f_{BT1}}$ • The base timer is cleared to 0000_{16} by matching the base timer with either following register (a) G1PO0 register (enabled by setting RST1 bit to 1, and bits RST4 and RST2 to 0), or (b) G1BTRR register (enabled by setting RST4 bit to 1, and bits RST2 and RST1 to 0) Cycle : $\frac{2(n+2)}{f_{BT1}}$ "H" and "L" width : $\frac{n+2}{f_{BT1}}$ n : setting value of either G1PO0 register or G1BTRR register
Waveform output start condition	The IFEj bit in the G1FE register is set to 1 (channel j function enabled)
Waveform output stop condition	The IFEj bit is set to 0 (channel j function disabled)
Interrupt request	The G1IRj bit in the interrupt request register is set to 1 when the base timer value matches the G1POj register value. (See **Figure 13.23**)
OUTC1j pin (1)	Pulse signal output pin
Selectable function	• Default value set function: Set starting waveform output level • Inverse output function : Waveform output signal is inversed and provided from the OUTC1j pin

NOTE:
1. Pins $OUTC1_0$ to $OUTC1_7$.

14.1.1.1 Counter Measure for Communication Error Occurs

If a communication error occurs while transmitting or receiving in clock synchronous serial I/O mode, follow the procedures below.

•Resetting the UiRB register (i=0 to 2)

(1) Set the RE bit in the UiC1 register to 0 (reception disabled)

(2) Set bits SMD2 to SMD0 in the UiMR register to 000_2 (Serial I/O disabled)

(3) Set bits SMD2 to SMD0 in the UiMR register to 001_2 (Clock synchronous serial I/O mode)

(4) Set the RE bit in the UiC1 register to 1 (reception enabled)

•Resetting the UiTB register (i=0 to 2)

(1) Set bits SMD2 to SMD0 in the UiMR register to 000_2 (Serial I/O disabled)

(2) Set bits SMD2 to SMD0 in the UiMR register to 001_2 (Clock synchronous serial I/O mode)

(3) 1 is written to TE bit in the UiC1 register (reception enabled), regardless to the TE bit.

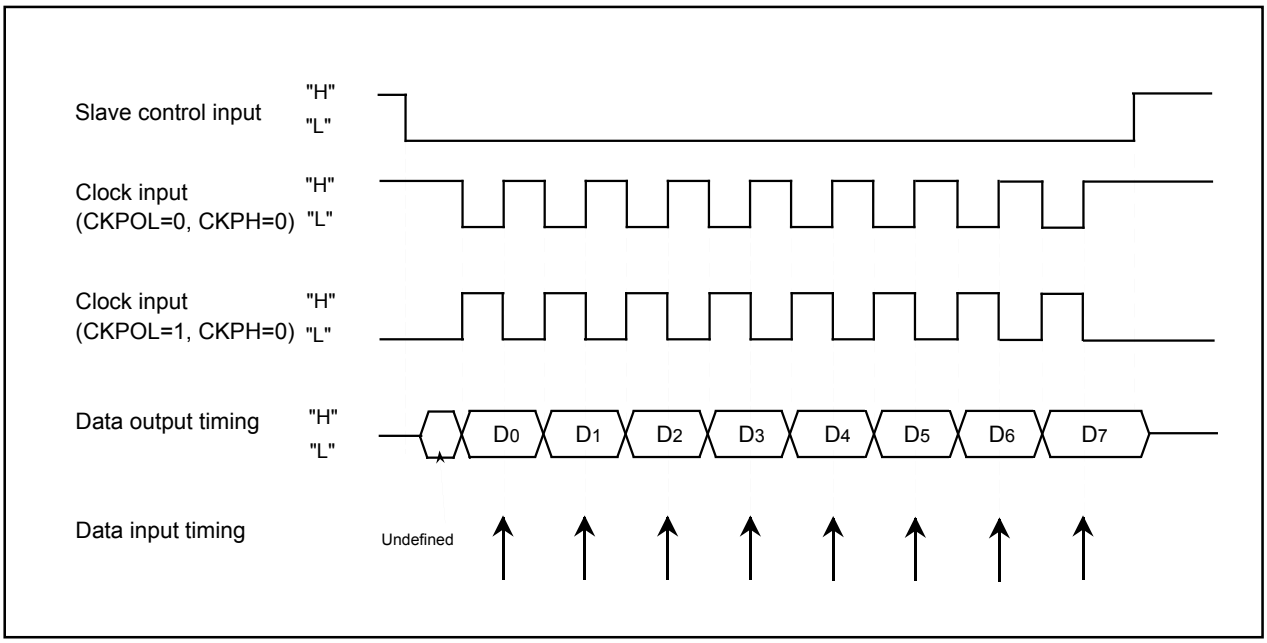


Figure 14.28 Transmission and Reception Timing (CKPH=0) in Slave Mode (External Clock)

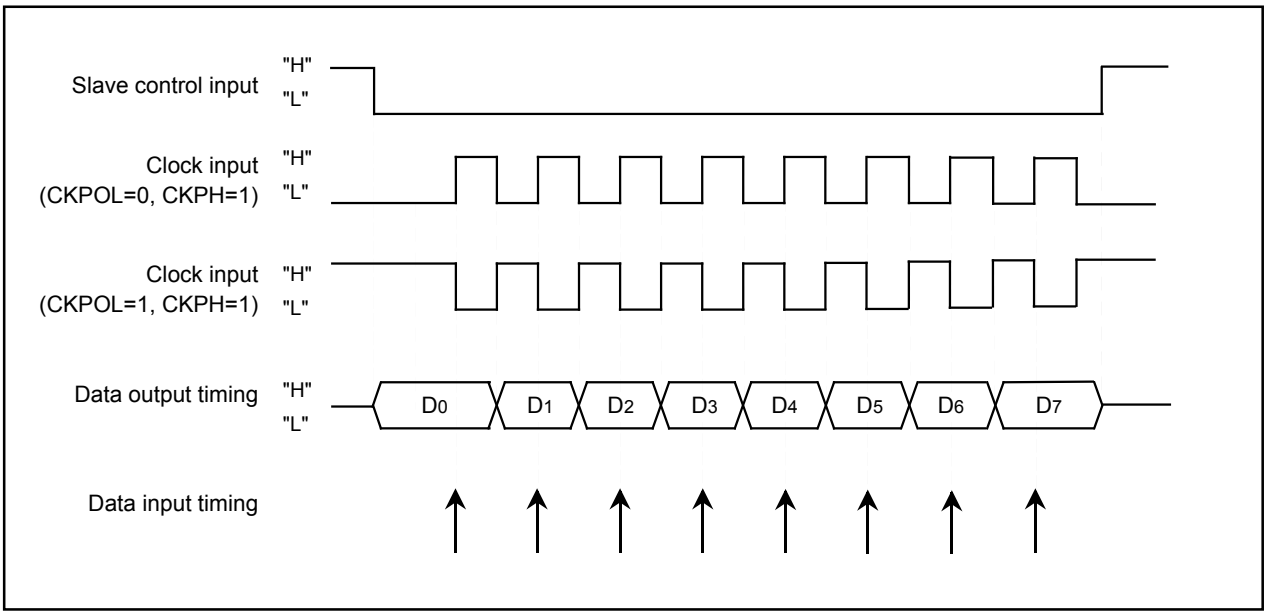


Figure 14.29 Transmission and Reception Timing (CKPH=1) in Slave Mode (External Clock)

15.1.2 Repeat mode

In repeat mode, analog voltage applied to a selected pin is repeatedly converted to a digital code. **Table 15.4** shows the repeat mode specifications. **Figure 15.8** shows the operation example in repeat mode. **Figure 15.9** shows the ADCON0 to ADCON2 registers in repeat mode.

Table 15.4 Repeat Mode Specifications

Item	Specification
Function	Bits CH2 to CH0 in the ADCON0 register and the ADGSEL1 to ADGSEL0 bits in the ADCON2 register select pins. Analog voltage applied to a selected pin is repeatedly converted to a digital code
A/D Conversion Start Condition	• When the TRG bit in the ADCON0 register is 0 (software trigger) Set the ADST bit in the ADCON0 register to 1 (A/D conversion started) • When the TRG bit in the ADCON0 register is 1 (hardware trigger) The $\overline{\text{ADTRG}}$ pin input changes state from “H” to “L” after setting the ADST bit to 1 (A/D conversion started)
A/D Conversion Stop Condition	Set the ADST bit to 0 (A/D conversion halted)
Interrupt Request Generation Timing	None generated
Analog Input Pin	Select one pin from AN_0 to AN_7, $AN0_0$ to $AN0_7$, $AN2_0$ to $AN2_7$, and $AN3_0$ to $AN3_2$
Readout of A/D Conversion Result	Readout one of the AD0 to AD7 registers that corresponds to the selected pin

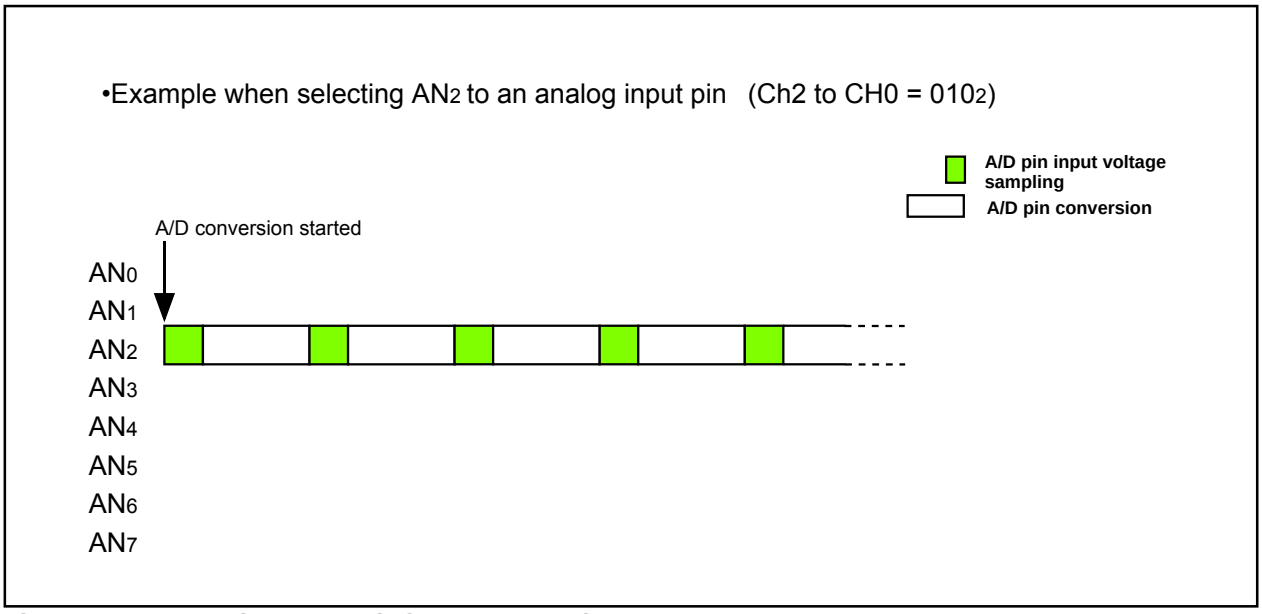


Figure 15.8 Operation Example in Repeat Mode

16.6 I2C0 Control Register 1 (S3D0 register)

The S3D0 register controls the I2C bus interface circuit.

16.6.1 Bit 0 : Interrupt Enable Bit by STOP Condition (SIM)

The SIM bit enables the I2C bus interface interrupt request by detecting a STOP condition. If the SIM bit is set to 1, the I2C bus interface interrupt request is generated by the STOP condition detect (no need to change in the PIN flag).

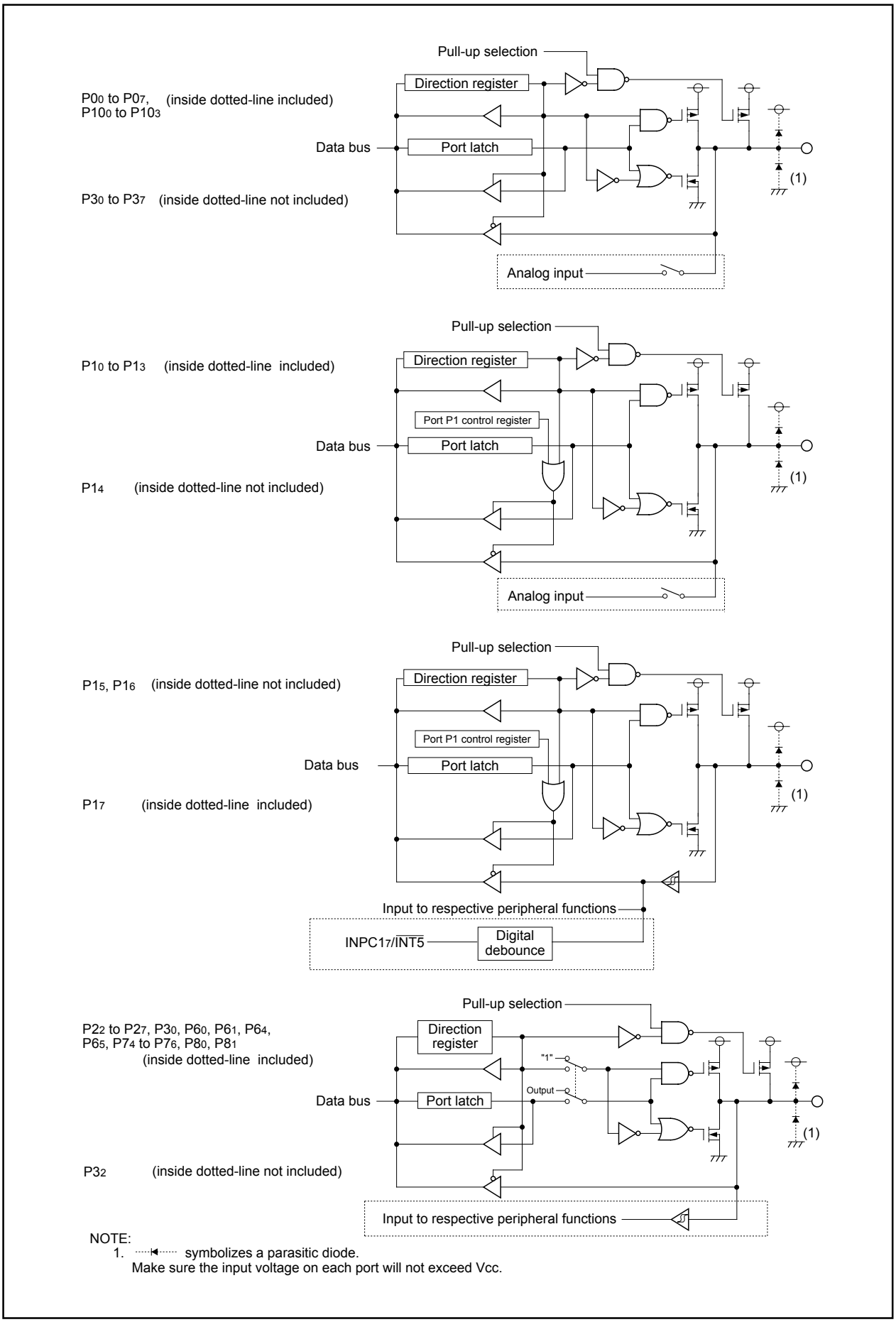
16.6.2 Bit 1: Interrupt Enable Bit at the Completion of Data Receive (WIT)

If the WIT bit is set to 1 while the ACK-CLK bit in the S20 register is set to 1 (ACK clock), the I2C bus interface interrupt request is generated and the PIN bit is set to 1 at the falling edge of the last data bit clock. Then an "L" signal is applied to the SCLMM and the ACK clock generation is controlled. **Table 16.4** and **Figure 16.12** show the interrupt generation timing and the procedure of communication restart. After the communication is restarted, the PIN bit is set to 0 again, synchronized with the falling edge of the ACK clock, and the I2C bus interface interrupt request is generated.

Table16.4 Timing of Interrupt Generation in Data Receive Mode

I2C bus Interface Interrupt Generation Timing	Procedure of Communication Restart
1) Synchronized with the falling edge of the last data bit clock	Set the ACK bit in the S20 register. Set the PIN bit to 1. (Do not write to the S00 register. The ACK clock operation may be unstable.)
2) Synchronized with the falling edge of the ACK clock	Set the S00 register

The internal WAIT flag can be read by reading the WIT bit. The internal WAIT flag is set to 1 after writing data to the S00 register and it is set to 0 after writing to the S20 register.
Consequently, the I2C bus interface interrupt request generated by the timing 1) or 2) can be determined. (See **Figure 16.12**)
When the data is transmitted and the address data is received immediately after the START condition, the WAIT flag remains 0 regardless of the WIT bit setting, and the I2C bus interface interrupt request is only generated at the falling edge of the ACK clock. Set the WIT bit to 0 when the ACK-CLK bit in the S20 register is set to 0 (no ACK clock).



NOTE:
1. ⋯◂⋯ symbolizes a parasitic diode.
Make sure the input voltage on each port will not exceed Vcc.

Figure 19.1 I/O Ports (1)

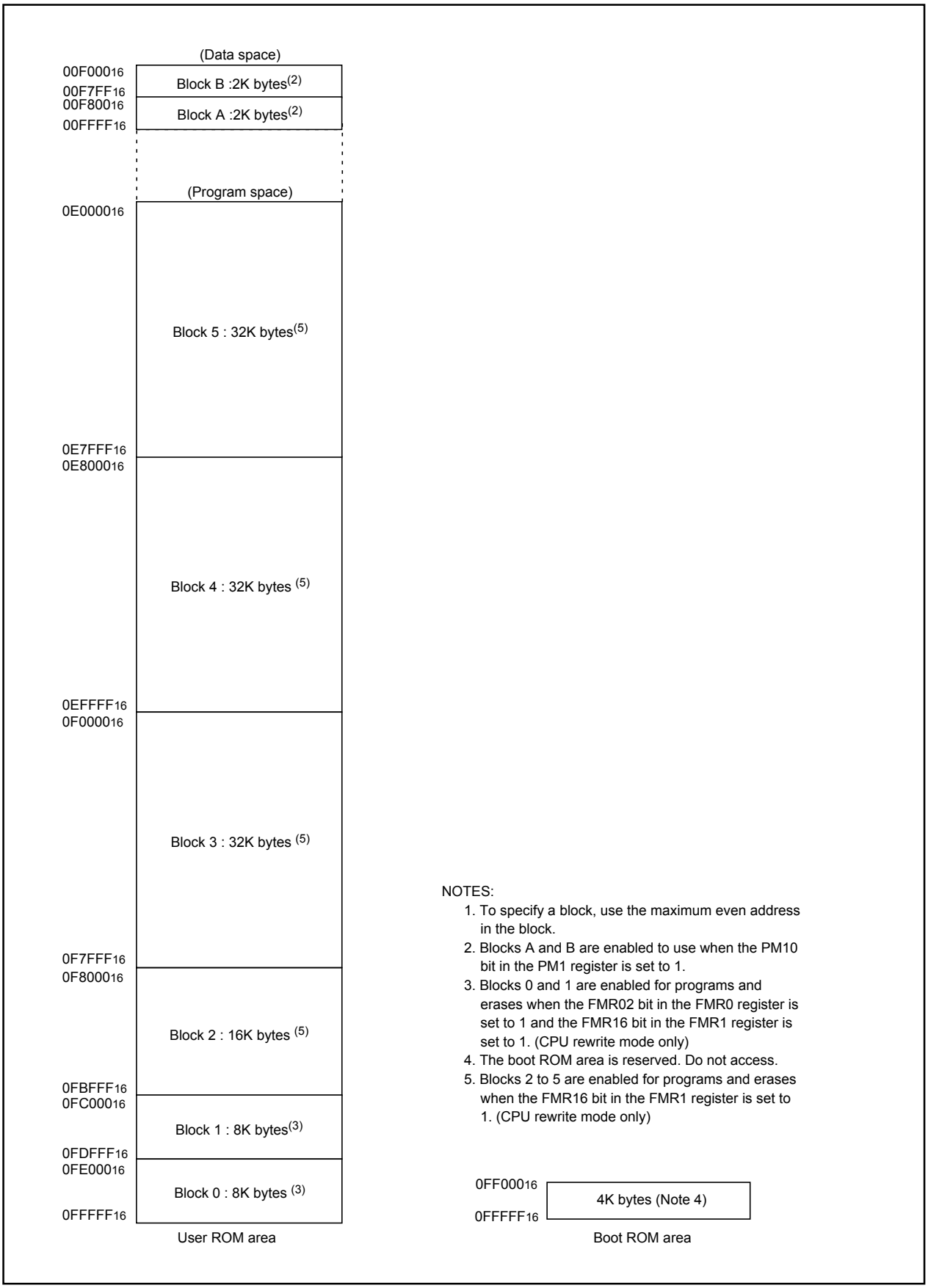


Figure 20.3 Flash Memory Block Diagram (ROM capacity 128 Kbytes)

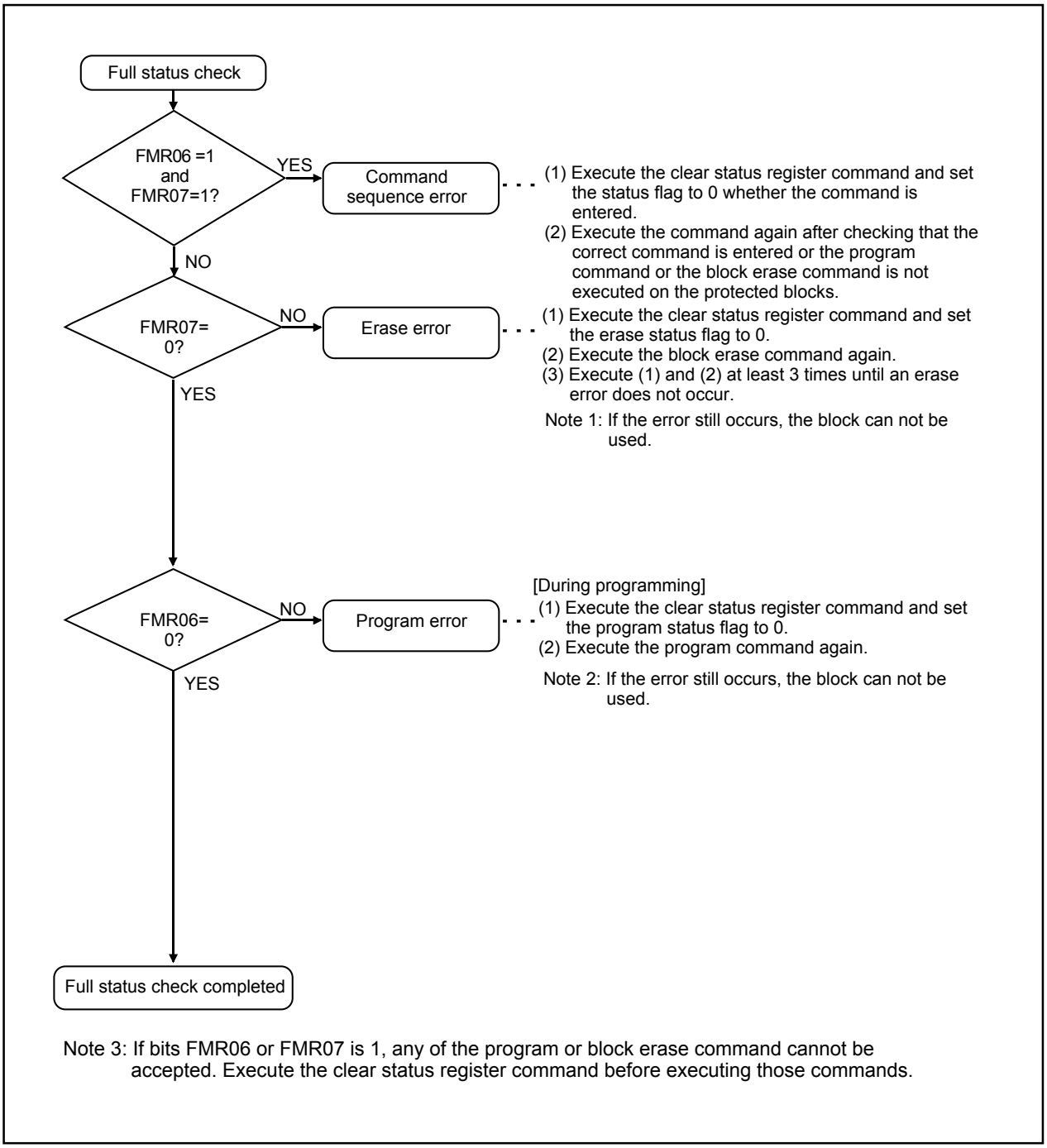


Figure 20.14 Full Status Check and Handling Procedure for Each Error

VCC = 5V

Timing Requirements

(VCC=5V, VSS=0V, at Topr=-40 to 125°C unless otherwise specified)

Table 21.93 Timer B Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN Input Cycle Time (counted on one edge)	100		ns
$t_{w(TBH)}$	TBiIN Input High ("H") Width (counted on one edge)	40		ns
$t_{w(TBL)}$	TBiIN Input Low ("L") Width (counted on one edge)	40		ns
$t_{c(TB)}$	TBiIN Input Cycle Time (counted on both edges)	200		ns
$t_{w(TBH)}$	TBiIN Input High ("H") Width (counted on both edges)	80		ns
$t_{w(TBL)}$	TBiIN Input Low ("L") Width (counted on both edges)	80		ns

Table 21.94 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN Input Cycle Time	400		ns
$t_{w(TBH)}$	TBiIN Input High ("H") Width	200		ns
$t_{w(TBL)}$	TBiIN Input Low ("L") Width	200		ns

Table 21.95 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN Input Cycle Time	400		ns
$t_{w(TBH)}$	TBiIN Input High ("H") Width	200		ns
$t_{w(TBL)}$	TBiIN Input Low ("L") Width	200		ns

Table 21.96 A/D Trigger Input

Symbol	Parameter	Standard		Unit
		Min.	Max	
$t_{c(AD)}$	$\overline{ADTRG}$ Input Cycle Time (required for trigger)	1000		ns
$t_{w(ADL)}$	$\overline{ADTRG}$ Input Low ("L") Width	125		ns

Table 21.97 Serial I/O

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi Input Cycle Time	200		ns
$t_{w(CKH)}$	CLKi Input High ("H") Width	100		ns
$t_{w(CKL)}$	CLKi Input Low ("L") Width	100		ns
$t_{d(C-Q)}$	TxDi Output Delay Time		80	ns
$t_{h(C-Q)}$	TxDi Hold Time	0		ns
$t_{su(D-C)}$	RxDi Input Setup Time	70		ns
$t_{h(C-Q)}$	RxDi Input Hold Time	90		ns

Table 21.98 External Interrupt $\overline{INTi}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ Input High ("H") Width	250		ns
$t_{w(INL)}$	$\overline{INTi}$ Input Low ("L") Width	250		ns

Vcc = 5V

Timing Requirements

(Vcc=5V, Vss=0V, at Topr=-40 to 125°C unless otherwise specified)

Table 21.99 Multi-master I²C Bus Line

Symbol	Parameter	Standard clock mode		High-speed clock mode		Unit
		Min.	Max.	Min.	Max.	
tBUF	Bus free time	4.7		1.3		µs
tHD;STA	The hold time in start condition	4.0		0.6		µs
tLOW	The hold time in SCL clock "0" status	4.7		1.3		µs
tR	SCL, SDA signals' rising time		1000	20+0.1Cb	300	ns
tHD;DAT	Data hold time	0		0	0.9	µs
tHIGH	The hold time in SCL clock "1" status	4.0		0.6		µs
tF	SCL, SDA signals' falling time		300	20+0.1Cb	300	ns
tsu;DAT	Data setup time	250		100		ns
tsu;STA	The setup time in restart condition	4.7		0.6		µs
tsu;STO	Stop condition setup time	4.0		0.6		µs

22.3 Protection

Set the PRC2 bit to 1 (write enabled) and then write to any address, and the PRC2 bit will be cleared to 0 (write protected). The registers protected by the PRC2 bit should be changed in the next instruction after setting the PRC2 bit to 1. Make sure no interrupts or DMA transfers will occur between the instruction in which the PRC2 bit is set to 1 and the next instruction.

Rev.	Date	Description	
		Page	Summary
		329	• **Table 19.1 Unassigned Pin Handling in Single-chip Mode** Note 5 added
			Flash Memory Version
		330	• **20.1 Flash Memory Performance** Description partially deleted
			• **Table 20.14 Flash Memory Version Specifications** Note 3 added
		331	• **20.1.1 Boot Mode** added
		332	• **20.2 Memory Map** Description is modified
		335	• **20.3.1 ROM Code Protect Function** Description is modified
		336	• **Figure 20.4 ROMCP Address** is modified
		337	• **Table 20.3 EW Mode 0 and EW Mode 1** Note 2 is modified
		339	• **20.5.1 Flash Memory Control Register 0 FMR01 Bit** and **FMR02 Bit**: description is modified
		340	• **20.5.2 Flash Memory Control Register 1 (FMR1) FMR6 Bit i**s modified, **FMR17 Bit** is modified
		341	• **Figure 20.6 FMR0 and FMR1 Registers** FMR0 register: note 3 modified, value after reset modified; FMR1 register: note 3 modified, reserved bit map modified
		342	• **Figure 20.7 FMR4 Register** Note 2 is modified
		345	• **20.6.3 Interrupts** EW1 mode modified
			• **20.6.4 How to Access** FMR16 bit is added
		346	• **20.6.9 Stop Mode** modified
		352	• **Table 20.7 Errors and FMR0 Register Status** Register name modified
		355	• **Table 20.8 Pin Functions** Pin settings are partially modified
			Electrical Characteristics
			• **V version is newly added**
		366	• **Table 21.1 Absolute Maximum Ratings** Parameters of Pd and Topr are modified
		367	• **Table 21.2 Recommended Operating Conditions** V_{IH} and V_{IL} are modified
		368	• **Table 21.3 A/D Conversion Characeristics** t_{SAMP} deleted, note 4 added
		369	• **Table 21.4 Flash Memory Version Electrical Characteristics:** Standard values of Program and Erase Endrance cycle modified, tps added
			• **Table 21.5 Flash Memory Version Electrical Characteristics:** tps added, data hold time added, note 1, 3, 8 modified, note 11 and 12 added
		370	• **Table 21.6 Low Voltage Detection Circuit Electrical Characteristics** Note 4 added
			• **Table 21.7 Power Supply Circuit from Timing CharacteristicsL** Note 2 & 3 are deleted, figure modified
		372	• **Table 21.9 Electrical Characteristics(2)** Note 5 is added
		380	• **Table 21.25 Electrical Characteristics(2)** Note 5 is added
		387	• **Table 21.40 Absolute Maximum Ratings** Parameters of Pd and Topr are modified