Renesas Electronics America Inc - M30290FCTHP#U7A Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	M16C/60
Core Size	16-Bit
Speed	20MHz
Connectivity	CANbus, I²C, IEBus, SIO, UART/USART
Peripherals	DMA, POR, PWM, Voltage Detect, WDT
Number of I/O	71
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 27x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30290fcthp-u7a

1.5 Pin Description

Table 1.14 Pin Description (64-pin and 80-pin packages)

Classification	Symbol	I/O Type	Function
Power supply	VCC, VSS	I	Apply 0V to the Vss pin. Apply following voltage to the Vcc pin. 2.7 to 5.5 V (Normal), 3.0 to 5.5 V (T-ver.), 4.2 to 5.5 V (V-ver.)
Analog power supply	AVCC AVSS	I	Supplies power to the A/D converter. Connect the AVCC pin to VCC and the AVSS pin to VSS
Reset input	$\overline{\text{RESET}}$	I	The microcomputer is in a reset state when "L" is applied to the $\overline{\text{RESET}}$ pin
CNVSS	CNVSS	I	Connect the CNVSS pin to VSS
Main clock input	XIN	I	I/O pins for the main clock oscillation circuit. Connect a ceramic resonator or crystal oscillator between XIN and XOUT. To apply external clock, apply it to XIN and leave XOUT open. If XIN is not used (for external oscillator or external clock) connect XIN pin to VCC and leave XOUT open
Main clock output	XOUT	O	
Sub clock input	XCIN	I	I/O pins for the sub clock oscillation circuit. Connect a crystal oscillator between XCIN and XCOUT
Sub clock output	XCOUT	O	
Clock output	CLKOUT	O	Outputs the clock having the same frequency as f1, f8, f32, or fC
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}$ to $\overline{\text{INT5}}$	I	Input pins for the $\overline{\text{INT}}$ interrupt. $\overline{\text{INT2}}$ can be used for Timer A Z-phase function
$\overline{\text{NMI}}$ interrupt input	$\overline{\text{NMI}}$	I	Input pin for the $\overline{\text{NMI}}$ interrupt. $\overline{\text{NMI}}$ cannot be used as I/O port while the three-phase motor control is enabled. Apply a stable "H" to $\overline{\text{NMI}}$ after setting it's direction register to "0" when the three-phase motor control is enabled
Key input interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	Input pins for the key input interrupt
Timer A	TA0OUT to TA4OUT	I/O	I/O pins for the timer A0 to A4
	TA0IN to TA4IN	I	Input pins for the timer A0 to A4
	ZP	I	Input pin for Z-phase
Timer B	TB0IN to TB2IN	I	Input pins for the timer B0 to B2
Three-phase motor control timer output	U, $\overline{\text{U}}$, V, $\overline{\text{V}}$, W, $\overline{\text{W}}$	O	Output pins for the three-phase motor control timer
	IDU, IDW, IDV, $\overline{\text{SD}}$	I/O	Input and output pins for the three-phase motor control timer
Serial I/O	$\overline{\text{CTS0}}$ to $\overline{\text{CTS2}}$	I	Input pins for data transmission control
	$\overline{\text{RTS0}}$ to $\overline{\text{RTS2}}$	O	Output pins for data reception control
	CLK0 to CLK3	I/O	Inputs and outputs the transfer clock
	RxD0 to RxD2	I	Inputs serial data
	SIN3	I	Inputs serial data
	TxD0 to TxD2	O	Outputs serial data
	SOUT3	O	Outputs serial data
	CLKS1	O	Output pin for transfer clock
I^2C bus Mode	SDA2	I/O	Inputs and outputs serial data
	SCL2		Inputs and outputs the transfer clock
Multi-master I^2C bus	SDAMM	I/O	Inputs and outputs serial data
	SCLMM		Inputs and outputs the transfer clock
Reference voltage input	VREF	I	Applies reference voltage to the A/D converter
A/D converter	AN0 to AN7 AN00 to AN03 AN24 AN30 to AN32	I	Analog input pins for the A/D converter
	$\overline{\text{ADTRG}}$	I	Input pin for an external A/D trigger

I: Input O: Output I/O: Input and output

Table 4.6 SFR Information (6)

Address	Register	Symbol	After reset
0140₁₆	CAN0 message box 14: Identifier/DLC		XX₁₆
0141₁₆			XX₁₆
0142₁₆			XX₁₆
0143₁₆			XX₁₆
0144₁₆			XX₁₆
0145₁₆			XX₁₆
0146₁₆	CAN0 message box 14 : Data field		XX₁₆
0147₁₆			XX₁₆
0148₁₆			XX₁₆
0149₁₆			XX₁₆
014A₁₆			XX₁₆
014B₁₆			XX₁₆
014C₁₆			XX₁₆
014D₁₆			XX₁₆
014E₁₆	CAN0 message box 14 : Time stamp		XX₁₆
014F₁₆			XX₁₆
0150₁₆	CAN0 message box 15 : Identifier/DLC		XX₁₆
0151₁₆			XX₁₆
0152₁₆			XX₁₆
0153₁₆			XX₁₆
0154₁₆			XX₁₆
0155₁₆			XX₁₆
0156₁₆	CAN0 message box 15 : Data field		XX₁₆
0157₁₆			XX₁₆
0158₁₆			XX₁₆
0159₁₆			XX₁₆
015A₁₆			XX₁₆
015B₁₆			XX₁₆
015C₁₆			XX₁₆
015D₁₆			XX₁₆
015E₁₆	CAN0 message box 15 : Time stamp		XX₁₆
015F₁₆			XX₁₆
0160₁₆	CAN0 global mask register	C0GMR	XX₁₆
0161₁₆			XX₁₆
0162₁₆			XX₁₆
0163₁₆			XX₁₆
0164₁₆			XX₁₆
0165₁₆			XX₁₆
0166₁₆	CAN0 local mask A register	C0LMAR	XX₁₆
0167₁₆			XX₁₆
0168₁₆			XX₁₆
0169₁₆			XX₁₆
016A₁₆			XX₁₆
016B₁₆			XX₁₆
016C₁₆	CAN0 local mask B register	C0LMBR	XX₁₆
016D₁₆			XX₁₆
016E₁₆			XX₁₆
016F₁₆			XX₁₆
0170₁₆			XX₁₆
0171₁₆			XX₁₆
≈			≈
01B3₁₆	Flash memory control register 4 (Note 2)	FMR4	0100000X₂
01B4₁₆			
01B5₁₆	Flash memory control register 1 (Note 2)	FMR1	000XXX0X₂
01B6₁₆			
01B7₁₆	Flash memory control register 0 (Note 2)	FMR0	01₁₆
≈			≈
01FD₁₆			
01FE₁₆			
01FF₁₆			

Note 1: The blank areas are reserved and cannot be used by users.
Note 2: This register is included in the flash memory version.

X : Undefined

5.5 Voltage Detection Circuit

Note

VCC = 5 V is assumed in **5.5 Voltage Detection Circuit**.

Voltage detection circuit in the M16C/29 Group, T-ver. and V-ver. cannot be used.

The voltage detection circuit has the reset level detection circuit and the low voltage detection circuit. The reset level detection circuit monitors the voltage applied to the VCC pin. The MCU is reset if the reset level detection circuit detects VCC is Vdet3 or below. Use bits VC27 and VC26 in the VCR2 register to determine whether the individual circuit is enabled.

Use the reset level detection circuit for brown-out detection reset.

The low voltage detection circuit also monitors the voltage applied to the VCC pin. The low voltage detection circuit use the VC13 bit in the VCR1 register to detect VCC is above or below Vdet4. The low voltage detection interrupt can be used in the voltage detection circuit.

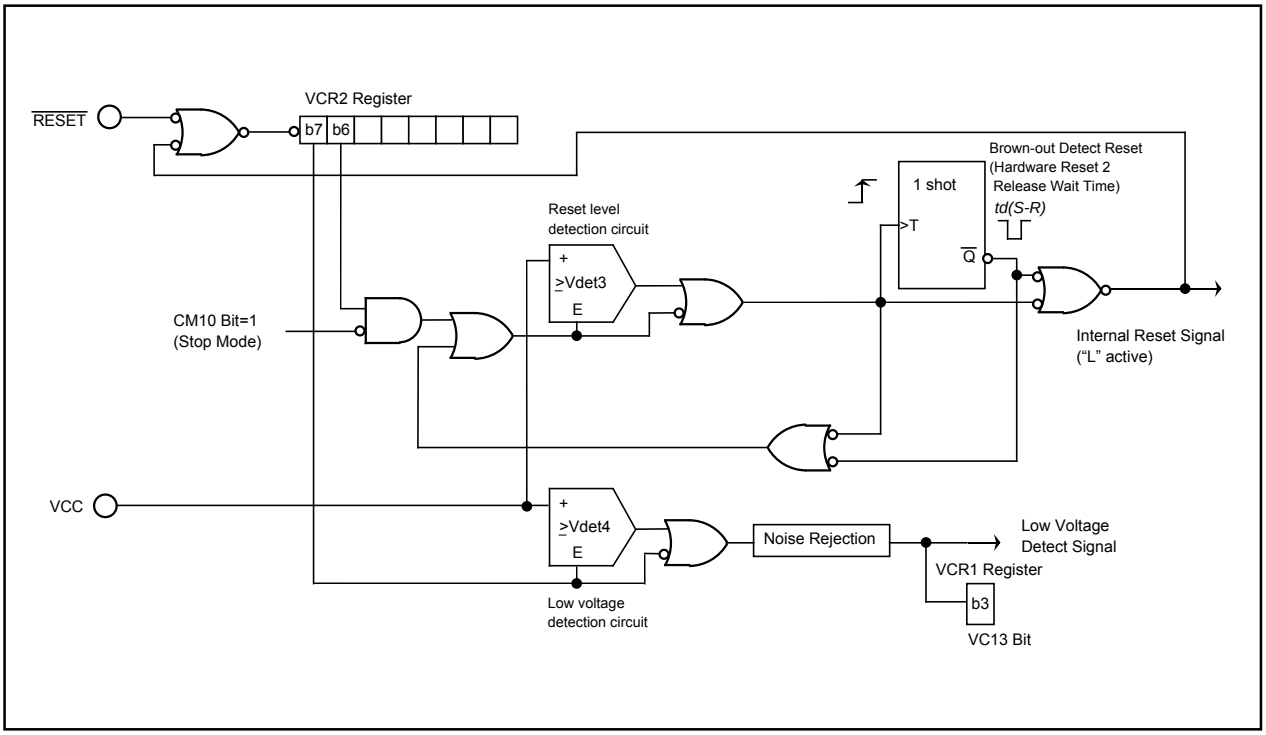


Figure 5.4 Voltage Detection Circuit Block

12.1.2 Event Counter Mode

In event counter mode, the timer counts pulses from an external device or overflows and underflows of other timers. Timers A2, A3, and A4 can count two-phase external signals. **Table 12.2** lists specifications in event counter mode (when not processing two-phase pulse signal). **Table 12.3** lists specifications in event counter mode (when processing two-phase pulse signal with the timers A2, A3 and A4). **Figure 12.8** shows TAiMR register in event counter mode (when not processing two-phase pulse signal). **Figure 12.9** shows TA2MR to TA4MR registers in event counter mode (when processing two-phase pulse signal with the timers A2, A3 and A4).

Table 12.2 Specifications in Event Counter Mode (when not processing two-phase pulse signal)

Item	Specification
Count source	• External signals input to TAiIN pin (i=0 to 4) (effective edge can be selected in program) • Timer B2 overflows or underflows, timer Aj (j=i-1, except j=4 if i=0) overflows or underflows, timer Ak (k=i+1, except k=0 if i=4) overflows or underflows
Count operation	• Increment or decrement can be selected by external signal or program • When the timer overflows or underflows, it reloads the reload register contents and continues counting. When operating in free-running mode, the timer continues counting without reloading.
Divided ratio	1/ (FFFF16 - n + 1) for increment 1/ (n + 1) for down-count n : set value of TAi register 000016 to FFFF16
Count start condition	Set TAiS bit in the TABSR register to 1 (start counting)
Count stop condition	Set TAiS bit to 0 (stop counting)
Interrupt request generation timing	Timer overflow or underflow
TAiIN pin function	I/O port or count source input
TAiOUT pin function	I/O port, pulse output, or up/down-count select input
Read from timer	Count value can be read by reading TAi register
Write to timer	• When not counting and until the 1st count source is input after counting start Value written to TAi register is written to both reload register and counter • When counting (after 1st count source input) Value written to TAi register is written to only reload register (Transferred to counter when reloaded next)
Select function	• Free-run count function Even when the timer overflows or underflows, the reload register content is not reloaded to it • Pulse output function Whenever the timer underflows or underflows, the output polarity of TAiOUT pin is inverted . When not counting, the pin outputs a low.

Timer Ai Mode Register (i=2 to 4)
(When using two-phase pulse signal processing)

b6	b5	b4	b3	b2	b1	b0
		0	1	0	0	0	1

Symbol	Address	After Reset
TA2MR to TA4MR	0398_{16} to $039A_{16}$	00_{16}

Bit Symbol	Bit Name	Function	RW
TMOD0	Operation mode select bit	$^{b1\ b0}$ 0 1: Event counter mode	RW
TMOD1			RW
MR0	To use two-phase pulse signal processing, set this bit to 0		RW
MR1	To use two-phase pulse signal processing, set this bit to 0		RW
MR2	To use two-phase pulse signal processing, set this bit to 1		RW
MR3	To use two-phase pulse signal processing, set this bit to 0		RW
TCK0	Count operation type select bit	0: Reload type 1: Free-run type	RW
TCK1	Two-phase pulse signal processing operation select bit (1)(2)	0: Normal processing operation 1: Multiply-by-4 processing operation	RW

NOTES:
1. The TCK1 bit is valid for timer A3 mode register. No matter how this bit is set, timers A2 and A4 always operate in normal processing mode and x4 processing mode, respectively.
2. If two-phase pulse signal processing is desired, following register settings are required:
   - Set the TAiP bit in the UDF register to 1 (two-phase pulse signal processing function enabled).
   - Set bits TAiTGH and TAiTGL in the TRGSR register to 00_2 (TAiIN pin input).
   - Set the port direction bits for TAiIN and TAiOUT to 0 (input mode).

Figure 12.9 TA2MR to TA4MR Registers in Event Counter Mode (when using two-phase pulse signal processing with timer A2, A3 or A4)

12.1.4 Pulse Width Modulation (PWM) Mode

In PWM mode, the timer outputs pulses of a given width in succession (see **Table 12.5**). The counter functions as either 16-bit pulse width modulator or 8-bit pulse width modulator. **Figure 12.12** shows TAiMR register in pulse width modulation mode. **Figures 12.13** and **12.14** show examples of how a 16-bit pulse width modulator operates and how an 8-bit pulse width modulator operates.

Table 12.5 Specifications in Pulse Width Modulation Mode

Item	Specification
Count source	f_1, f_2, f_8, f_{32}, f_{C32}
Count operation	• Decrement (operating as an 8-bit or a 16-bit pulse width modulator) • The timer reloads a new value at a rising edge of PWM pulse and continues counting • The timer is not affected by a trigger that occurs during counting
16-bit PWM	• High level width n / fj n : set value of TAi register (i=o to 4) • Cycle time $(2^{16}-1)$ / fj fixed fj: count source frequency (f_1, f_2, f_8, f_{32}, f_{C32})
8-bit PWM	• High level width n x (m+1) / fj n : set value of TAi register high-order address • Cycle time (2^8-1) x (m+1) / fj m : set value of TAi register low-order address
Count start condition	• TAiS bit in the TABSR register is set to 1 (= start counting) • The TAiS bit = 1 and external trigger input from the TAiIN pin • The TAiS bit = 1 and one of the following external triggers occurs • Timer B2 overflow or underflow, timer Aj (j=i-1, except j=4 if i=0) overflow or underflow, timer Ak (k=i+1, except k=0 if i=4) overflow or underflow
Count stop condition	TAiS bit is set to 0 (stop counting)
Interrupt request generation timing	PWM pulse goes “L”
TAiIN pin function	I/O port or trigger input
TAiOUT pin function	Pulse output
Read from timer	An undefined value is read by reading TAi register
Write to timer	• When not counting and until the 1st count source is input after counting start Value written to TAi register is written to both reload register and counter • When counting (after 1st count source input) Value written to TAi register is written to only reload register (Transferred to counter when reloaded next)

12.2.3 Pulse Period and Pulse Width Measurement Mode

In pulse period and pulse width measurement mode, the timer measures pulse period or pulse width of an external signal (see **Table 12.8**). **Figure 12.20** shows the TBiMR register in pulse period and pulse width measurement mode. **Figure 12.21** shows the operation timing when measuring a pulse period. **Figure 12.22** shows the operation timing when measuring a pulse width.

Table 12.8 Specifications in Pulse Period and Pulse Width Measurement Mode

Item	Specification
Count source	f_1, f_2, f_8, f_{32}, f_{C32}
Count operation	• Increment • Counter value is transferred to reload register at an effective edge of measurement pulse. The counter value is set to 0000_{16} to continue counting.
Count start condition	Set TBiS (i=0 to 2) bit (3) to 1 (start counting)
Count stop condition	Set TBiS bit to 0 (stop counting)
Interrupt request generation timing	• When an effective edge of measurement pulse is input (1) • Timer overflow. When an overflow occurs, MR3 bit in the TBiMR register is set to 1 (overflowed) simultaneously. MR3 bit is cleared to 0 (no overflow) by writing to TBiMR register at the next count timing or later after MR3 bit was set to 1. At this time, make sure TBiS bit is set to 1 (start counting).
TBi_{IN} pin function	Measurement pulse input
Read from timer	Contents of the reload register (measurement result) can be read by reading TBi register (2)
Write to timer	Value written to TBi register is written to neither reload register nor counter

NOTES:
1. Interrupt request is not generated when the first effective edge is input after the timer started counting.
2. Value read from TBi register is undefined until the second valid edge is input after the timer starts counting.
3. Bits TB0S to TB2S are assigned to the bit 5 to bit 7 in the TABSR register .

Timer Bi Mode Register (i=0 to 2)

b7	b6	b5	b4	b3	b2	b1	b0
						1	0

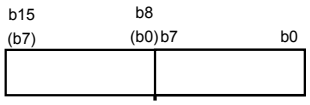
Symbol	Address	After Reset
TB0MR to TB2MR	$039B_{16}$ to $039D_{16}$	$00XX0000_2$

Bit Symbol	Bit Name	Function	RW
TMOD0	Operation mode select bit	b1 b0 1 0 : Pulse period / pulse width measurement mode	RW
TMOD1			RW
MR0	Measurement mode select bit	b3 b2 0 0: Pulse period measurement (Measurement between a falling edge and the next falling edge of measured pulse) 0 1: Pulse period measurement (Measurement between a rising edge and the next rising edge of measured pulse) 1 0: Pulse width measurement (Measurement between a falling edge and the next rising edge of measured pulse and between a rising edge and the next falling edge) 1 1: Do not set.	RW
MR1			RW
MR2	TB0MR register Set to 0 in pulse period and pulse width measurement mode		RW
	TB1MR, TB2MR registers Nothing is assigned. If necessary, set to 0. When read, its content is undefined		—
MR3	Timer Bi overflow flag (1)	0 : Timer did not overflow 1 : Timer has overflowed	RO
TCK0	Count source select bit	b7 b6 0 0: f_1 or f_2 0 1: f_8 1 0: f_{32} 1 1: f_{C32}	RW
TCK1			RW

NOTE:
1.This flag is undefined after reset. When the TBiS bit is set to 1 (start counting), the MR3 bit is cleared to 0 (no overflow) by writing to the TBiMR register at the next count timing or later after the MR3 bit was set to 1 (overflowed). The MR3 bit cannot be set to 1 by program. Bits TB0S to TB2S are assigned to the bit 5 to bit 7 in the TABSR register.

Figure 12.20 TBiMR Register in Pulse Period and Pulse Width Measurement Mode

Waveform Generation Register j (j=0 to 7)



Symbol	Address	After Reset
G1PO0 to G1PO2	0301_{16}-0300_{16}, 0303_{16}-0302_{16}, 0305_{16}-0304_{16}	Undefined
G1PO3 to G1PO5	0307_{16}-0306_{16}, 0309_{16}-0308_{16}, $030B_{16}$-$030A_{16}$	Undefined
G1PO6 to G1PO7	$030D_{16}$-$030C_{16}$, $030F_{16}$-$030E_{16}$	Undefined

Function	Setting Range	RW
• When the RLD bit in the G1POCRj register is set to 0, value written is immediately reloaded into the G1POj register for output, for example, a waveform output,reflecting the value. • When the RLD bit is set to 1, value reloaded while the base timer is reset. The value written can be read until reloaded	0000_{16} to $FFFF_{16}$	RW

Figure 13.7 G1PO0 to G1PO7 Registers

14.1.2.4 Serial Data Logic Switching Function (UART2)

The data written to the U2TB register has its logic reversed before being transmitted. Similarly, the received data has its logic reversed when read from the U2RB register. **Figure 14.19** shows serial data logic.

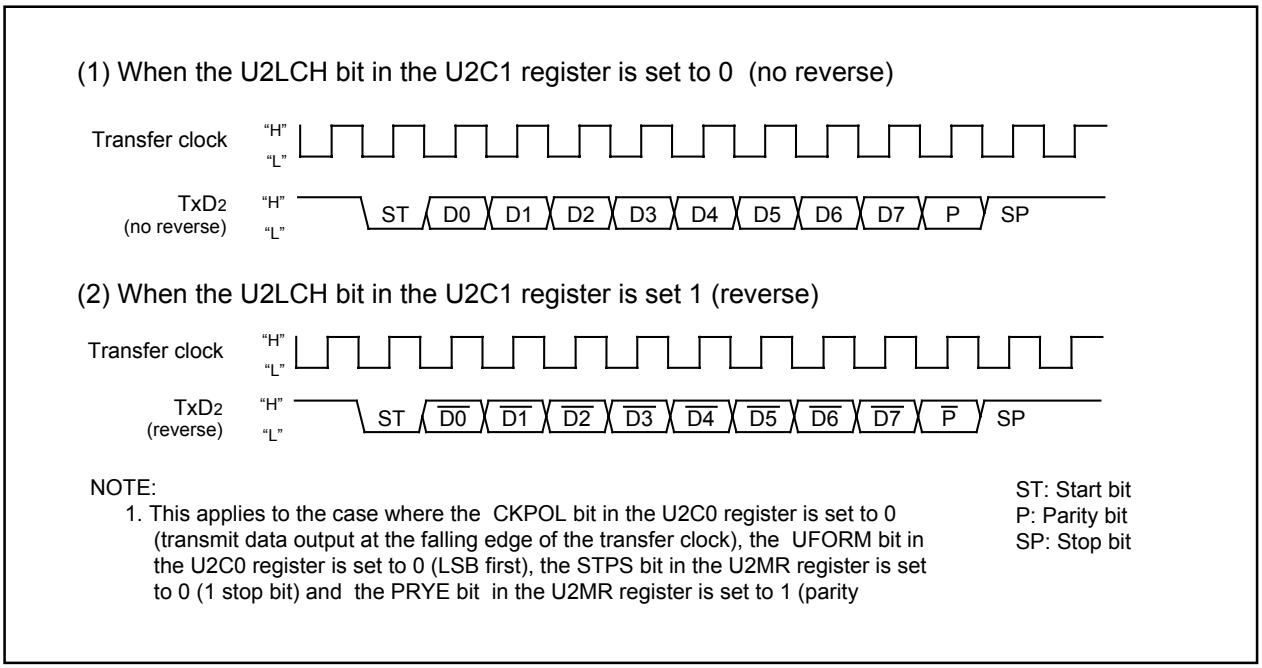


Figure 14.19 Serial Data Logic Switching

14.1.2.5 TxD and RxD I/O Polarity Inverse Function (UART2)

This function inverses the polarities of the TxD2 pin output and RxD2 pin input. The logic levels of all input/output data (including the start, stop and parity bits) are inversed. **Figure 14.20** shows the TxD pin output and RxD pin input polarity inverse.

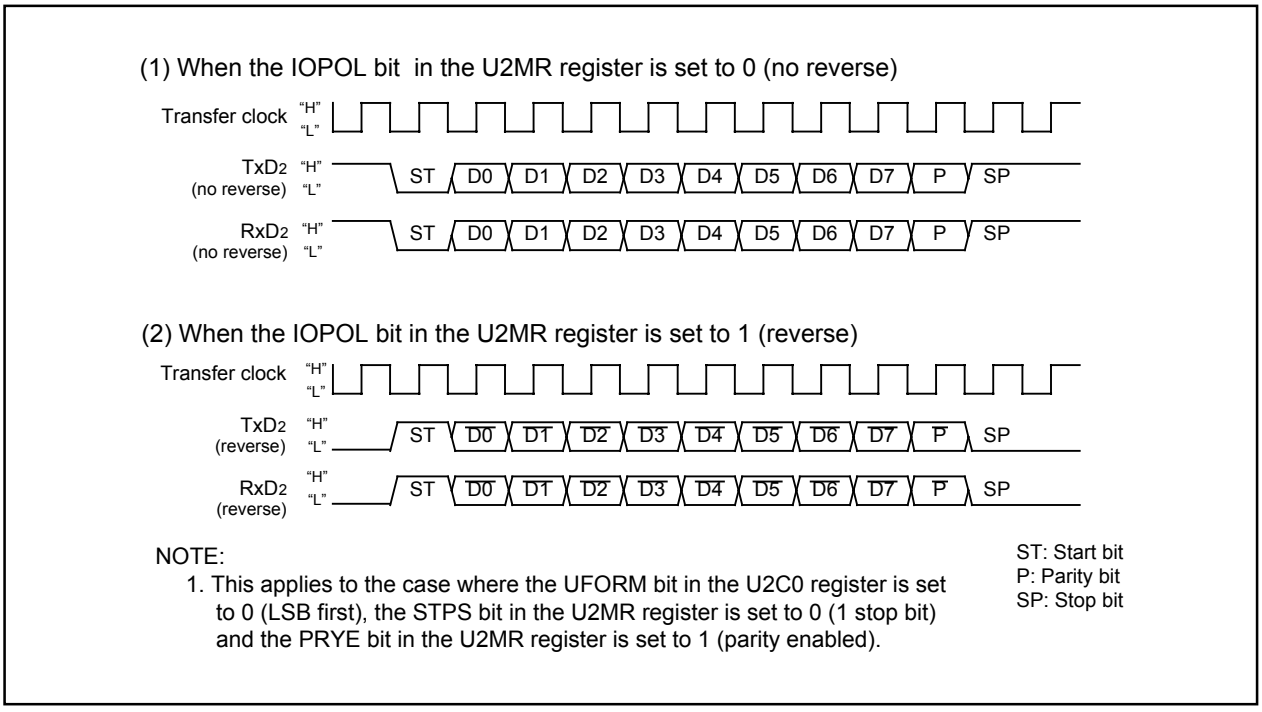


Figure 14.20 TxD and RxD I/O Polarity Inverse

15.5 Output Impedance of Sensor under A/D Conversion

To carry out A/D conversion properly, charging the internal capacitor C shown in **Figure 15.29** has to be completed within a specified period of time. T (sampling time) as the specified time. Let output impedance of sensor equivalent circuit be R0, MCU's internal resistance be R, precision (error) of the A/D converter be X, and the A/D converter's resolution be Y (Y is 1024 in the 10-bit mode, and 256 in the 8-bit mode).

$$\text{VC is generally } VC = VIN\{1-e^{-\frac{1}{C(R0+R)}t}\}$$

$$\text{And when } t = T,\quad VC = VIN - \frac{X}{Y}VIN = VIN\left(1-\frac{X}{Y}\right)$$

$$e^{-\frac{1}{C(R0+R)}T} = \frac{X}{Y}$$

$$-\frac{1}{C(R0+R)}T = \ln\frac{X}{Y}$$

$$\text{Hence,}\quad R0 = -\frac{T}{C\cdot\ln\frac{X}{Y}} - R$$

Figure 15.29 shows analog input pin and externalsensor equivalent circuit. When the difference between VIN and VC becomes 0.1 LSB, we find impedance R0 when voltage between pins. VC changes from 0 to VIN-(0.1/1024) VIN in timer T. (0.1/1024) means that A/D precision drop due to insufficient capacitor chage is held to 0.1LSB at time of A/D conversion in the 10-bit mode. Actual error however is the value of absolute precision added to 0.1LSB. When f(XIN) = 10MHz, T=0.3µs in the A/D conversion mode with sample & hold. Output inpedance R0 for sufficiently charging capacitor C within time T is determined as follows.

T = 0.3µs, R = 7.8kΩ, C = 1.5pF, X = 0.1, and Y = 1024. Hence,

$$R0 = -\frac{0.3\times10^{-6}}{1.5\times10^{-12}\cdot\ln\frac{0.1}{1024}} - 7.8\times10^{3} \cong 13.9\times10^{3}$$

Thus, the allowable output impedance of the sensor circuit capable of thoroughly driving the A/D converter turns out of be approximately 13.9kΩ.

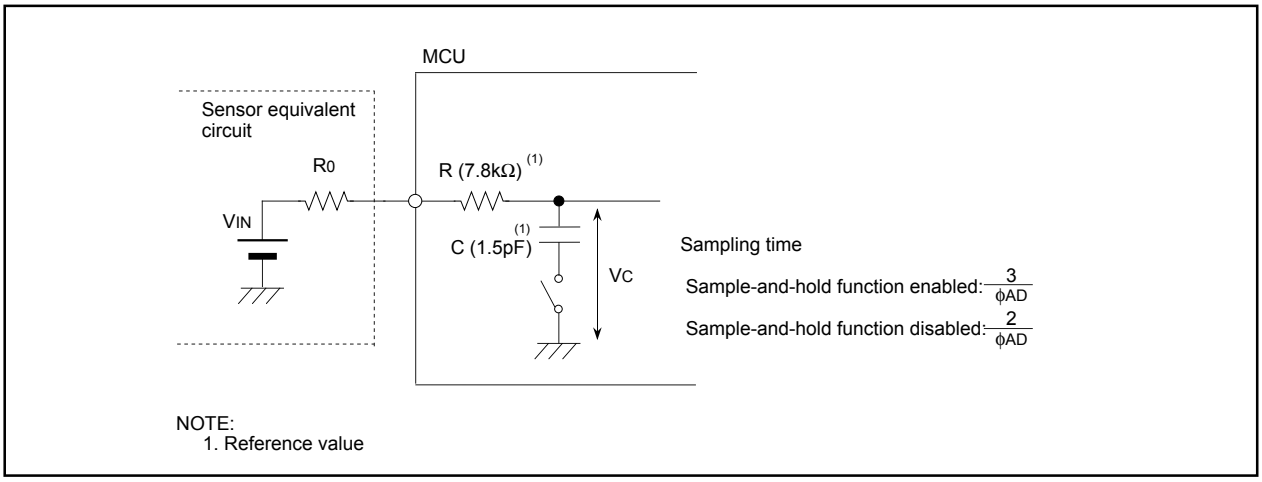


Figure 15.29 Analog Input Pin and External Sensor Equivalent Circuit

16. Multi-master I2C bus Interface

The multi-master I2C bus interface is a serial communication circuit based on Philips I2C bus data transfer format, equipped with arbitration lost detection and synchronous functions. **Figure 16.1** shows a block diagram of the multi-master I2C bus interface and **Table 16.1** lists the multi-master I2C bus interface functions.

The multi-master I2C bus interface consists of the S0D0 register, the S00 register, the S20 register, the S3D0 register, the S4D0 register, the S10 register, the S2D0 register and other control circuits.

Figures 16.2 to **16.8** show the registers associated with the multi-master I2C bus.

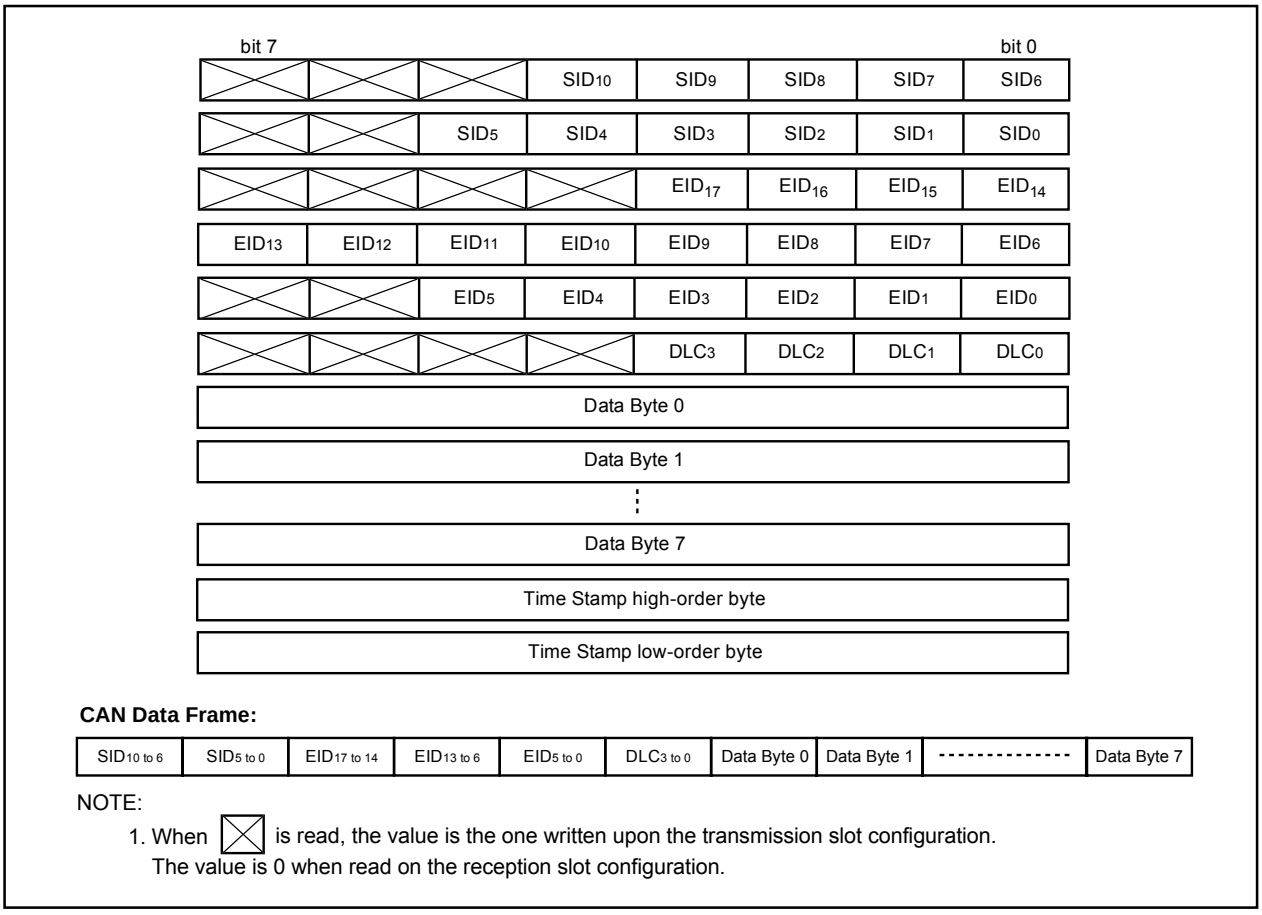
Table 16.1 Multi-master I2C bus interface functions

Item	Function
Format	Based on Philips I2C bus standard: 7-bit addressing format High-speed clock mode Standard clock mode
Communication mode	Based on Philips I2C bus standard: Master transmit Master receive Slave transmit Slave receive
SCL clock frequency	16.1kHz to 400kHz (at VIIC (1)= 4MHz)
I/O pin	Serial data line SDAMM(SDA) Serial clock line SDLMM(SCL)

NOTE:

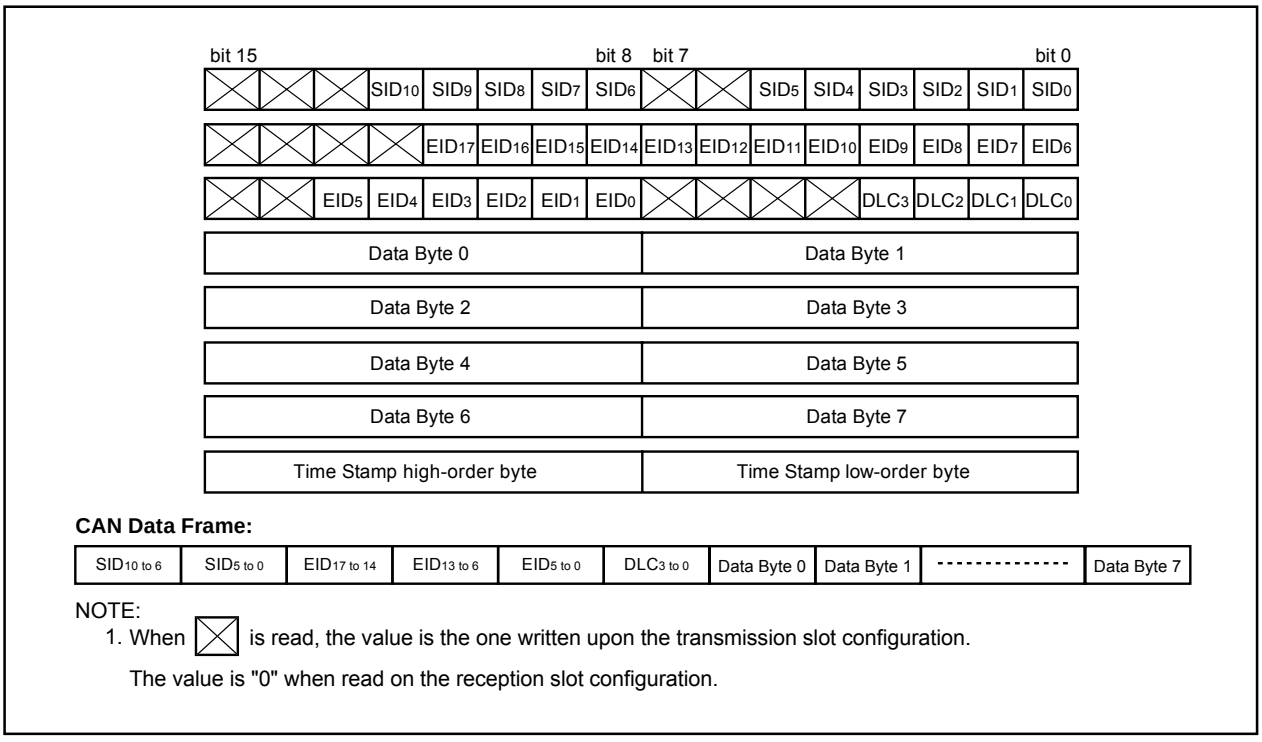
1. VIIC=I2C system clock

Figures 17.2 and **17.3** show the bit mapping in each slot in byte access and word access. The content of each slot remains unchanged unless transmission or reception of a new message is performed.



NOTE:
1. When ☒ is read, the value is the one written upon the transmission slot configuration.
The value is 0 when read on the reception slot configuration.

Figure 17.2 Bit Mapping in Byte Access



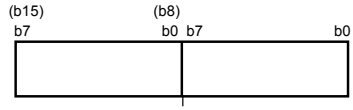
NOTE:
1. When ☒ is read, the value is the one written upon the transmission slot configuration.
The value is "0" when read on the reception slot configuration.

Figure 17.3 Bit Mapping in Word Access

17.1.3.4 C0SSTR Register

Figure 17.9 shows the C0SSTR register.

CAN0 Slot Status Register



Symbol	Address	After Reset
C0SSTR	0215_{16}, 0214_{16}	0000_{16}

Function	Setting Values	RW
Slot status bits Each bit corresponds to the slot with the same number	0: Reception slot The message has been read. Transmission slot Transmission is not completed. 1: Reception slot The message has not been read. Transmission slot Transmission is completed	RO

Figure 17.9 C0SSTR Register

20.11 CAN I/O Mode

Note

The CAN I/O mode is not available in M16C/29 T-ver./V-ver.

In CAN I/O mode, the user ROM area can be rewritten while the MCU is mounted on-board by using a CAN programmer which is applicable for the M16C/29 group. For more information about CAN programmers, contact the manufacturer of your CAN programmer. For details on how to use, refer to the user's manual included with your CAN programmer.
Table 20.9 lists pin functions for CAN I/O mode. Figures 20.19 and 20.20 show pin connections for CAN I/O mode.

20.11.1 ID code check function

This function determines whether the ID codes sent from the CAN programmer and those written in the flash memory match.(Refer to **20.3 Functions To Prevent Flash Memory from Rewriting**.)

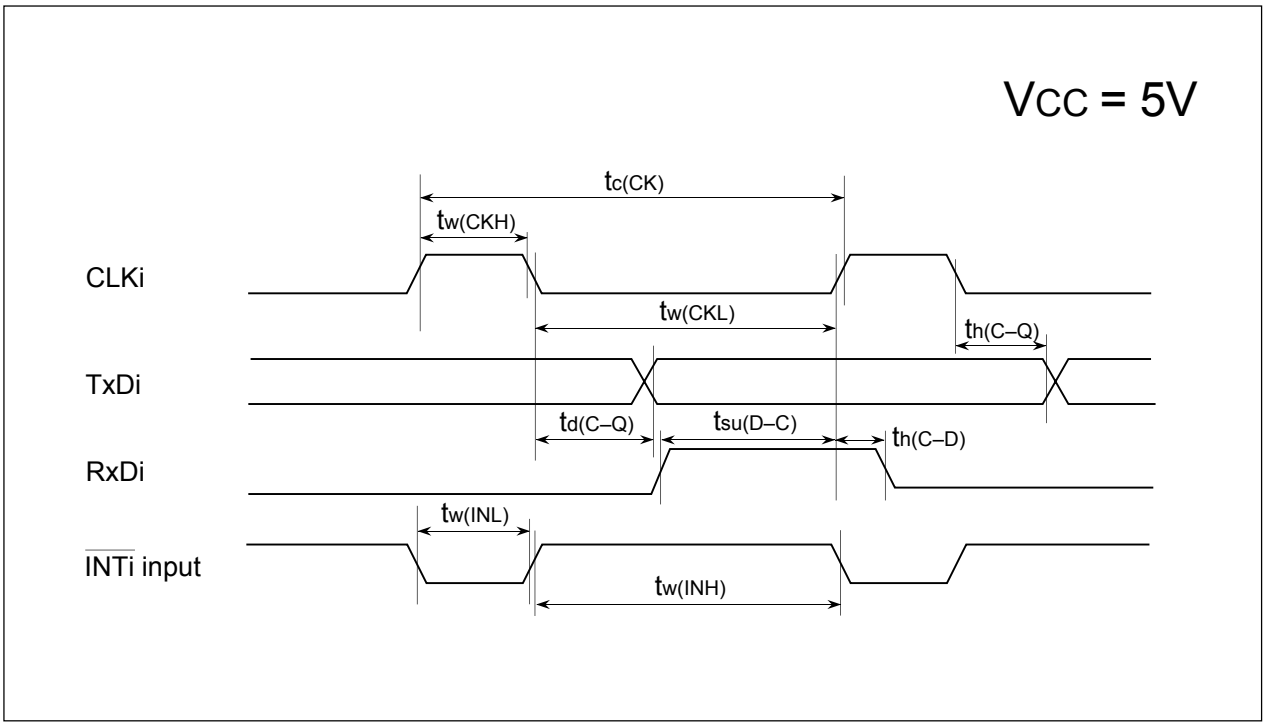


Figure 21.8 Timing Diagram (2)

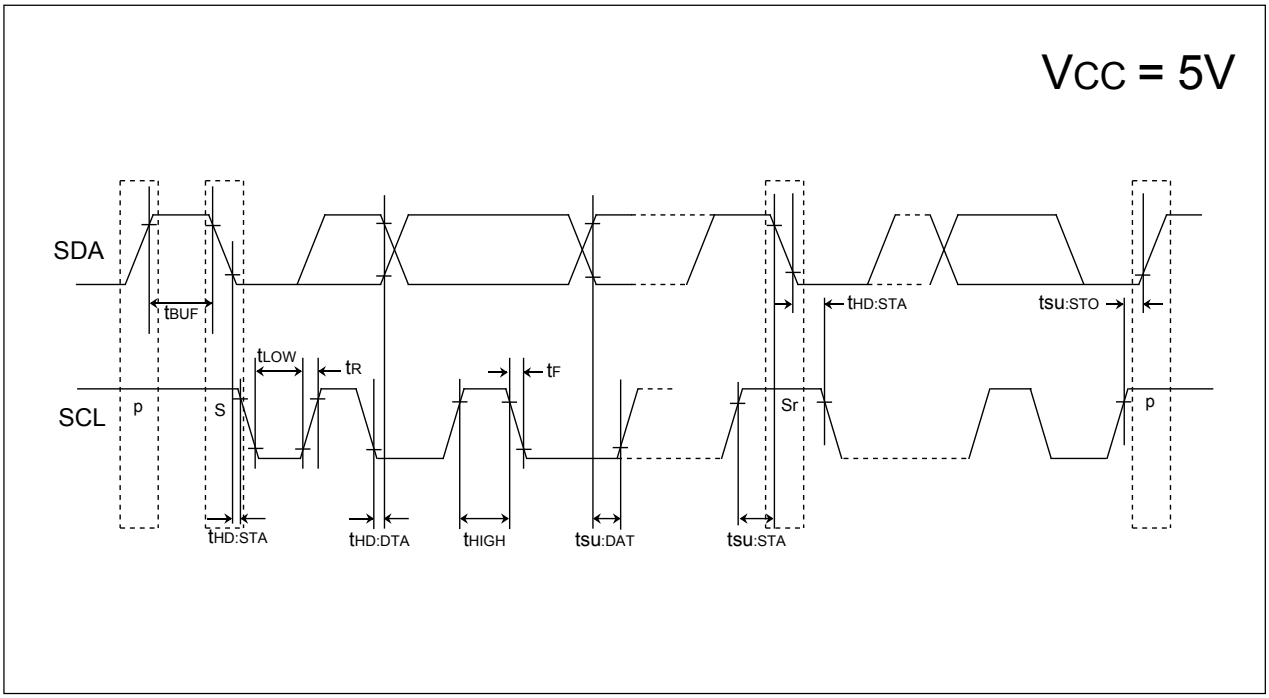


Figure 21.9 Timing Diagram (3)

V_{CC} = 5V

Table 21.85 Electrical Characteristics (2) (1)

Symbol	Parameter	Measurement Condition			Standard			Unit
					Min.	Typ.	Max.	
I_{CC}	Power Supply Current (V_{CC}=4.2 to 5.5V)	Output pins are left open and other pins are connected to V_{SS}	Mask ROM	f(BCLK) = 20 MHz, main clock, no division		18	25	mA
				f(BCLK) = 16 MHz, main clock, no division		14	20	mA
				On-chip oscillation, $f_{2(ROC)}$ selected, f(BCLK) = 1 MHz		2		mA
			Flash memory	f(BCLK) = 20 MHz, main clock, no division		18	25	mA
				f(BCLK) = 16 MHz, main clock, no division		14	20	mA
				On-chip oscillation, $f_{2(ROC)}$ selected, f(BCLK) = 1 MHz		2		mA
			Flash memory program	f(BCLK) = 10 MHz, Vcc = 5.0 V		11		mA
			Flash memory erase	f(BCLK) = 10 MHz, Vcc = 5.0 V		11		mA
			Mask ROM	f(BCLK) = 32 kHz, In low-power consumption mode, Program running on ROM(3)		25		µA
				On-chip oscillation, $f_{2(ROC)}$ selected, f(BCLK) = 1 MHz, In wait mode		50		µA
			Flash memory	f(BCLK) = 32 kHz, In low-power consumption mode, Program running on RAM(3)		25		µA
				f(BCLK) = 32 kHz, In low-power consumption mode, Program running on flash memory(3)		450		µA
				On-chip oscillation, $f_{2(ROC)}$ selected, f(BCLK) = 1 MHz, In wait mode		50		µA
			Mask ROM, Flash memory	f(BCLK) = 32 kHz, In wait mode(2), Oscillation capacity high		8.5		µA
				f(BCLK) = 32 kHz, In wait mode(2), Oscillation capacity low		3		µA
				While clock stops, Topr = 25° C		0.8	3	µA

NOTES:

1. Referenced to V_{CC} = 4.2 to 5.5 V, V_{SS} = 0 V at Topr = -40 to 105 ° C, f(BCLK) = 20MHz / V_{CC} = 4.2 to 5.5 V, V_{SS} = 0V at Topr = -40 to 125 ° C, f(BCLK) = 16 MHz, unless otherwise specified.
2. With one timer operates, using f_{C32}.
3. This indicates the memory in which the program to be executed exists.

22.7 Timer S

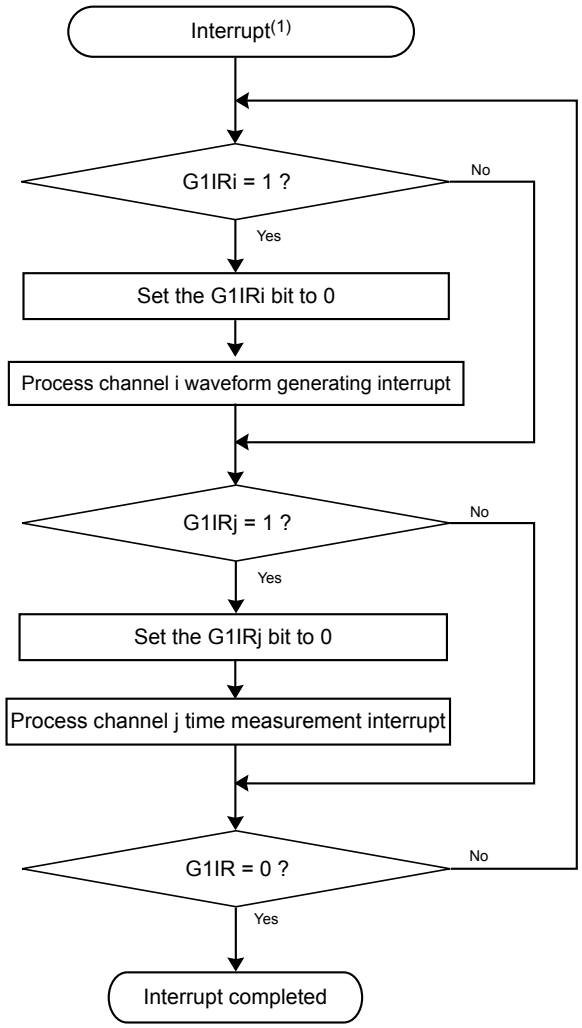
22.7.1 Rewrite the G1IR Register

Bits in the G1IR register are not automatically set to 0 (no interrupt requested) even if a requested interrupt is acknowledged. Set each bit to 0 by program after the interrupt requests are verified.

The IC/OC interrupt is generated when any bit in the G1IR register is set to 1 (interrupt requested) after all the bits are set to 0. If conditions to generate an interrupt are met when the G1IR register holds the value other than 00_{16}, the IC/OC interrupt request will not be generated. In order to enable an IC/OC interrupt request again, clear the G1IR register to 00_{16}. Use the following instructions to set each bit in the G1IR register to 0.

Subject instructions: AND, BCL

Figure 22.3 shows an example of IC/OC interrupt i flow chart.



NOTE:
1. Example for the interrupt operation when using the channel i waveform generating interrupt and channel j time measurement interrupt.

Figure 22.3 IC/OC Interrupt i Flow Chart

22.8 Serial I/O

22.8.1 Clock-Synchronous Serial I/O

22.8.1.1 Transmission/reception

1. With an external clock selected, and choosing the $\overline{RTS}$ function, the output level of the $\overline{RTSi}$ pin goes to “L” when the data-receivable status becomes ready, which informs the transmission side that the reception has become ready. The output level of the $\overline{RTSi}$ pin goes to “H” when reception starts. So if the $\overline{RTSi}$ pin is connected to the $\overline{CTSi}$ pin on the transmission side, the circuit can transmission and reception data with consistent timing. With the internal clock, the $\overline{RTS}$ function has no effect.

2. If a low-level signal is applied to the $\overline{SD}$ pin when the IVPCR1 bit in the TB2SC register is set to 1 (three-phase output forcible cutoff by input on $\overline{SD}$ pin enabled), the $P7_3/RTS_2/TxD1$(when the U1MAP bit in PACR register is 1) and CLK_2 pins go to a high-impedance state.

22.8.1.2 Transmission

When an external clock is selected, the conditions must be met while if the CKPOL bit in the UiC0 register is set to 0 (transmit data output at the falling edge and the receive data taken in at the rising edge of the transfer clock), the external clock is in the high state; if the CKPOL bit in the UiC0 register is set to 1 (transmit data output at the rising edge and the receive data taken in at the falling edge of the transfer clock), the external clock is in the low state.

- The TE bit in UiC1 register is set to 1 (transmission enabled)
- The TI bit in UiC1 register is set to 0 (data present in UiTB register)
- If $\overline{CTS}$ function is selected, input on the $\overline{CTSi}$ pin is set to “L”

22.8.1.3 Reception

1. In operating the clock-synchronous serial I/O, operating a transmitter generates a shift clock. Fix settings for transmission even when using the device only for reception. Dummy data is output to the outside from the TxDi pin when receiving data.

2. When an internal clock is selected, set the TE bit in the UiC1 register (i = 0 to 2) to 1 (transmission enabled) and write dummy data to the UiTB register, and the shift clock will thereby be generated. When an external clock is selected, set the TE bit in the UiC1 register (i = 0 to 2) to 1 and write dummy data to the UiTB register, and the shift clock will be generated when the external clock is fed to the CLKi input pin.

3. When successively receiving data, if all bits of the next receive data are prepared in the UARTi receive register while the RE bit in the UiC1 register (i = 0 to 2) is set to 1 (data present in the UiRB register), an overrun error occurs and the UiRB register OER bit is set to 1 (overrun error occurred). In this case, because the content of the UiRB register is undefined, a corrective measure must be taken by programs on the transmit and receive sides so that the valid data before the overrun error occurred will be retransmitted. Note that when an overrun error occurred, the SiRIC register IR bit does not change state.

4. To receive data in succession, set dummy data in the lower-order byte of the UiTB register every time reception is made.

5. When an external clock is selected, make sure the external clock is in high state if the CKPOL bit is set to 0, and in low state if the CKPOL bit is set to 1 before the following conditions are met:
   - The RE bit in the UiC1 register is set to 1 (reception enabled)
   - The TE bit in the UiC1 register is set to 1 (transmission enabled)
   - The TI bit in the UiC1 register= 0 (data present in the UiTB register)

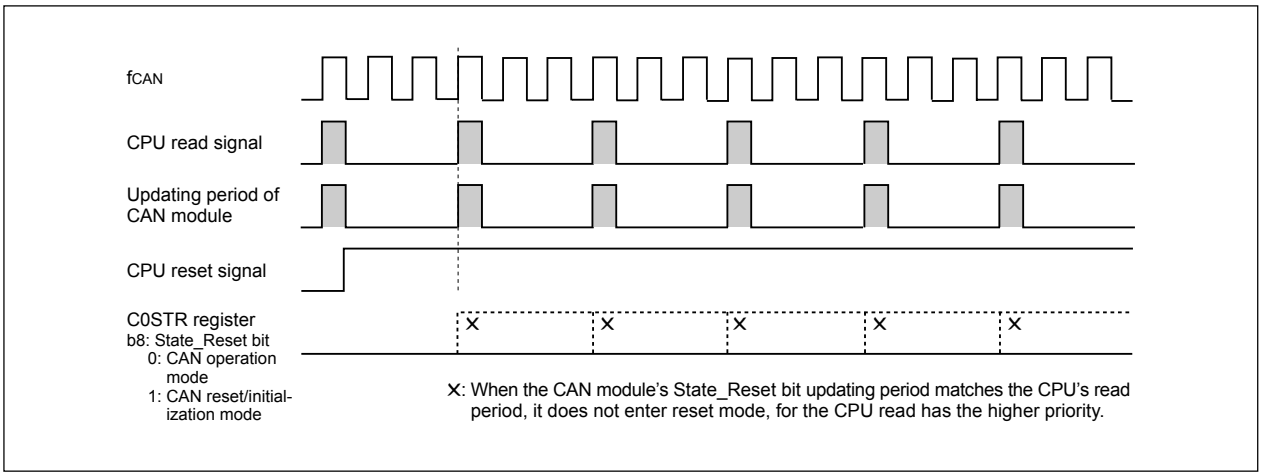


Figure 22.5 When Updating Period of CAN Module Matches Access Period from CPU

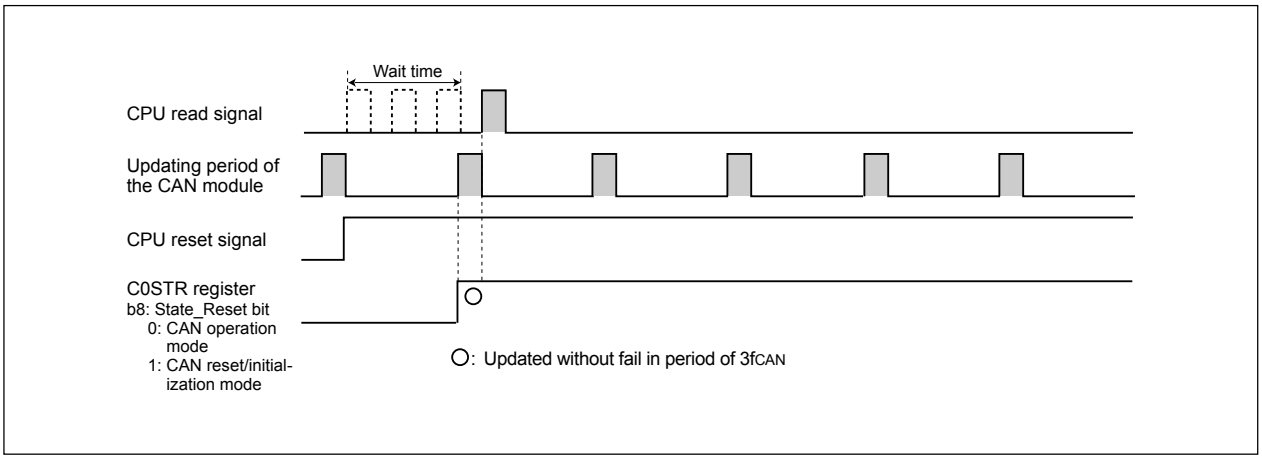


Figure 22.6 With a Wait Time of 3fCAN Before CPU Read

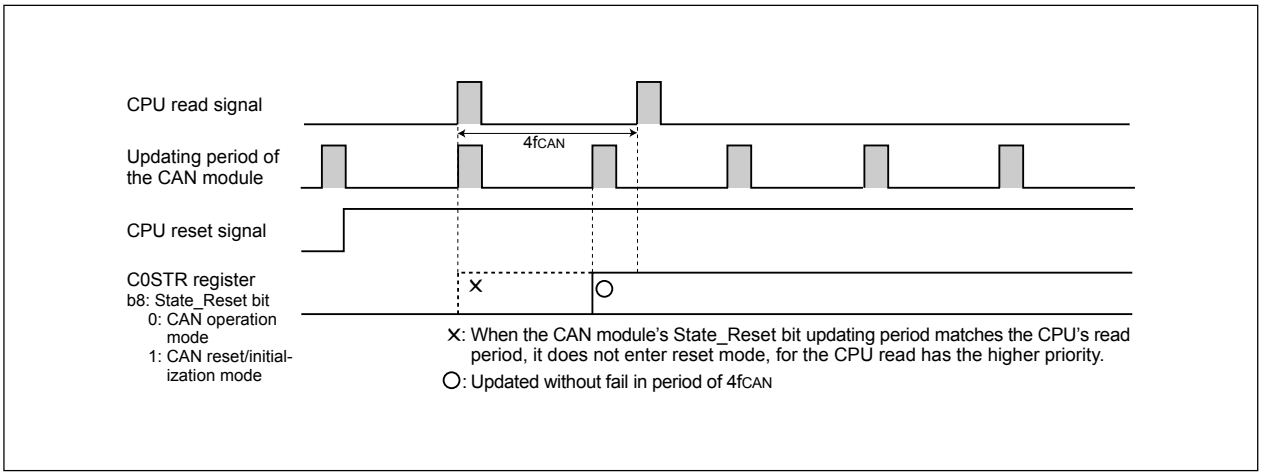


Figure 22.7 When Polling Period of CPU is 3fCAN or Longer