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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	M16C/60
Core Size	16-Bit
Speed	20MHz
Connectivity	CANbus, I²C, IEBus, SIO, UART/USART
Peripherals	DMA, POR, PWM, Voltage Detect, WDT
Number of I/O	55
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30291fahp-u5a

Quick Reference to Pages Classified by Address

Address	Register	Symbol	Page
0080₁₆ 0081₁₆ 0082₁₆ 0083₁₆ 0084₁₆ 0085₁₆	CAN0 message box 2: Identifier/DLC		289
0086₁₆ 0087₁₆ 0088₁₆ 0089₁₆ 008A₁₆ 008B₁₆ 008C₁₆ 008D₁₆	CAN0 message box 2: Data field		289
008E₁₆ 008F₁₆	CAN0 message box 2: time stamp		289
0090₁₆ 0091₁₆ 0092₁₆ 0093₁₆ 0094₁₆ 0095₁₆	CAN0 message box 3: Identifier/DLC		289
0096₁₆ 0097₁₆ 0098₁₆ 0099₁₆ 009A₁₆ 009B₁₆ 009C₁₆ 009D₁₆	CAN0 message box 3: Data field		289
009E₁₆ 009F₁₆	CAN0 message box 3: time stamp		289
00A0₁₆ 00A1₁₆ 00A2₁₆ 00A3₁₆ 00A4₁₆ 00A5₁₆	CAN0 message box 4: Identifier/DLC		289
00A6₁₆ 00A7₁₆ 00A8₁₆ 00A9₁₆ 00AA₁₆ 00AB₁₆ 00AC₁₆ 00AD₁₆	CAN0 message box 4: Data field		289
00AE₁₆ 00AF₁₆	CAN0 message box 4: time stamp		289
00B0₁₆ 00B1₁₆ 00B2₁₆ 00B3₁₆ 00B4₁₆ 00B5₁₆	CAN0 message box 5: Identifier/DLC		289
00B6₁₆ 00B7₁₆ 00B8₁₆ 00B9₁₆ 00BA₁₆ 00BB₁₆ 00BC₁₆ 00BD₁₆	CAN0 message box 5: Data field		289
00BE₁₆ 00BF₁₆	CAN0 message box 5: time stamp		289

Address	Register	Symbol	Page
00C0₁₆ 00C1₁₆ 00C2₁₆ 00C3₁₆ 00C4₁₆ 00C5₁₆	CAN0 message box 6: Identifier/DLC		289
00C6₁₆ 00C7₁₆ 00C8₁₆ 00C9₁₆ 00CA₁₆ 00CB₁₆ 00CC₁₆ 00CD₁₆	CAN0 message box 6: Data field		289
00CE₁₆ 00CF₁₆	CAN0 message box 6: time stamp		289
00D0₁₆ 00D1₁₆ 00D2₁₆ 00D3₁₆ 00D4₁₆ 00D5₁₆	CAN0 message box 7: Identifier/DLC		289
00D6₁₆ 00D7₁₆ 00D8₁₆ 00D9₁₆ 00DA₁₆ 00DB₁₆ 00DC₁₆ 00DD₁₆	CAN0 message box 7: Data field		289
00DE₁₆ 00DF₁₆	CAN0 message box 7: time stamp		289
00E0₁₆ 00E1₁₆ 00E2₁₆ 00E3₁₆ 00E4₁₆ 00E5₁₆	CAN0 message box 8: Identifier/DLC		289
00E6₁₆ 00E7₁₆ 00E8₁₆ 00E9₁₆ 00EA₁₆ 00EB₁₆ 00EC₁₆ 00ED₁₆	CAN0 message box 8: Data field		289
00EE₁₆ 00EF₁₆	CAN0 message box 8: time stamp		289
00F0₁₆ 00F1₁₆ 00F2₁₆ 00F3₁₆ 00F4₁₆ 00F5₁₆	CAN0 message box 9: Identifier/DLC		289
00F6₁₆ 00F7₁₆ 00F8₁₆ 00F9₁₆ 00FA₁₆ 00FB₁₆ 00FC₁₆ 00FD₁₆	CAN0 message box 9: Data field		289
00FE₁₆ 00FF₁₆	CAN0 message box 9: time stamp		289

Note: The blank areas are reserved and cannot be accessed by users.

1.3 Product List

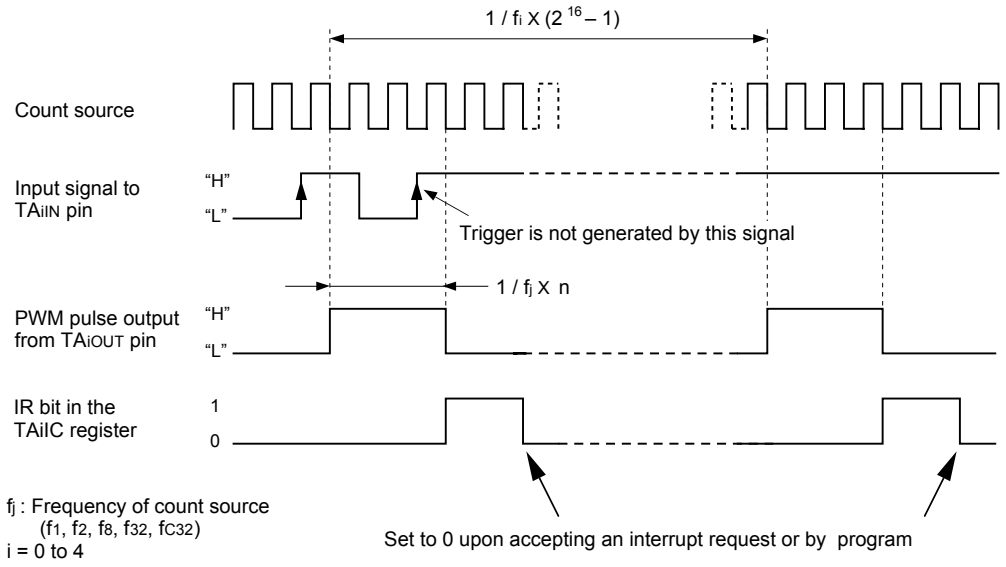
Tables 1.3 to 1.5 list the M16C/29 Group products and **Figure 1.3** shows the type numbers, memory sizes and packages. **Tables 1.6 to 1.8** list the product code of flash memory version for M16C/29 Group. **Figure 1.4 to Figure 1.6** show the marking diagram of flash memory version for M16C/29 Group.

Table 1.3 Product List (1) -Normal Version **As of March, 2007**

Type Number	ROM Capacity	RAM Capacity	Package Type	Remarks	Product Code
M30290FAHP	96 K + 4 K	8 K	PLQP0080KB-A (80P6Q-A)	Flash Memory	U3, U5, U7, U9
M30290FCHP	128 K + 4 K	12 K			
M30291FAHP	96 K + 4 K	8 K	PLQP0064KB-A (64P6Q-A)		
M30291FCHP	128 K + 4 K	12 K			
M30290M8-XXXHP	64 K	4 K	PLQP0080KB-A (80P6Q-A)	Mask ROM	U3, U5
M30290MA-XXXHP	96 K	8 K			
M30290MC-XXXHP	128 K	12 K			
M30291M8-XXXHP	64 K	4 K	PLQP0064KB-A (64P6Q-A)		
M30291MA-XXXHP	96 K	8 K			
M30291MC-XXXHP	128 K	12 K			

Table 1.4 Product List (2) -T Version **As of March, 2007**

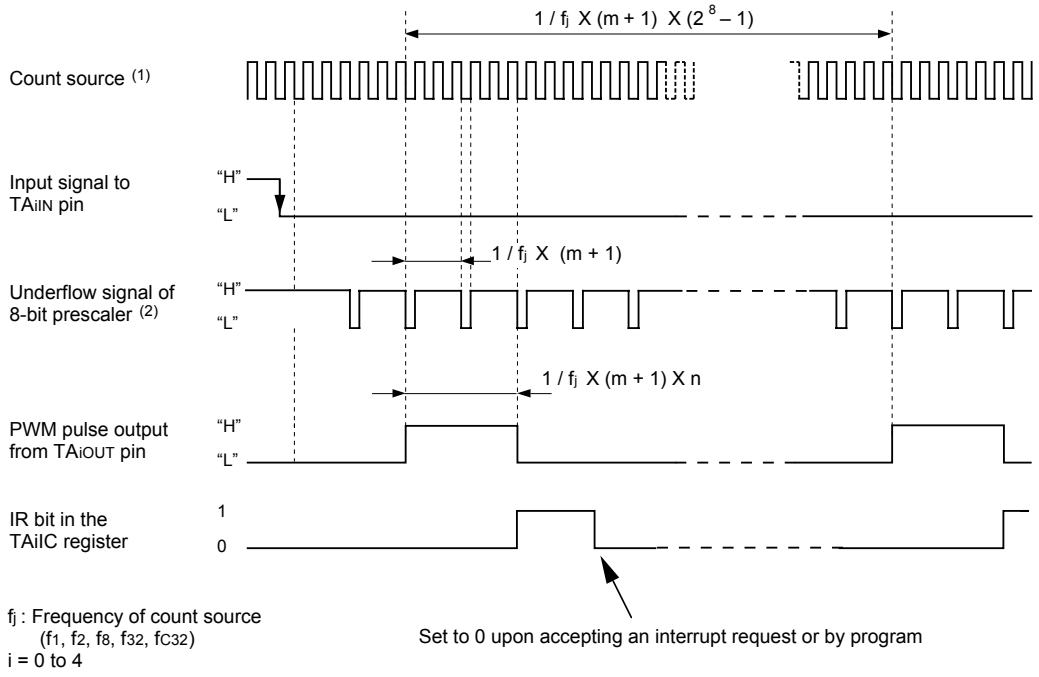
Type Number	ROM Capacity	RAM Capacity	Package Type	Remarks	Product Code
M30290FATHP	96 K + 4 K	8 K	PLQP0080KB-A (80P6Q-A)	Flash Memory	U3, U5, U7, U9
M30290FCTHP	128 K + 4 K	12 K			
M30291FATHP	96 K + 4 K	8 K	PLQP0064KB-A (64P6Q-A)		
M30291FCTHP	128 K + 4 K	12 K			
M30290M8T-XXXHP	64 K	4 K	PLQP0080KB-A (80P6Q-A)	Mask ROM	U0
M30290MAT-XXXHP	96 K	8 K			
M30290MCT-XXXHP	128 K	12 K			
M30291M8T-XXXHP	64 K	4 K	PLQP0064KB-A (64P6Q-A)		
M30291MAT-XXXHP	96 K	8 K			
M30291MCT-XXXHP	128 K	12 K			



fj : Frequency of count source
(f1, f2, f8, f32, fC32)
i = 0 to 4

NOTES:
1. n = 0000 16 to FFFE 16.
2. This timing diagram is for the case where the TAi register is 0003 16, bits TAiTGH and TAiTGL in the ONSF or TRGSR register is set to 00 2 (TAiIN pin input), the MR1 bit in the TAiMR register is set to 1 (rising edge), and the MR2 bit in the TAiMR register is set to 1 (trigger selected by TAiTGH and TAiTGL bits).

Figure 12.13 Example of 16-bit Pulse Width Modulator Operation



fj : Frequency of count source
(f1, f2, f8, f32, fC32)
i = 0 to 4

NOTES:
1. The 8-bit prescaler counts the count source.
2. The 8-bit pulse width modulator counts the 8-bit prescaler's underflow signal.
3. m = 00 16 to FF 16; n = 00 16 to FE 16.
4. This timing diagram is for the case where the TAi register is 0202 16, bits TAiTGH and TAiTGL in the ONSF or TRGSR register is set to 00 2 (TAiIN pin input), the MR1 bit in the TAiMR register is set to 0 (falling edge), and the MR2 bit in the TAiMR register is set to 1 (trigger selected by bits TAiTGH and TAiTGL).

Figure 12.14 Example of 8-bit Pulse Width Modulator Operation

12.3.1.2 Position-data-retain Function Control Register

Figure 12.36 shows the structure of the position-data-retain function contol register.

Position-Data-Retain Function Control Register (1)

b7	b6	b5	b4	b3	b2	b1	b0
✕	✕	✕	✕				

Symbol	Address	After Reset
PDRF	$034E_{16}$	$XXXX\ 0000_2$

Bit Symbol	Bit Name	Function	RW
PDRW	W-phase position data retain bit	Input level at pin IDW is read out. 0: "L" level 1: "H" level	RO
PDRV	V-phase position data retain bit	Input level at pin IDV is read out. 0: "L" level 1: "H" level	RO
PDRU	U-phase position data retain bit	Input level at pin IDU is read out. 0: "L" level 1: "H" level	RO
PDRT	Retain-trigger polarity select bit	0: Rising edge of positive phase 1: Falling edge of positive phase	RW
(b7-b4)	Nothing is assigned. If necessary, set to 0. When read, the contents are undefined		—

NOTE:
1.This register is valid only in the three-phase mode.

Figure 12.36 PDRF Register

12.3.1.2.1 W-phase Position Data Retain Bit (PDRW)

This bit is used to retain the input level at pin IDW.

12.3.1.2.2 V-phase Position Data Retain Bit (PDRV)

This bit is used to retain the input level at pin IDV.

12.3.1.2.3 U-phase Position Data Retain Bit (PDRU)

This bit is used to retain the input level at pin IDU.

12.3.1.2.4 Retain-trigger Polarity Select Bit (PDRT)

This bit is used to select the trigger polarity to retain the position data.

When this bit is set to 0, the rising edge of each positive phase selected.

When this bit is set to 1, the falling edge of each pocitive phase selected.

14.1.1 Clock Synchronous serial I/O Mode

The clock synchronous serial I/O mode uses a transfer clock to transmit and receive data. **Table 14.1** lists the specifications of the clock synchronous serial I/O mode. **Table 14.2** lists the registers used in clock synchronous serial I/O mode and the register values set.

Table 14.1 Clock Synchronous Serial I/O Mode Specifications

Item	Specification
Transfer data format	• Transfer data length: 8 bits
Transfer clock	• The CKDIR bit in the UiMR(i=0 to 2) register is set to 0 (internal clock) : fj/ (2(n+1)) fj = f1SIO, f2SIO, f8SIO, f32SIO. n: Setting value of UiBRG register 0016 to FF16 • CKDIR bit is set to 1 (external clock) : Input from CLKi pin
Transmission, reception control	• Selectable from $\overline{CTS}$ function, $\overline{RTS}$ function or $\overline{CTS}$/$\overline{RTS}$ function disable
Transmission start condition	• Before transmission can start, the following requirements must be met (1) – The TE bit in the UiC1 register is set to 1 (transmission enabled) – The TI bit in the UiC1 register is set to 0 (data present in UiTB register) – If $\overline{CTS}$ function is selected, input on the $\overline{CTS}$i pin is set to “L”
Reception start condition	• Before reception can start, the following requirements must be met (1) – The RE bit in the UiC1 register is set to 1 (reception enabled) – The TE bit in the UiC1 register is set to 1 (transmission enabled) – The TI bit in the UiC1 register is set to 0 (data present in the UiTB register)
Interrupt request generation timing	• For transmission, one of the following conditions can be selected – The UiIRS bit (3) is set to 0 (transmit buffer empty): when transferring data from the UiTB register to the UARTi transmit register (at start of transmission) – The UiIRS bit is set to 1 (transfer completed): when the serial I/O finished sending data from the UARTi transmit register • For reception When transferring data from the UARTi receive register to the UiRB register (at completion of reception)
Error detection	• Overrun error (2) This error occurs if the serial I/O started receiving the next data before reading the UiRB register and received the 7th bit in the the next data
Select function	• CLK polarity selection Transfer data input/output can be chosen to occur synchronously with the rising or the falling edge of the transfer clock • LSB first, MSB first selection Whether to start sending/receiving data beginning with bit 0 or beginning with bit 7 can be selected • Continuous receive mode selection Reception is enabled immediately by reading the UiRB register • Switching serial data logic (UART2) This function reverses the logic value of the transmit/receive data • Transfer clock output from multiple pins selection (UART1) The output pin can be selected in a program from two UART1 transfer clock pins that have been set • Separate $\overline{CTS}$/$\overline{RTS}$ pins (UART0) $\overline{CTS}_0$ and $\overline{RTS}_0$ are input/output from separate pins • UART1 pin remapping selection The UART1 pin can be selected from the P67 to P64 or P73 to P70

NOTES:
1. When an external clock is selected, the conditions must be met while if the CKPOL bit in the UiC0 register is set to 0 (transmit data output at the falling edge and the receive data taken in at the rising edge of the transfer clock), the external clock is in the high state; if the CKPOL bit in the UiC0 register is set to 1 (transmit data output at the rising edge and the receive data taken in at the falling edge of the transfer clock), the external clock is in the low state.
2. If an overrun error occurs, bits 8 to 0 in the UiRB register are undefined. The IR bit in the SiRIC register remains unchanged.
3. The U0IRS and U1IRS bits respectively are the bits 0 and 1 in the UCON register; the U2IRS bit is bit 4 in the U2C1 register.

A/D Control Register 0 (1)

b7	b6	b5	b4	b3	b2	b1	b0
			0	0			

Symbol: ADCON0 | Address: 03D6$_{16}$ | After Reset: 00000XXX$_2$

Bit Symbol	Bit Name	Function	RW
CH0	Analog input pin select bit (2, 3)	b2 b1 b0 0 0 0: Select AN$_0$ 0 0 1: Select AN$_1$ 0 1 0: Select AN$_2$ 0 1 1: Select AN$_3$ 1 0 0: Select AN$_4$ 1 0 1: Select AN$_5$ 1 1 0: Select AN$_6$ 1 1 1: Select AN$_7$	RW
CH1			RW
CH2			RW
MD0	A/D operation mode select bit 0 (3)	b4 b3 0 0: One-shot mode or delayed trigger mode 0,1	RW
MD1			RW
TRG	Trigger select bit	0: Software trigger 1: Hardware trigger ($\overline{\text{AD}}_{\text{TRG}}$ trigger)	RW
ADST	A/D conversion start flag	0: A/D conversion disabled 1: A/D conversion started	RW
CKS0	Frequency select bit 0	See **Table 15.2**	RW

NOTES:
1. If the ADCON0 register is rewritten during A/D conversion, the conversion result will be undefined.
2. AN0$_0$ to AN0$_7$, AN2$_0$ to AN2$_7$, and AN3$_0$ to AN3$_2$ can be used in the same way as AN$_0$ to AN$_7$. Use bits ADGSEL1 and ADGSEL 0 in the ADCON2 register to select the desired pin.
3. After rewriting bits MD1 and MD0, set bits CH2 to CH0 over again using an another instruction.

A/D Control Register 1 (1)

b7	b6	b5	b4	b3	b2	b1	b0
X	X	1			0		

Symbol: ADCON1 | Address: 03D7$_{16}$ | After Reset: 00$_{16}$

Bit Symbol	Bit Name	Function	RW
SCAN0	A/D Sweep Pin Select Bit	Invalid in one-shot mode	RW
SCAN1			RW
MD2	A/D Operation Mode Select Bit 1	0 : Any mode other than repeat sweep mode 1	RW
BITS	8/10-Bit Mode Select Bit	0 : 8-bit mode 1 : 10-bit mode	RW
CKS1	Frequency Select Bit 1	Refer to **Table 15.2**	RW
VCUT	Vref Connect Bit (2)	1 : Vref connected	RW
— (b7-b6)	Nothing is assigned. If necessary, set to 0. When read, the contents are 0		—

NOTES:
1. If the ADCON1 register is rewritten during A/D conversion, the conversion result will be undefined.
2. If the VCUT bit is reset from 0 (Vref unconnected) to 1 (Vref connected), wait for 1 µs or more before starting A/D conversion.

A/D Control Register 2 (1)

b7	b6	b5	b4	b3	b2	b1	b0
X	X	0		0			

Symbol: ADCON2 | Address: 03D4$_{16}$ | After Reset: 00$_{16}$

Bit Symbol	Bit Name	Function	RW
SMP	A/D conversion method select bit	0: Without sample and hold 1: With sample and hold	RW
ADGSEL0	A/D input group select bit	b2 b1 0 0: Select port P10 group 0 1: Select port P9 group 1 0: Select port P0 group 1 1: Select port P1/P9 group	RW
ADGSEL1			RW
— (b3)	Reserved bit	Set to 0	RW
CKS2	Frequency select bit 2	See **Table 15.2**	RW
TRG1	Trigger select bit 1	Set to 0 in one-shot mode	RW
— (b7-b6)	Nothing is assigned. If necessary, set to 0. When read, the content is 0		—

NOTE:
1. If the ADCON2 register is rewritten during A/D conversion, the conversion result will be undefined.

Figure 15.7 ADCON0 to ADCON2 Registers in One-Shot Mode

15.1.2 Repeat mode

In repeat mode, analog voltage applied to a selected pin is repeatedly converted to a digital code. **Table 15.4** shows the repeat mode specifications. **Figure 15.8** shows the operation example in repeat mode. **Figure 15.9** shows the ADCON0 to ADCON2 registers in repeat mode.

Table 15.4 Repeat Mode Specifications

Item	Specification
Function	Bits CH2 to CH0 in the ADCON0 register and the ADGSEL1 to ADGSEL0 bits in the ADCON2 register select pins. Analog voltage applied to a selected pin is repeatedly converted to a digital code
A/D Conversion Start Condition	• When the TRG bit in the ADCON0 register is 0 (software trigger) Set the ADST bit in the ADCON0 register to 1 (A/D conversion started) • When the TRG bit in the ADCON0 register is 1 (hardware trigger) The $\overline{\text{ADTRG}}$ pin input changes state from “H” to “L” after setting the ADST bit to 1 (A/D conversion started)
A/D Conversion Stop Condition	Set the ADST bit to 0 (A/D conversion halted)
Interrupt Request Generation Timing	None generated
Analog Input Pin	Select one pin from AN_0 to AN_7, $AN0_0$ to $AN0_7$, $AN2_0$ to $AN2_7$, and $AN3_0$ to $AN3_2$
Readout of A/D Conversion Result	Readout one of the AD0 to AD7 registers that corresponds to the selected pin

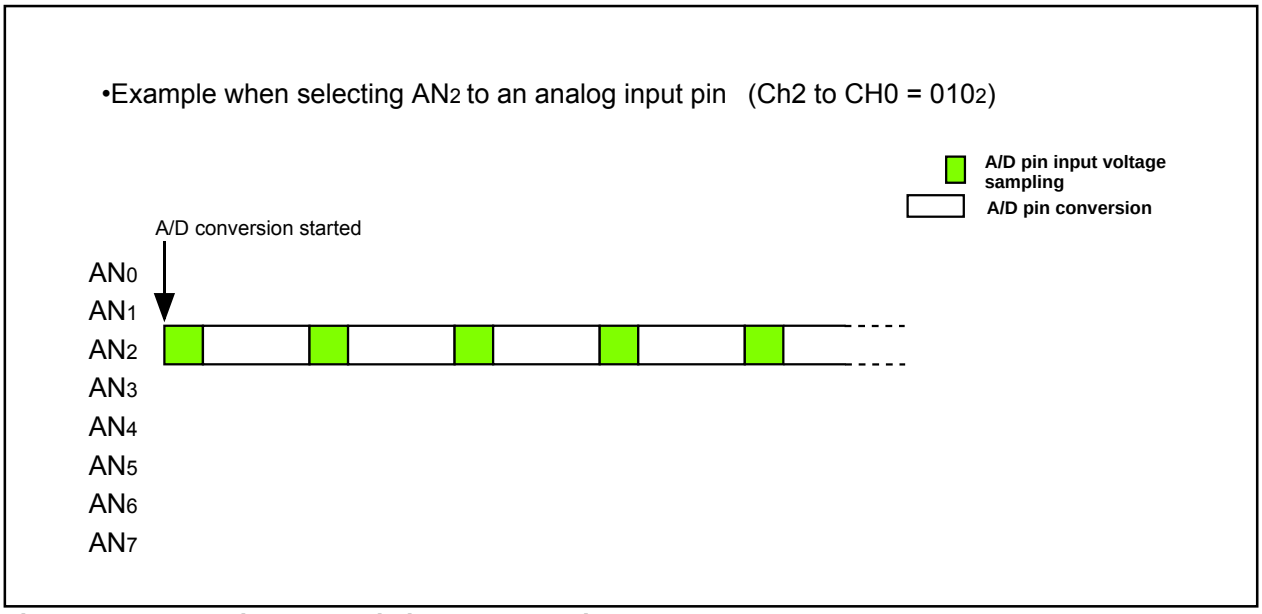


Figure 15.8 Operation Example in Repeat Mode

A/D Trigger Control Register (1)

b7	b6	b5	b4	b3	b2	b1	b0
X	X	X	X	0		1	1

Symbol	Address	After Reset
ADTRGCON	$03D2_{16}$	00_{16}

Bit Symbol	Bit Name	Function	RW
SSE	A/D operation mode select bit 2	1: Simultaneous sample sweep mode or delayed trigger mode 0, 1	RW
DTE	A/D operation mode select bit 3	0: Other than delayed trigger mode 0, 1	RW
HPTRG0	AN0 trigger select bit	See **Table 15.9**	RW
HPTRG1	AN1 trigger select bit	Set to 0 in simultaneous sample sweep mode	RW
$\overline{\text{(b7-b4)}}$	Nothing is assigned. If necessary, set to 0. When read, the content is 0		—

NOTE:
1. If ADTRGCON is rewritten during A/D conversion, the conversion result will be undefined.

Figure 15.18 ADTRGCON Register in Simultaneous Sample Sweep Mode

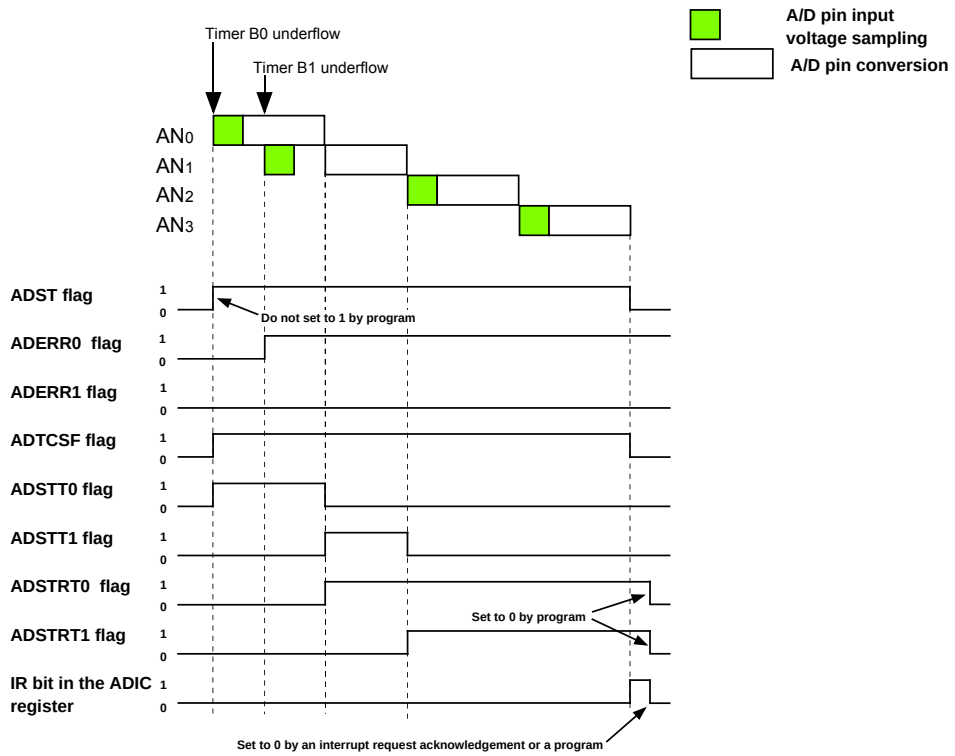
Table 15.9 Trigger Select Bit Setting in Simultaneous Sample Sweep Mode

TRG	TRG1	HPTRG0	TRIGGER
0	-	-	Software trigger
1	-	1	Timer B0 underflow (1)
1	0	0	$\overline{\text{AD}_{\text{TRG}}}$
1	1	0	Timer B2 or Timer B2 interrupt generation frequency setting counter underflow (2)

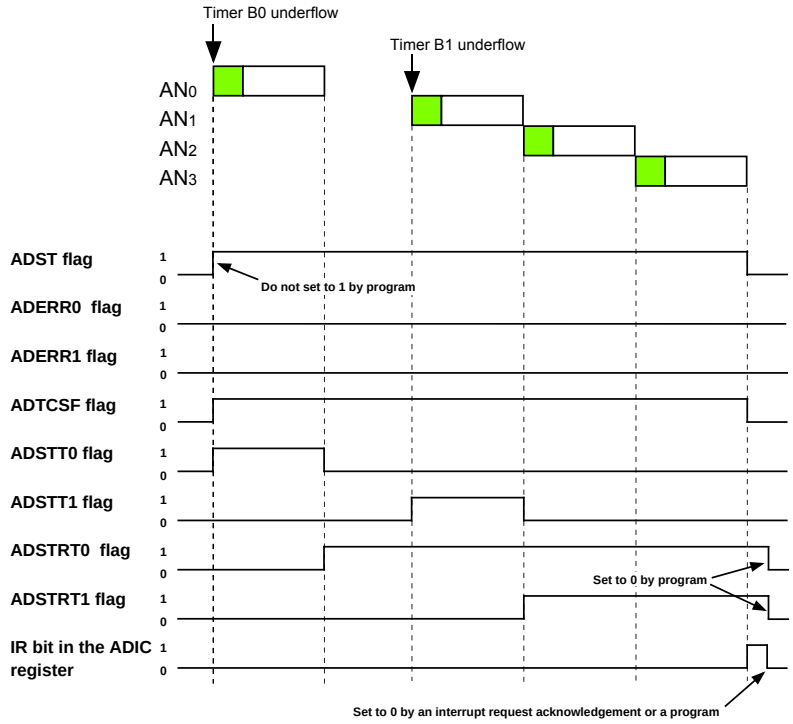
NOTES:
1. A count can be started for Timer B2, Timer B2 interrupt generation frequency setting counter underflow or the INT5 pin falling edge as count start conditions of Timer B0.
2. Select Timer B2 or Timer B2 interrupt generation frequency setting counter using the TB2SEL bit in the TB2SC register.

•Example when selecting AN_0 to AN_3 to A/D sweep pins (SCAN1 to SCAN0 = 01_2)

•Example 1: When Timer B1 underflow is generated during AN_0 pin conversion



•Example 2: When Timer B1 underflow is generated after AN_0 pin conversion



ADST flag: Bit 6 in the ADCON0 register
ADERR0, ADERR1, ADTCSF, ADSTT0, ADSTT1, ADSTRT0 and ADSTRT1 flag: bits 0, 1, 3, 4, 5, 6 and 7 in the ADSTAT0 register

Figure 15.20 Each Flag Operation in ADSTAT0 Register Associated with the Operation Example in Delayed Trigger Mode 0 (1)

I2C0 Data Shift Register

b7	b6	b5	b4	b3	b2	b1	b0

Symbol	Address	After Reset
S00	02E016	XX16

Function	RW
Transmit/receive data are stored. In master transmit mode, the start condition/stop condition are triggered by writing data to the register (refer to **16.9 START Condition Generation Method** and **16.11 STOP Condition Generation Method**). Start transmitting/receiving data while synchronizing with SCL	RW(1)

NOTE:
1. Write is enabled only when the ES0 bit in the S1D0 register is 1 (I2C bus interface is enabled). Write the transmit data after the receive data is read because the S00 register is used to store both the transmit and receive data. When the S00 register is set, bits BC2 to BC0 in the S1D0 register are set to 000_2, while bits LRB, AAS, and AL in the S10 register are set to 0 respectively.

I2C0 Clock Control Register

b7	b6	b5	b4	b3	b2	b1	b0

Symbol	Address	After Reset
S20	02E416	0016

Bit Symbol	Bit Name	Function	RW
CCR0	SCL Frequency Control Bits	See **Table 16.3**	RW
CCR1			RW
CCR2			RW
CCR3			RW
CCR4			RW
FAST MODE	SCL Mode Specification Bit	0: Standard clock mode 1: High-speed clock mode	RW
ACKBIT	ACK Bit	0: ACK is returned 1: ACK is not returned	RW
ACK-CLK	ACK Clock Bit	0: No ACK clock 1: With ACK clock	RW

Figure 16.3 S00 and S20 Registers

I2C0 Status Register

b7	b6	b5	b4	b3	b2	b1	b0

Symbol	Address	After Reset
S10	02E816	0001000X2

Bit Symbol	Bit Name	Function	RW
LRB	Last receive bit	0: Last bit = 0 1: Last bit = 1	RO(1)
ADR0	General call detecting flag	0: No general call detected 1: General call detected	RO(1)
AAS	Slave address comparison flag	0: No address matched 1: Address matched	RO(1)
AL	Arbitration lost detection flag	0: Not detected 1: Detected	RO(2)
PIN	I2C bus interface interrupt request bit	0: Interrupt request issued 1: No interrupt request issued	RO(2)
BB	Bus busy flag	0: Bus free 1: Bus busy	RO(1)
TRX	Communication mode select bits 0	0: Receive mode 1: Transmit mode	RW(3)
MST	Communication mode select bit 1	0: Slave mode 1: Master mode	RW(3)

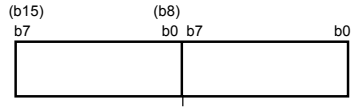
NOTES:
1. This bit is read only if it is used for the status check.
   To write to this bit, refer to **16.9 START Condition Generation Method** and **16.11 STOP Condition Generation Method**.
2. Read only. If necessary, set to 0.
3. To write to these bits, refer to **16.9 START Condition Generation Method** and **16.11 STOP Condition Generation Method.**

Figure 16.5 S10 Register

17.1.3.4 C0SSTR Register

Figure 17.9 shows the C0SSTR register.

CAN0 Slot Status Register

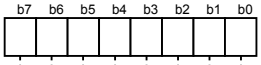


Symbol	Address	After Reset
C0SSTR	0215_{16}, 0214_{16}	0000_{16}

Function	Setting Values	RW
Slot status bits Each bit corresponds to the slot with the same number	0: Reception slot The message has been read. Transmission slot Transmission is not completed. 1: Reception slot The message has not been read. Transmission slot Transmission is completed	RO

Figure 17.9 C0SSTR Register

Port Pi Register (i=0 to 3, 6 to 8 and 10)(1)

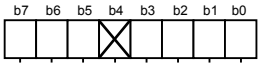


Symbol	Address	After Reset
P0 to P3	03E016, 03E116, 03E416, 03E516	Undefined
P6 to P8	03EC16, 03ED16, 03F016	Undefined
P10	03F416	Undefined

Bit Symbol	Bit Name	Function	RW
Pi_0	Port Pi0 bit	The pin level on any I/O port which is set for input mode can be read by reading the corresponding bit in this register. The pin level on any I/O port which is set for output mode can be controlled by writing to the corresponding bit in this register 0: "L" level 1: "H" level (1) (i = 0 to 3, 6 to 8 and 10)	RW
Pi_1	Port Pi1 bit		RW
Pi_2	Port Pi2 bit		RW
Pi_3	Port Pi3 bit		RW
Pi_4	Port Pi4 bit		RW
Pi_5	Port Pi5 bit		RW
Pi_6	Port Pi6 bit		RW
Pi_7	Port Pi7 bit		RW

NOTE:
1. Set the PACR register.
In 80-pin package, set bits PACR2, PACR1, PACR0 to 011_2.
In 64-pin package, set bits PACR2, PACR1, PACR0 to 010_2.

Port P9 Register (1)



Symbol	Address	After Reset
P9	03F116	Undefined

Bit Symbol	Bit Name	Function	RW
P9_0	Port P90 bit	The pin level on any I/O port which is set for input mode can be read by reading the corresponding bit in this register. The pin level on any I/O port which is set for output mode can be controlled by writing to the corresponding bit in this register (except for P85) 0: "L" level 1: "H" level	RW
P9_1	Port P91 bit		RW
P9_2	Port P92 bit		RW
P9_3	Port P93 bit		RW
$\overline{(b4)}$	Nothing is assigned (2)		-
P9_5	Port P95 bit		RW
P9_6	Port P96 bit		RW
P9_7	Port P97 bit		RW

NOTES:
1. Set the PACR register.
In 80-pin package, set bits PACR2, PACR1, PACR0 to 011_2.
In 64-pin package, set bits PACR2, PACR1, PACR0 to 010_2.
2. Nothing is assigned. If necessary, set to 0. When read, the content is 0.

Figure 19.7 P0 to P3 and P6 to P10 Registers

Flash Memory Control Register 4

b7	b6	b5	b4	b3	b2	b1	b0
0		0	0	0	0		

Symbol	Address	After Reset
FMR4	$01B3_{16}$	01000000_2

Bit Symbol	Bit Name	Function	RW
FMR40	Erase suspend function enable bit (1)	0: Disabled 1: Enabled	RW
FMR41	Erase suspend request bit (2)	0: Erase restart 1: Suspend request	RW
$\overline{\text{(b5-b2)}}$	Reserved bit	Set to 0	RO
FMR46	Erase status	0: During auto-erase operation 1: Auto-erase stop (erase suspend mode)	RO
$\overline{\text{(b7)}}$	Reserved bit	Set to 0	RW

NOTES:
1. Set the FMR40 bit to 1 immediately after setting it first to 0. Do not generate any interrupt or DMA transfer between setting the bit to 0 and setting it to 1. Set by program in space other than the flash memory in EW mode 0.
2. The FMR41 bit is valid only when the FMR40 bit is set to 1. The FMR41 bit can be written only between executing an erase command and completing erase (this bit is set to 0 other than the above duration). The FMR41 bit can be set to 0 or 1 by program in EW mode 0. In EW mode 1, the FMR41 bit is automatically set to 1 when the FMR40 bit is 1 and a maskable interrupt is generated during erasing. The FMR41 bit cannot be set to 1 by program (it can be set to 0 by program).

Figure 20.7 FMR4 Register

20.6 Precautions in CPU Rewrite Mode

Described below are the precautions to be observed when rewriting the flash memory in CPU rewrite mode.

20.6.1 Operation Speed

When the CPU clock source is the main clock, set the CPU clock frequency at 10 MHz or less with the CM06 bit in the CM0 register and bits CM17 and CM16 in the CM1 register, before entering CPU rewrite mode (EW mode 0 or EW mode 1). Also, when selecting f_3(ROC) of a on-chip oscillator as a CPU clock source, set bits ROCR3 and ROCR2 in the ROCR register to the CPU clock division rate at “divide-by-4” or “divide-by-8”, before entering CPU rewrite mode (EW mode 0 or EW mode 1).
In both cases, set the PM17 bit in the PM1 register to 1 (with wait state).

20.6.2 Prohibited Instructions

The following instructions cannot be used in EW mode 0 because the CPU tries to read data in the flash memory: UND instruction, INTO instruction, JMPS instruction, JSRS instruction, and BRK instruction

20.6.3 Interrupts

EW Mode 0

- To use interrupts having vectors in a relocatable vector table, the vectors must be relocated to the RAM area.
- The $\overline{\text{NMI}}$ and watchdog timer interrupts are available since registers FMR0 and FMR1 are forcibly reset when either interrupt occurs. However, the interrupt program, which allocates the jump addresses for each interrupt routine to the fixed vector table, is needed. Flash memory rewrite operation is aborted when the $\overline{\text{NMI}}$ or watchdog timer interrupt occurs. Set the FMR01 bit to 1 and execute the rewrite and erase program again after exiting the interrupt routine.
- The address match interrupt can not be used since the CPU tries to read data in the flash memory.

EW Mode 1

- Do not acknowledge any interrupts with vectors in the relocatable vector table or the address match interrupt during the auto program period or auto erase period with erase-suspend function disabled.

20.6.4 How to Access

To set bit FMR01, FMR02, FMR11 or FMR16 to 1, write 1 immediately after setting to 0. Do not generate an interrupt or a DMA transfer between the instruction to set the bit to 0 and the instruction to set it to 1.
When the $\overline{\text{NMI}}$ function is selected, set the bit while an “H” signal is applied to the P8$_5$/$\overline{\text{NMI}}$/$\overline{\text{SD}}$ pin.

20.6.5 Writing in the User ROM Area

20.6.5.1 EW Mode 0

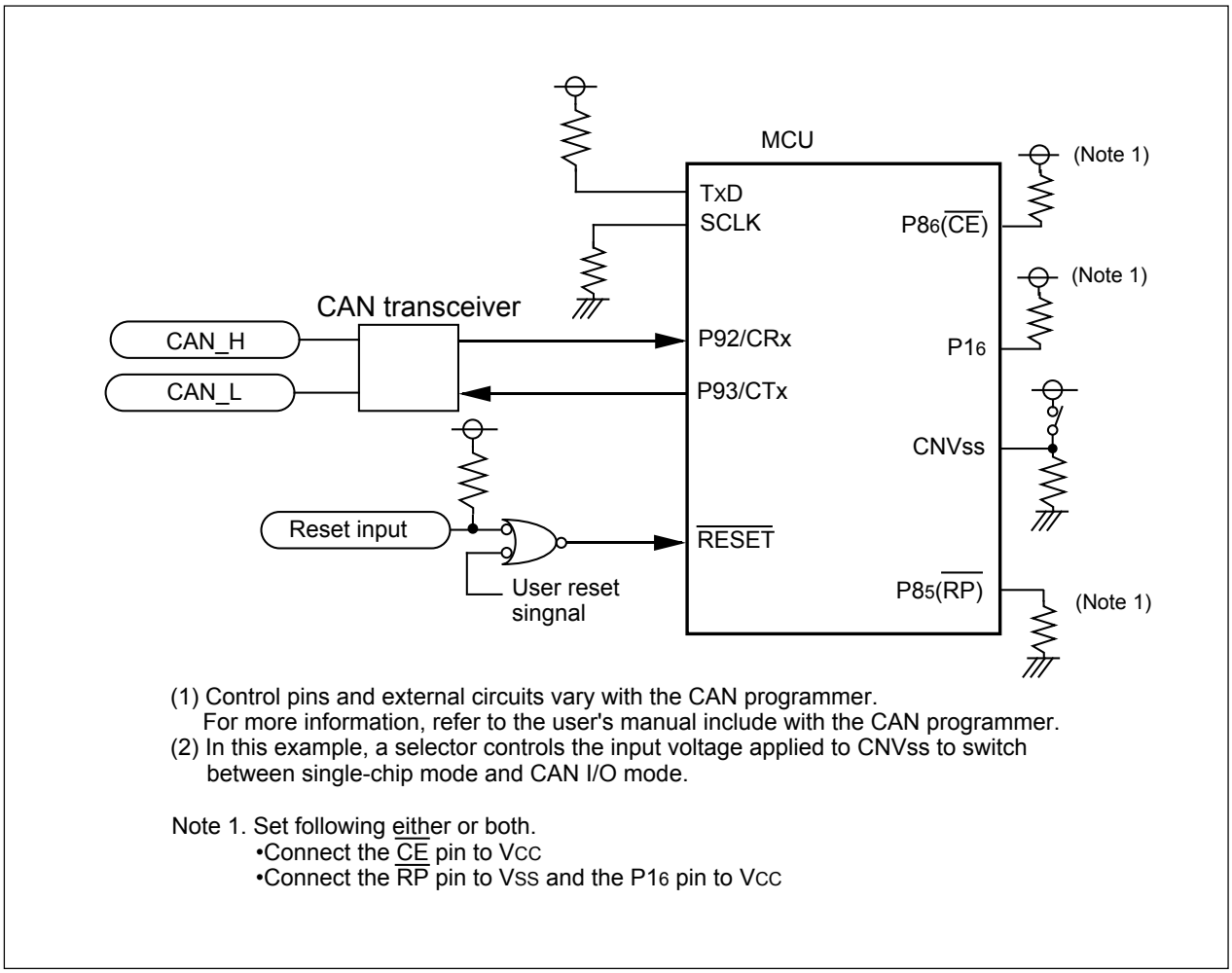
- If the supply voltage drops while rewriting the block where the rewrite control program is stored, the flash memory can not be rewritten, because the rewrite control program is not correctly rewritten. If this error occurs, rewrite the user ROM area in standard serial I/O mode or parallel I/O mode.

20.6.5.2 EW Mode 1

- Do not rewrite the block where the rewrite control program is stored.

20.11.2 Example of Circuit Application in CAN I/O Mode

Figure 20.21 shows example of circuit application in CAN I/O mode. Refer to the user's manual for CAN programmer to handle pins controlled by a CAN programmer.



(1) Control pins and external circuits vary with the CAN programmer.
For more information, refer to the user's manual include with the CAN programmer.
(2) In this example, a selector controls the input voltage applied to CNVss to switch between single-chip mode and CAN I/O mode.

Note 1. Set following either or both.
•Connect the $\overline{CE}$ pin to V_{CC}
•Connect the $\overline{RP}$ pin to V_{SS} and the $P1_6$ pin to V_{CC}

Figure 20.21 Circuit Application in CAN I/O Mode

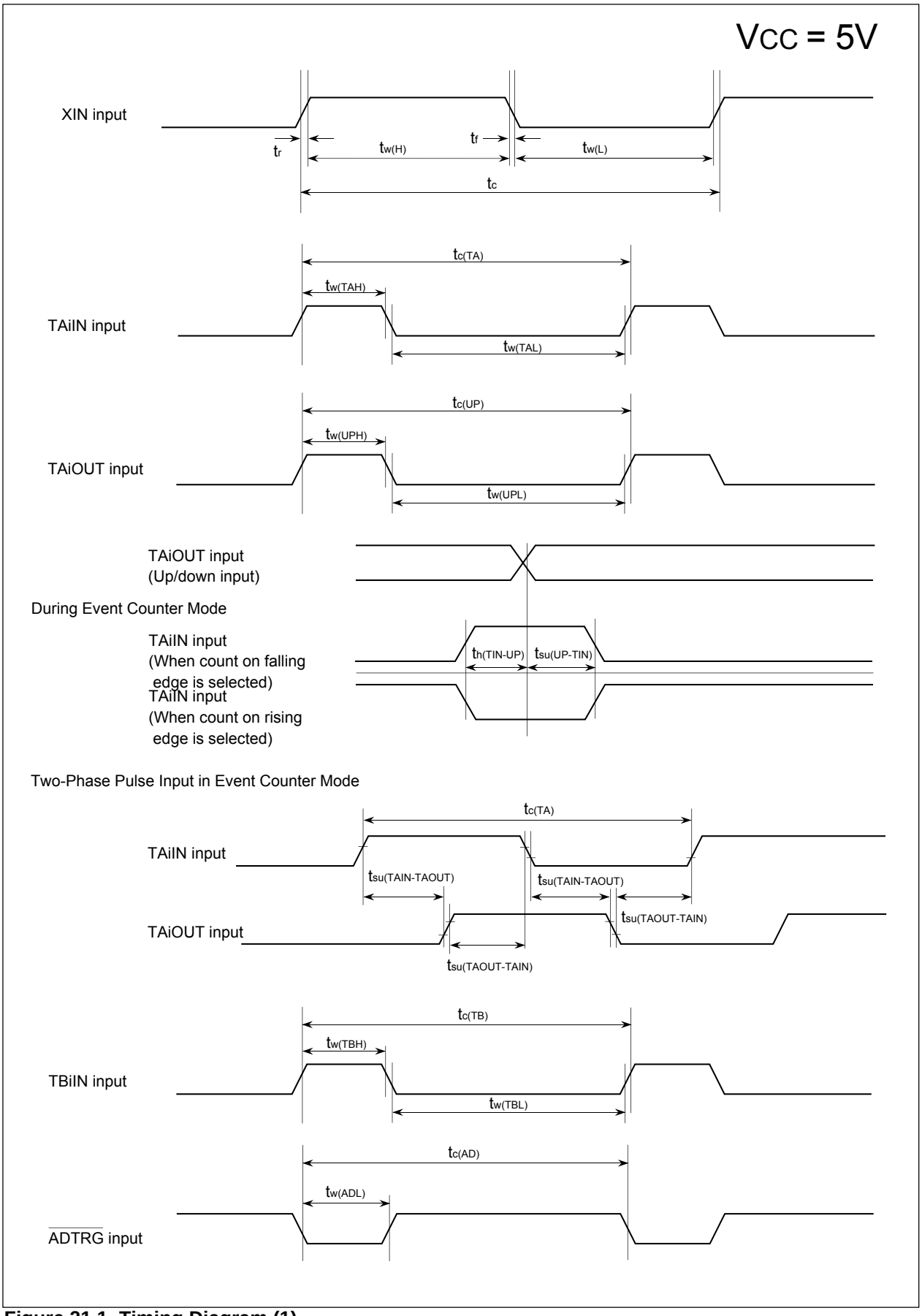


Figure 21.1 Timing Diagram (1)

VCC = 3V

Timing Requirements

(VCC = 3V, VSS = 0V, at Topr = – 20 to 85°C / – 40 to 85°C unless otherwise specified)

Table 21.26 External Clock Input (XIN input)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t_c	External clock input cycle time	100		ns
$t_{w(H)}$	External clock input HIGH pulse width	40		ns
$t_{w(L)}$	External clock input LOW pulse width	40		ns
t_r	External clock rise time		18	ns
t_f	External clock fall time		18	ns

V_{CC} = 3V

Timing Requirements

(V_{CC} = 3V, V_{SS} = 0V, at Topr = – 40 to 85°C unless otherwise specified)

Table 21.71 Timer B Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time (counted on one edge)	150		ns
$t_{w(TBH)}$	TBiIN input HIGH pulse width (counted on one edge)	60		ns
$t_{w(TBL)}$	TBiIN input LOW pulse width (counted on one edge)	60		ns
$t_{c(TB)}$	TBiIN input cycle time (counted on both edges)	300		ns
$t_{w(TBH)}$	TBiIN input HIGH pulse width (counted on both edges)	120		ns
$t_{w(TBL)}$	TBiIN input LOW pulse width (counted on both edges)	120		ns

Table 21.72 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	600		ns
$t_{w(TBH)}$	TBiIN input HIGH pulse width	300		ns
$t_{w(TBL)}$	TBiIN input LOW pulse width	300		ns

Table 21.73 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	600		ns
$t_{w(TBH)}$	TBiIN input HIGH pulse width	300		ns
$t_{w(TBL)}$	TBiIN input LOW pulse width	300		ns

Table 21.74 A/D Trigger Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(AD)}$	$\overline{ADTRG}$ input cycle time (trigger able minimum)	1500		ns
$t_{w(ADL)}$	$\overline{ADTRG}$ input LOW pulse width	200		ns

Table 21.75 Serial I/O

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	300		ns
$t_{w(CKH)}$	CLKi input HIGH pulse width	150		ns
$t_{w(CKL)}$	CLKi input LOW pulse width	150		ns
$t_{d(C-Q)}$	TxDi output delay time		160	ns
$t_{h(C-Q)}$	TxDi hold time	0		ns
$t_{su(D-C)}$	RxDi input setup time	100		ns
$t_{h(C-D)}$	RxDi input hold time	90		ns

Table 21.76 External Interrupt $\overline{INTi}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input HIGH pulse width	380		ns
$t_{w(INL)}$	$\overline{INTi}$ input LOW pulse width	380		ns

22.9 A/D Converter

1. Set registers ADCON0 (except bit 6), ADCON1, ADCON2 and ADTRGCON when A/D conversion is stopped (before a trigger occurs).

2. When the VCUT bit in ADCON1 register is changed from 0 (Vref not connected) to 1 (Vref connected), start A/D conversion after passing 1 µs or longer.

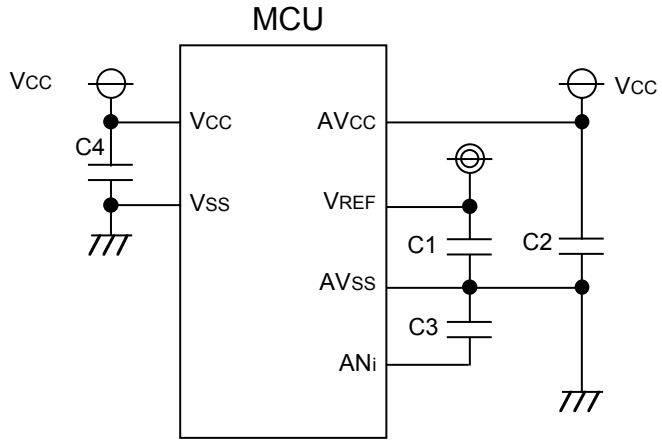
3. To prevent noise-induced device malfunction or latchup, as well as to reduce conversion errors, insert capacitors between the AVCC, VREF, and analog input pins (ANi, AN0i, AN2i(i=0 to 7), and AN3i(i=0 to 2)) each and the AVSS pin. Similarly, insert a capacitor between the VCC1 pin and the VSS pin. **Figure 22.4** is an example connection of each pin.

4. Make sure the port direction bits for those pins that are used as analog inputs are set to 0 (input mode). Also, if the TGR bit in the ADCON0 register is set to 1 (external trigger), make sure the port direction bit for the $\overline{\text{ADTRG}}$ pin is set to 0 (input mode).

5. When using key input interrupts, do not use any of the four AN4 to AN7 pins as analog inputs. (A key input interrupt request is generated when the A/D input voltage goes low.)

6. The ϕAD frequency must be 10 MHz or less. Without sample-and-hold function, limit the ϕAD frequency to 250kHz or more. With the sample and hold function, limit the ϕAD frequency to 1MHz or more.

7. When changing an A/D operation mode, select analog input pin again in bits CH2 to CH0 in the ADCON0 register and bits SCAN1 to SCAN0 in the ADCON1 register.



ANi: ANi, AN0i, AN2i (i=0 to 7), and AN3i (i=0 to 2)

NOTES:
1. C1 ≥ 0.47 µF, C2 ≥ 0.47 µF, C3 ≥ 100 pF, C4 ≥ 0.1 µF (reference)
2. Use thick and shortest possible wiring to connect capacitors.

Figure 22.4 Use of capacitors to reduce noise