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Details	
Product Status	Obsolete
Core Processor	M16C/60
Core Size	16-Bit
Speed	20MHz
Connectivity	CANbus, I²C, IEBus, SIO, UART/USART
Peripherals	DMA, POR, PWM, Voltage Detect, WDT
Number of I/O	55
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30291fahp-u7a

Table of Contents

Quick Reference to Pages Classified by Address

Address	Register	Symbol	Page
0180$_{16}$			
0181$_{16}$			
0182$_{16}$			
0183$_{16}$			
0184$_{16}$			
0185$_{16}$			
0186$_{16}$			
01B0$_{16}$			
01B1$_{16}$			
01B2$_{16}$			
01B3$_{16}$	Flash memory control register 4 (Note 2)	FMR4	342
01B4$_{16}$			
01B5$_{16}$	Flash memory control register 1 (Note 2)	FMR1	341
01B6$_{16}$			
01B7$_{16}$	Flash memory control register 0 (Note 2)	FMR0	341
01B8$_{16}$			
01B9$_{16}$			
01BA$_{16}$			
01BB$_{16}$			
01BC$_{16}$			
0200$_{16}$	CAN0 message control register 0	C0MCTL0	292
0201$_{16}$	CAN0 message control register 1	C0MCTL1	292
0202$_{16}$	CAN0 message control register 2	C0MCTL2	292
0203$_{16}$	CAN0 message control register 3	C0MCTL3	292
0204$_{16}$	CAN0 message control register 4	C0MCTL4	292
0205$_{16}$	CAN0 message control register 5	C0MCTL5	292
0206$_{16}$	CAN0 message control register 6	C0MCTL6	292
0207$_{16}$	CAN0 message control register 7	C0MCTL7	292
0208$_{16}$	CAN0 message control register 8	C0MCTL8	292
0209$_{16}$	CAN0 message control register 9	C0MCTL9	292
020A$_{16}$	CAN0 message control register 10	C0MCTL10	292
020B$_{16}$	CAN0 message control register 11	C0MCTL11	292
020C$_{16}$	CAN0 message control register 12	C0MCTL12	292
020D$_{16}$	CAN0 message control register 13	C0MCTL13	292
020E$_{16}$	CAN0 message control register 14	C0MCTL14	292
020F$_{16}$	CAN0 message control register 15	C0MCTL15	292
0210$_{16}$ 0211$_{16}$	CAN0 control register	C0CTLR	293
0212$_{16}$ 0213$_{16}$	CAN0 status register	C0STR	294
0214$_{16}$ 0215$_{16}$	CAN0 slot status register	C0SSTR	295
0216$_{16}$ 0217$_{16}$	CAN 0 interrupt control register	C0ICR	296
0218$_{16}$ 0219$_{16}$	CAN0 extended ID register	C0IDR	296
021A$_{16}$ 021B$_{16}$	CAN0 configuration register	C0CONR	297
021C$_{16}$	CAN0 receive error count register	C0RECR	298
021D$_{16}$	CAN0 transmit error count register	C0TECR	298
021E$_{16}$ 021F$_{16}$	CAN0 time stamp register	C0TSR	299
0210$_{16}$			
02FE$_{16}$			
02FF$_{16}$			

Address	Register	Symbol	Page
0240$_{16}$			
0241$_{16}$			
0242$_{16}$ 0243$_{16}$	CAN0 acceptance filter support register	C0AFS	299
0244$_{16}$			
0245$_{16}$			
0246$_{16}$			
0247$_{16}$			
0248$_{16}$			
0249$_{16}$			
024A$_{16}$			
024C$_{16}$			
024D$_{16}$			
024E$_{16}$			
024F$_{16}$			
0250$_{16}$			
0251$_{16}$			
0252$_{16}$			
0253$_{16}$			
0254$_{16}$			
0255$_{16}$			
0256$_{16}$			
0257$_{16}$			
0258$_{16}$			
0259$_{16}$			
025A$_{16}$	Three-phase protect control register	TPRC	139
025B$_{16}$			
025C$_{16}$	0n-chip oscillator control register	ROCR	50
025D$_{16}$	Pin assignment control register	PACR	177, 326
025E$_{16}$	Peripheral clock select register	PCLKR	52
025F$_{16}$	CAN0 clock select register	CCLKR	53
02E0$_{16}$	I^{2}C0 data shift register	S00	258
02E1$_{16}$			
02E2$_{16}$	I^{2}C0 address register	S0D0	257
02E3$_{16}$	I^{2}C0 control register 0	S1D0	259
02E4$_{16}$	I^{2}C0 clock control register	S20	258
02E5$_{16}$	I^{2}C0 start/stop condition control register	S2D0	263
02E6$_{16}$	I^{2}C0 control register 1	S3D0	261
02E7$_{16}$	I^{2}C0 control register 2	S4D0	262
02E8$_{16}$	I^{2}C0 status register	S10	260
02E9$_{16}$			
02EA$_{16}$			
02FE$_{16}$			
02FF$_{16}$			

Note 1: The blank areas are reserved and cannot be accessed by users.
Note 2: This register is included in the flash memory version.

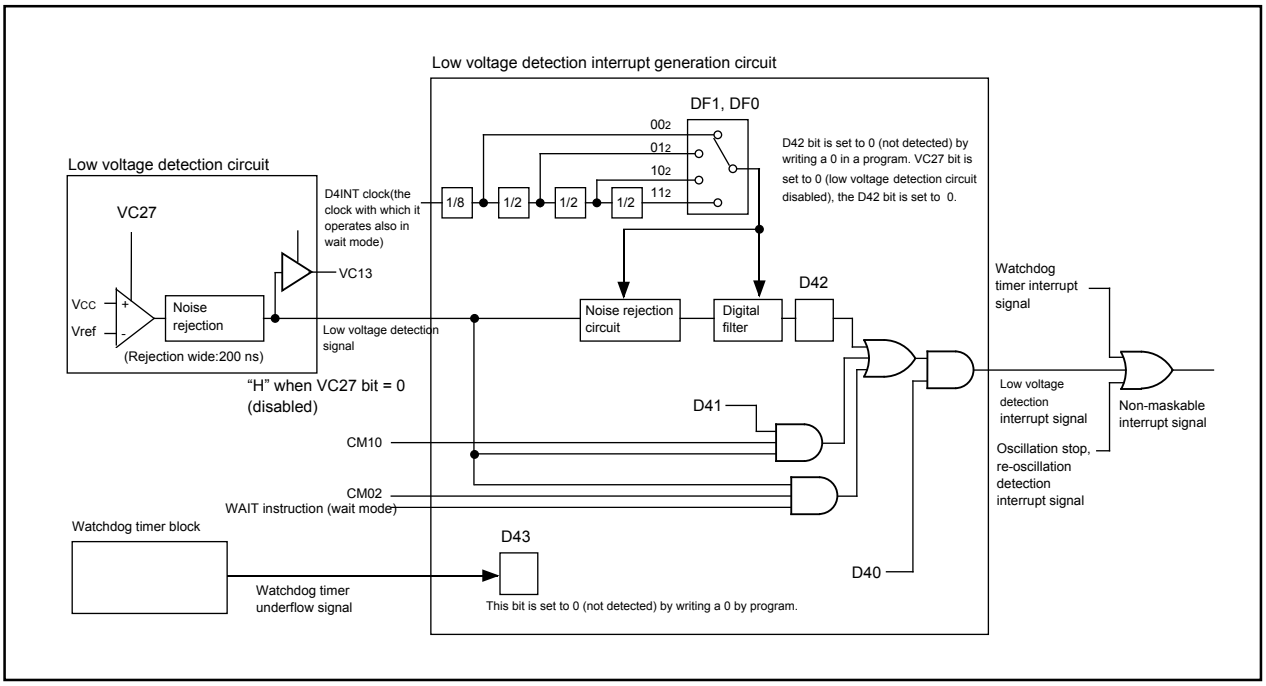
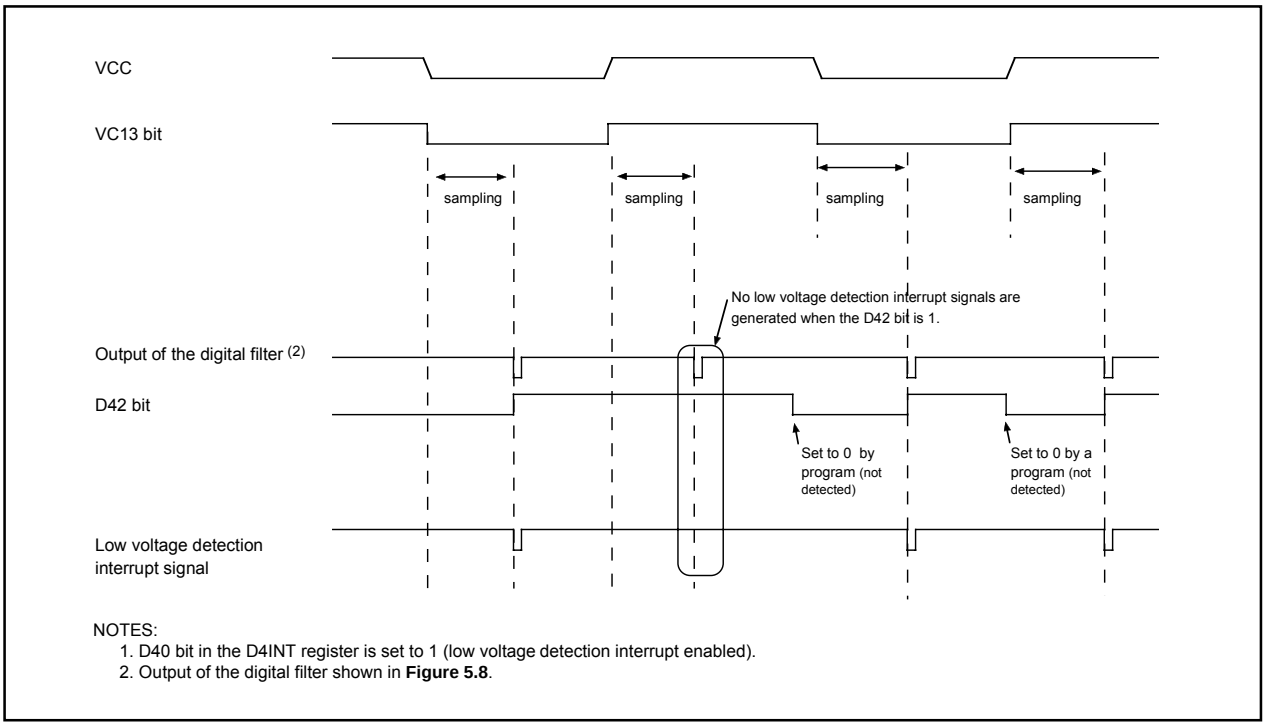


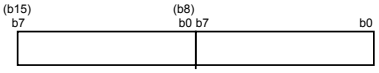
Figure 5.8 Low Voltage Detection Interrupt Generation Block



NOTES:
1. D40 bit in the D4INT register is set to 1 (low voltage detection interrupt enabled).
2. Output of the digital filter shown in **Figure 5.8**.

Figure 5.9 Low voltage Detection Interrupt Generation Circuit Operation Example

Timer Ai Register (i= 0 to 4) (1)

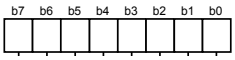


Symbol	Address	After Reset
TA0	038716, 038616	Undefined
TA1	038916, 038816	Undefined
TA2	038B16, 038A16	Undefined
TA3	038D16, 038C16	Undefined
TA4	038F16, 038E16	Undefined

Mode	Function	Setting Range	RW
Timer mode	Divide the count source by n + 1 where n = set value	000016 to FFFF16	RW
Event counter mode	Divide the count source by FFFF16 – n + 1 where n = set value when counting up or by n + 1 when counting down(5)	000016 to FFFF16	RW
One-shot timer mode	Divide the count source by n where n = set value and cause the timer to stop	000016 to FFFF16 (2, 4)	WO
Pulse width modulation mode (16-bit PWM)	Modify the pulse width as follows: PWM period: (216 – 1) / fj High level PWM pulse width: n / fj where n = set value, fj = count source frequency	000016 to FFFE16 (3, 4)	WO
Pulse width modulation mode (8-bit PWM)	Modify the pulse width as follows: PWM period: (28 – 1) x (m + 1)/ fj High level PWM pulse width: (m + 1)n / fj where n = high-order address set value, m = low-order address set value, fj = count source frequency	0016 to FE16 (High-order address) 0016 to FF16 (Low-order address) (3, 4)	WO

NOTES:
1. The register must be accessed in 16 bit units.
2. If the TAi register is set to 000016, the counter does not work and timer Ai interrupt requests are not generated either. Furthermore, if “pulse output” is selected, no pulses are output from the TAiOUT pin.
3. If the TAi register is set to 000016, the pulse width modulator does not work, the output level on the TAiOUT pin remains low, and timer Ai interrupt requests are not generated either. The same applies when the 8 high-order bits of the timer TAi register are set to 000016 while operating as an 8-bit pulse width modulator.
4. Use the MOV instruction to write to the TAi register.
5. The timer counts pulses from an external device or overflows or underflows in other timers.

Count Start Flag



Symbol	Address	After Reset
TABSR	038016	0016

Bit Symbol	Bit Name	Function	RW
TA0S	Timer A0 count start flag	0 : Stops counting 1 : Starts counting	RW
TA1S	Timer A1 count start flag		RW
TA2S	Timer A2 count start flag		RW
TA3S	Timer A3 count start flag		RW
TA4S	Timer A4 count start flag		RW
TB0S	Timer B0 count start flag		RW
TB1S	Timer B1 count start flag		RW
TB2S	Timer B2 count start flag		RW

Up/Down Flag (1)

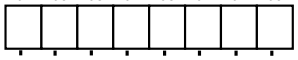
Symbol	Address	After Reset
UDF	038416	0016

Bit Symbol	Bit Name	Function	RW
TA0UD	Timer A0 up/down flag	0: Down count 1: Up count Enabled by setting the MR2 bit in the TAiMR register to 0 (= switching source in UDF register) during event counter mode	RW
TA1UD	Timer A1 up/down flag		RW
TA2UD	Timer A2 up/down flag		RW
TA3UD	Timer A3 up/down flag		RW
TA4UD	Timer A4 up/down flag		RW
TA2P	Timer A2 two-phase pulse signal processing select bit	0: two-phase pulse signal processing disabled 1: two-phase pulse signal processing enabled (2, 3)	WO
TA3P	Timer A3 two-phase pulse signal processing select bit		WO
TA4P	Timer A4 two-phase pulse signal processing select bit		WO

NOTES:
1. Use MOV instruction to write to this register.
2. Make sure the port direction bits for the TA2IN to TA4IN and TA2OUT to TA4OUT pins are set to 0 input mode.
3. When the two-phase pulse signal processing function is not used, set the corresponding bit to 0.

Figure 12.5 TA0 to TA4 Registers, TABSR Register, and UDF Register

Interrupt Request Register (1)



Symbol	Address	After Reset
G1IR	0330_{16}	Undefined

Bit Symbol	Bit Name	Function	RW
G1IR0	Interrupt request, Ch0	0 : No interrupt request 1 : Interrupt requested	RW
G1IR1	Interrupt request, Ch1		RW
G1IR2	Interrupt request, Ch2		RW
G1IR3	Interrupt request, Ch3		RW
G1IR4	Interrupt request, Ch4		RW
G1IR5	Interrupt request, Ch5		RW
G1IR6	Interrupt request, Ch6		RW
G1IR7	Interrupt request, Ch7		RW

NOTE:
1. When writing 0 to each bit in the G1IR register, use the following instruction:
AND, BCLR

Figure 13.9 G1IR Register

14.1.3.1 Detection of Start and Stop Condition

Whether a start or a stop condition has been detected is determined.

A start condition-detected interrupt request is generated when the SDA2 pin changes state from high to low while the SCL2 pin is in the high state. A stop condition-detected interrupt request is generated when the SDA2 pin changes state from low to high while the SCL2 pin is in the high state.

Because the start and stop condition-detected interrupts share the interrupt control register and vector, check the BBS bit in the U2SMR register to determine which interrupt source is requesting the interrupt.

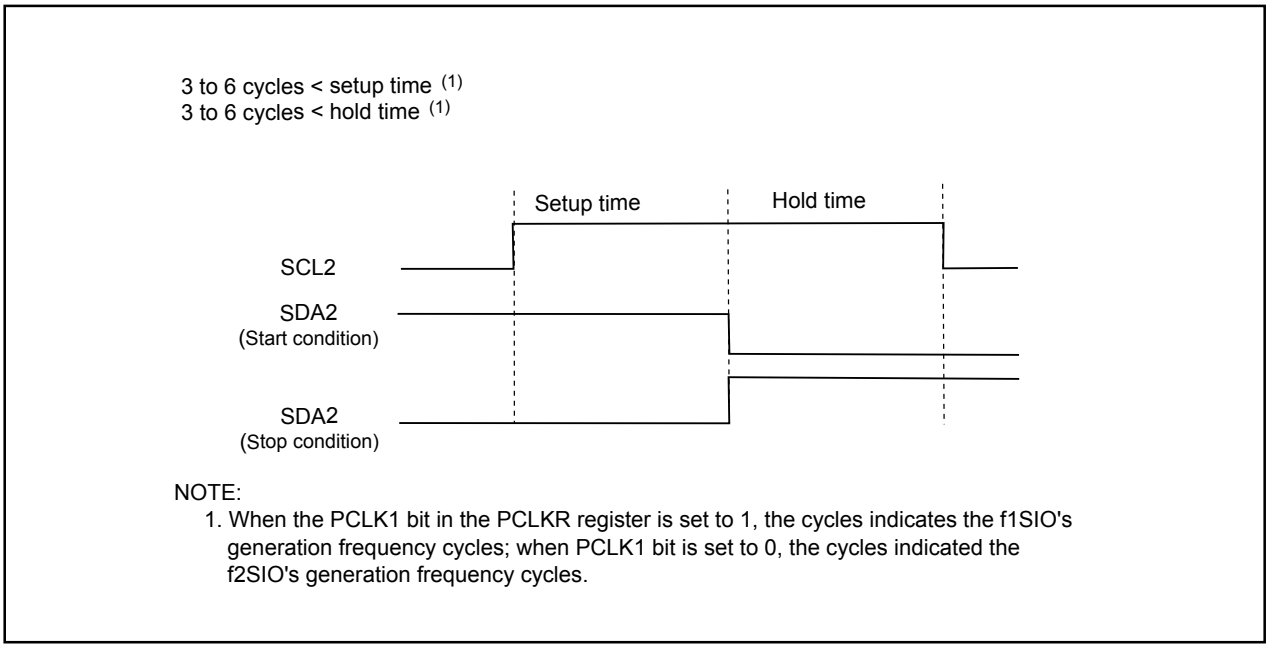


Figure 14.24 Detection of Start and Stop Condition

14.1.3.2 Output of Start and Stop Condition

A start condition is generated by setting the STAREQ bit in the U2SMR4 register to 1 (start).

A restart condition is generated by setting the RSTAREQ bit in the U2SMR4 register to 1 (start).

A stop condition is generated by setting the STPREQ bit in the U2SMR4 register to 1 (start).

The output procedure is described below.

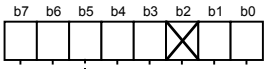
(1) Set the STAREQ bit, RSTAREQ bit or STPREQ bit to 1 (start).

(2) Set the STSPSEL bit in the U2SMR4 register to 1 (output).

Make sure that no interrupts or DMA transfers will occur between (1) and (2).

The function of the STSPSEL bit is shown in **Table 14.14** and **Figure 14.25**.

A/D Conversion Status Register 0 (1)



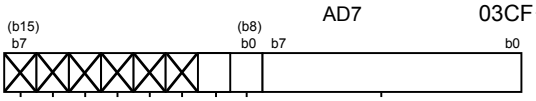
Symbol	Address	After reset
ADSTAT0	03D316	0016

Bit Symbol	Bit Name	Function	RW
ADERR0	AN1 trigger status flag	0: AN1 trigger did not occur during AN0 conversion 1: AN1 trigger occured during AN0 conversion	RW
ADERR1	Conversion termination flag	0: Conversion not terminated 1: Conversion terminated by Timer B0 underflow	RW
(b2)	Nothing is assigned. If necessary, set to 0. When read, its content is 0		—
ADTCSF	Delayed trigger sweep status flag	0: Sweep not in progress 1: Sweep in progress	RO
ADSTT0	AN0 conversion status flag	0: AN0 conversion not in progress 1: AN0 conversion in progress	RO
ADSTT1	AN1 conversion status flag	0: AN1 conversion not in progress 1: AN1 conversion in progress	RO
ADSTRT0	AN0 conversion completion status flag	0: AN0 conversion not completed 1: AN0 conversion completed	RW
ADSTRT1	AN1 conversion completion status flag	0: AN1 conversion not completed 1: AN1 conversion completed	RW

NOTE:
1. ADSTAT0 register is valid only when the DTE bit in the ADTRGCON register is set to 1.

A/D Register i (i=0 to 7)

Symbol	Address	After Reset
AD0	03C116 to 03C016	Undefined
AD1	03C316 to 03C216	Undefined
AD2	03C516 to 03C416	Undefined
AD3	03C716 to 03C616	Undefined
AD4	03C916 to 03C816	Undefined
AD5	03CB16 to 03CA16	Undefined
AD6	03CD16 to 03CC16	Undefined
AD7	03CF16 to 03CE16	Undefined



Function		RW
When the BITS bit in the ADCON1 register is 1 (10-bit mode)	When the BITS bit in the ADCON1 register is 0 (8-bit mode)	RW
Eight low-order bits of A/D conversion result	A/D conversion result	RO
Two high-order bits of A/D conversion result	When read, its content is undefined	RO
Nothing is assigned. If necessary, set to 0. When read, its content is 0		—

Figure 15.4 ADSTAT0 Register and AD0 to AD7 Registers

Timer B2 special mode register (1)

b7	b6	b5	b4	b3	b2	b1	b0
X	0	0					

Symbol	Address	After Reset
TB2SC	$039E_{16}$	$X0000000_2$

Bit Symbol	Bit Name	Function	RW
PWCON	Timer B2 reload timing switch bit (2)	0: Timer B2 underflow 1: Timer A output at odd-numbered	RW
IVPCR1	Three-phase output port $\overline{SD}$ control bit 1 (3, 4, 7)	0: Three-phase output forcible cutoff by $\overline{SD}$ pin input (high impedance) disabled 1: Three-phase output forcible cutoff by $\overline{SD}$ pin input (high impedance) enabled	RW
TB0EN	Timer B0 operation mode select bit	0: Other than A/D trigger mode 1: A/D trigger mode (5)	RW
TB1EN	Timer B1 operation mode select bit	0: Other than A/D trigger mode 1: A/D trigger mode (5)	RW
TB2SEL	Trigger select bit (6)	0: TB2 interrupt 1: Underflow of TB2 interrupt generation frequency setting counter [ICTB2]	RW
$\overline{\text{(b6-b5)}}$	Reserved bits	Set to 0	RW
— (b7)	Nothing is assigned. If necessary, set to 0. When read, its content is 0		—

NOTES:
1. Write to this register after setting the PRC1 bit in the PRCR register to 1 (write enabled).
2. If the INV11 bit is 0 (three-phase mode 0) or the INV06 bit is 1 (triangular wave modulation mode), set this bit to 0 (timer B2 underflow).
3. When setting the IVPCR1 bit to 1 (three-phase output forcible cutoff by $\overline{SD}$ pin input enabled), Set the $PD8_5$ bit to 0 (= input mode).
4. Related pins are U($P8_0$), $\overline{U}$($P8_1$), V($P7_2$), $\overline{V}$($P7_3$), W($P7_4$), $\overline{W}$($P7_5$). When a high-level ("H") signal is applied to the $\overline{SD}$ pin and set the IVPCR1 bit to 0 after forcible cutoff, pins U, $\overline{U}$, V, $\overline{V}$, W, and $\overline{W}$ are exit from the high-impedance state. If a low-level ("L") signal is applied to the $\overline{SD}$ pin, three-phase motor control timer output will be disabled (INV03=0). At this time, when the IVPCR1 bit is 0, pins U, $\overline{U}$, V, $\overline{V}$, W, and $\overline{W}$ become programmable I/O ports. When the IVPCR1 bit is set to 1, pins U, $\overline{U}$, V, $\overline{V}$, W, and $\overline{W}$ are placed in a high-impedance state regardless of which function of those pins is used.
5. When this bit is used in delayed trigger mode 0, set bits TB0EN and TB1EN to 1 (A/D trigger mode).
6. When setting the TB2SEL bit to 1 (underflow of TB2 interrupt generation frequency setting counter[ICTB2]), set the INV02 bit to 1 (three-phase motor control timer function).

Figure 15.5 TB2SC Register

17.1.1 CAN0 Message Box

Table 17.1 shows the memory mapping of the CAN0 message box.

It is possible to access to the message box in byte or word.

Mapping of the message contents differs from byte access to word access. Byte access or word access can be selected by the MsgOrder bit of the C0CTLR register.

Table 17.1 Memory Mapping of CAN0 Message Box

Address	Message content (Memory mapping)	
	Byte access (8 bits)	Word access (16 bits)
0060_{16} + n • 16 + 0	SID_{10} to SID_6	SID_5 to SID_0
0060_{16} + n • 16 + 1	SID_5 to SID_0	SID_{10} to SID_6
0060_{16} + n • 16 + 2	EID_{17} to EID_{14}	EID_{13} to EID_6
0060_{16} + n • 16 + 3	EID_{13} to EID_6	EID_{17} to EID_{14}
0060_{16} + n • 16 + 4	EID_5 to EID_0	Data Length Code (DLC)
0060_{16} + n • 16 + 5	Data Length Code (DLC)	EID_5 to EID_0
0060_{16} + n • 16 + 6	Data byte 0	Data byte 1
0060_{16} + n • 16 + 7 ⋮ 0060_{16} + n • 16 + 13	Data byte 1 ⋮ Data byte 7	Data byte 0 ⋮ Data byte 6
0060_{16} + n • 16 + 14	Time stamp high-order byte	Time stamp low-order byte
0060_{16} + n • 16 + 15	Time stamp low-order byte	Time stamp high-order byte

n = 0 to 15: the number of the slot

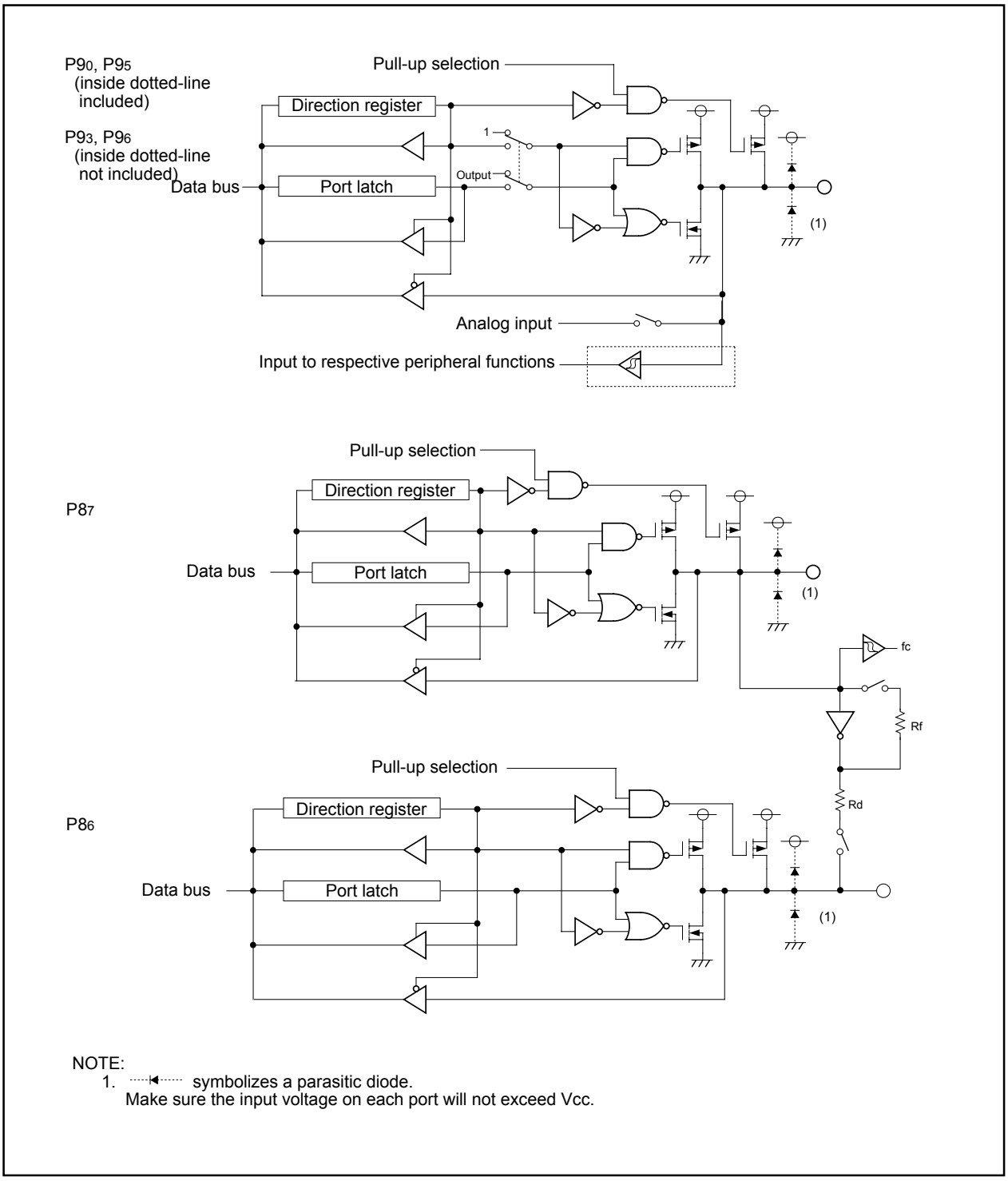


Figure 19.4 I/O Ports (4)

20.2 Memory Map

The flash memory contains the user ROM area and the boot ROM area (reserved area). **Figures 20.1** to **20.3** show a block diagram of the flash memory. The user ROM area has space to store the MCU operation program in single-chip mode and two 2-Kbyte spaces: the block A and B.

The user ROM area is divided into several blocks. The user ROM area can be rewritten in CPU rewrite, standard serial I/O, parallel I/O, or CAN I/O mode.

However, to rewrite program in block 0 and 1 in CPU rewrite mode, set the FMR02 bit in the FMR0 register to 1 (block 0, 1 rewrite enabled) and the FMR16 bit in the FMR1 register to 1 (blocks 0 to 5 rewrite enabled). Also, to rewrite program in blocks 2 to 5 in CPU rewrite mode, set the FMR16 bit in the FMR1 register to 1 (blocks 0 to 5 rewrite enabled). When the PM10 bit in the PM1 register is set to 1 (data space access enabled), blocks A and B can be available for use.

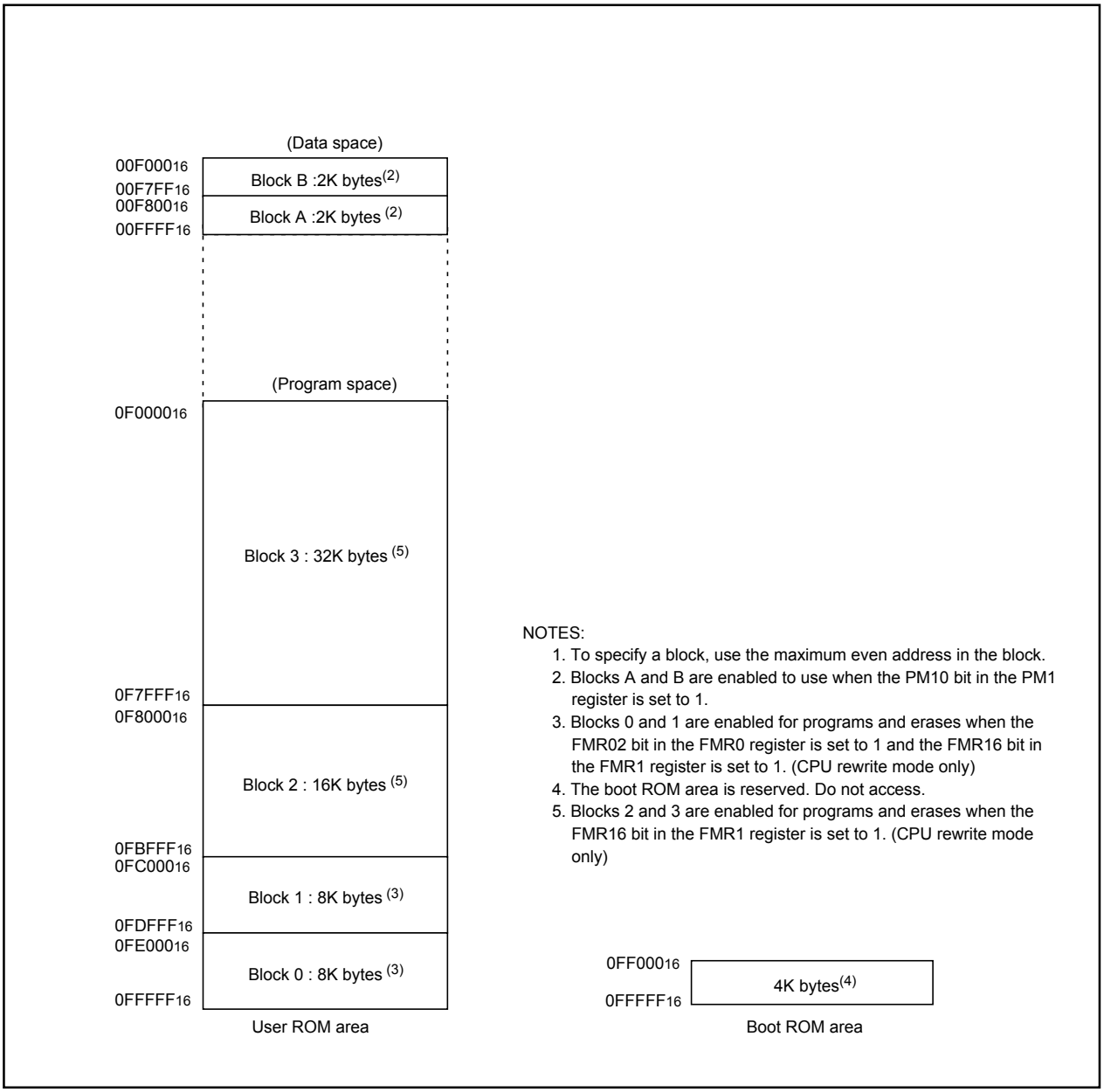


Figure 20.1 Flash Memory Block Diagram (ROM capacity 64 Kbytes)

20.8.4 Full Status Check

If an error occurs, bits FMR06 to FMR07 in the FMR0 register are set to 1, indicating a specific error. Therefore, execution results can be comfirmed by verifying these status bits (full status check).

Table 20.7 lists errors and FMR0 register state. **Figure 20.14** shows a flow chart of the full status check and handling procedure for each error.

Table 20.7 Errors and FMR0 Register Status

FMR0 register (SRD register) status		Error	Error occurrence condition
FMR07 (SR5)	FMR06 (SR4)		
1	1	Command sequence error	• An incorrect commands is written • A value other than xxD0$_{16}$ or xxFF$_{16}$ is written in the second bus cycle of the block erase command (1) • When the block erase command is executed on an protected block • When the program command is executed on protected blocks
1	0	Erase error	• The block erase command is executed on an unprotected block but the program operation is not successfully completed
0	1	Program error	• The program command is executed on an unprotected block but the program operation is not successfully completed

Note 1: The flash memory enters read array mode by writing command code xxFF$_{16}$ in the second bus cycle of these commands. The command code written in the first bus cycle becomes invalid.

Table 20.8 Pin Descriptions (Flash Memory Standard Serial I/O Mode)

Pin	Name		I/O	Descriptio n
VCC,VSS	Power input			Apply the voltage guaranteed for Program and Erase to Vcc pin and 0 V to Vss pin.
CNVSS	CNVSS		I	Connect to Vcc pin.
$\overline{\text{RESET}}$	Reset input		I	Reset input pin. While $\overline{\text{RESET}}$ pin is “L”, wait for td(ROC).
XIN	Clock input		I	Connect a ceramic resonator or crystal oscillator between XIN and XOUT pins. To input an externally generated clock, input it to XIN pin and open XOUT pin.
XOUT	Clock output		O	
AVCC, AVSS	Analog power supply input			Connect AVss to Vss and AVcc to Vcc, respectively.
VREF	Reference voltage input		I	Enter the reference voltage for AD conversion.
P00 to P07	Input port P0		I	Input “H” or “L” signal or leave open.
P10 to P15, P17	Input port P1		I	Input “H” or “L” signal or leave open.
P16	Input port P1		I	Connect this pin to Vcc while $\overline{\text{RESET}}$ pin is “L”. (2)
P20 to P27	Input port P2		I	Input "H" or “L” level signal or leave open.
P30 to P37	Input port P3		I	Input "H" or “L” level signal or leave open.
P60 to P63	Input port P6		I	Input "H" or “L” level signal or leave open.
P64	BUSY output		O	Standard serial I/O mode 1: BUSY signal output pin Standard serial I/O mode 2: Monitor signal output pin for boot program operation check
P65	SCLK input		I	Standard serial I/O mode 1: Serial clock input pin Standard serial I/O mode 2: Input “L”.
P66	RxD input		I	Serial data input pin
P67	TxD output		O	Serial data output pin (1)
P70 to P77	Input port P7		I	Input “H” or “L” signal or leave open.
P80 to P84, P87	Input port P8		I	Input “H” or “L” signal or leave open.
P85	$\overline{\text{RP}}$ input		I	Connect this pin to Vss while $\overline{\text{RESET}}$ pin is “L”. (2)
P86	$\overline{\text{CE}}$ input		I	Connect this pin to Vcc while $\overline{\text{RESET}}$ pin is “L”. (2)
P90 to P92, P95 to P97	Input port P9		I	Input “H” or “L” signal or leave open.
P93	Input port P93	Normal-ver.	I/O	“H” signal is output for specific time. Input “H” signal or leave open.
		T-ver./V-ver.	I	Input “H” or “L” signal or leave open.
P100 to P107	Input port P10		I	Input “H” or “L” signal or leave open.

NOTES:

1. When using standard serial I/O mode 1, to input “H” to the TxD pin is necessary while the $\overline{\text{RESET}}$ pin is held “L”. Therefore, connect this pin to VCC via a resistor. Adjust the pull-up resistor value on a system not to affect a data transfer after reset, because this pin changes to a data-output pin
2. Set the following, either or both.
   -Connect the $\overline{\text{CE}}$ pin to VCC.
   -Connect the $\overline{\text{RP}}$ pin to VSS and P16 pin to VCC.

20.10 Parallel I/O Mode

In parallel input/output mode, the user ROM can be rewritten by a parallel programmer supporting the M16C/29 group. Contact your parallel programmer manufacturer for more information on the parallel programmer. Refer to the user's manual included with your parallel programmer for instructions.

20.10.1 ROM Code Protect Function

The ROM code protect function prevents the flash memory from being read or rewritten. (Refer to **20.3 Functions To Prevent Flash Memory from Rewriting**).

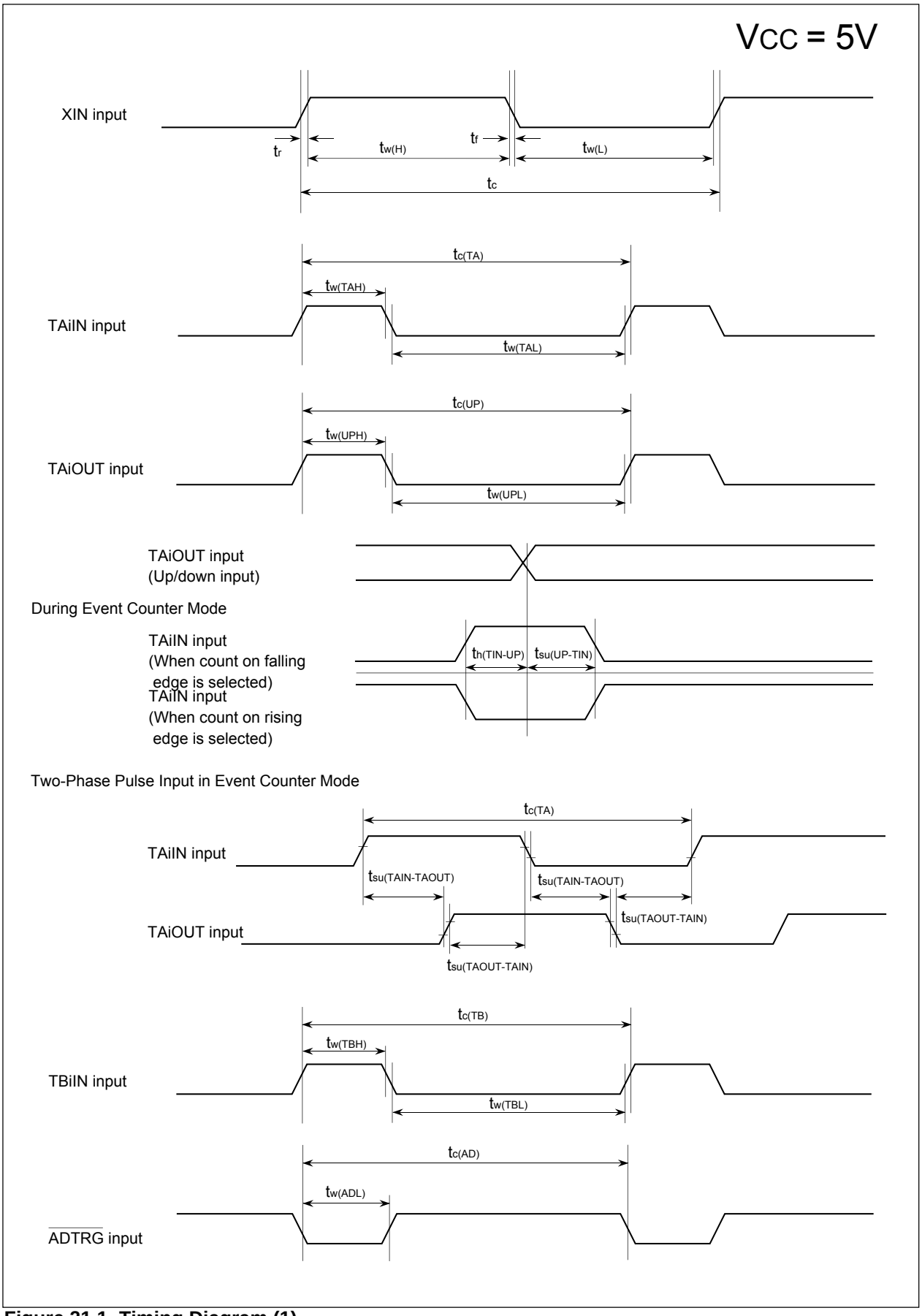


Figure 21.1 Timing Diagram (1)

V_{CC} = 3V

Timing Requirements

(V_{CC} = 3V, V_{SS} = 0V, at Topr = – 40 to 85°C unless otherwise specified)

Table 21.77 Multi-master I^2C bus Line

Symbol	Parameter	Standard clock mode		High-speed clock mode		Unit
		Min.	Max.	Min.	Max.	
tBUF	Bus free time	4.7		1.3		µs
tHD;STA	The hold time in start condition	4.0		0.6		µs
tLOW	The hold time in SCL clock 0 status	4.7		1.3		µs
tR	SCL, SDA signals' rising time		1000	20+0.1Cb	300	ns
tHD;DAT	Data hold time	0		0	0.9	µs
tHIGH	The hold time in SCL clock 1 status	4.0		0.6		µs
tF	SCL, SDA signals' falling time		300	20+0.1Cb	300	ns
tsu;DAT	Data setup time	250		100		ns
tsu;STA	The setup time in restart condition	4.7		0.6		µs
tsu;STO	Stop condition setup time	4.0		0.6		µs

VCC = 5V

Timing Requirements

(VCC=5V, VSS=0V, at Topr=-40 to 125°C unless otherwise specified)

Table 21.93 Timer B Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN Input Cycle Time (counted on one edge)	100		ns
$t_{w(TBH)}$	TBiIN Input High ("H") Width (counted on one edge)	40		ns
$t_{w(TBL)}$	TBiIN Input Low ("L") Width (counted on one edge)	40		ns
$t_{c(TB)}$	TBiIN Input Cycle Time (counted on both edges)	200		ns
$t_{w(TBH)}$	TBiIN Input High ("H") Width (counted on both edges)	80		ns
$t_{w(TBL)}$	TBiIN Input Low ("L") Width (counted on both edges)	80		ns

Table 21.94 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN Input Cycle Time	400		ns
$t_{w(TBH)}$	TBiIN Input High ("H") Width	200		ns
$t_{w(TBL)}$	TBiIN Input Low ("L") Width	200		ns

Table 21.95 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN Input Cycle Time	400		ns
$t_{w(TBH)}$	TBiIN Input High ("H") Width	200		ns
$t_{w(TBL)}$	TBiIN Input Low ("L") Width	200		ns

Table 21.96 A/D Trigger Input

Symbol	Parameter	Standard		Unit
		Min.	Max	
$t_{c(AD)}$	$\overline{ADTRG}$ Input Cycle Time (required for trigger)	1000		ns
$t_{w(ADL)}$	$\overline{ADTRG}$ Input Low ("L") Width	125		ns

Table 21.97 Serial I/O

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi Input Cycle Time	200		ns
$t_{w(CKH)}$	CLKi Input High ("H") Width	100		ns
$t_{w(CKL)}$	CLKi Input Low ("L") Width	100		ns
$t_{d(C-Q)}$	TxDi Output Delay Time		80	ns
$t_{h(C-Q)}$	TxDi Hold Time	0		ns
$t_{su(D-C)}$	RxDi Input Setup Time	70		ns
$t_{h(C-Q)}$	RxDi Input Hold Time	90		ns

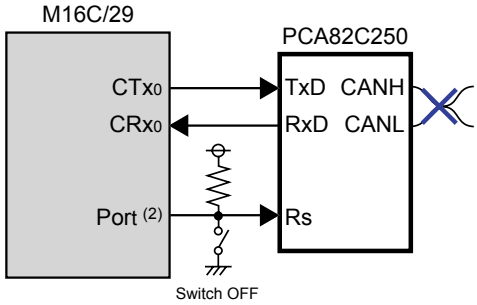
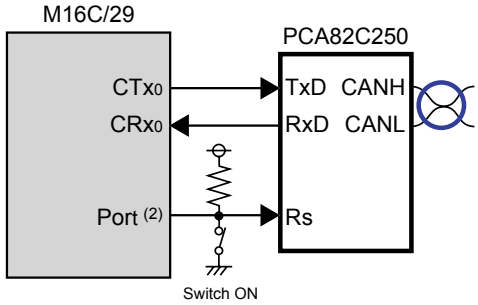
Table 21.98 External Interrupt $\overline{INTi}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ Input High ("H") Width	250		ns
$t_{w(INL)}$	$\overline{INTi}$ Input Low ("L") Width	250		ns

22.11.2 CAN Transceiver in Boot Mode

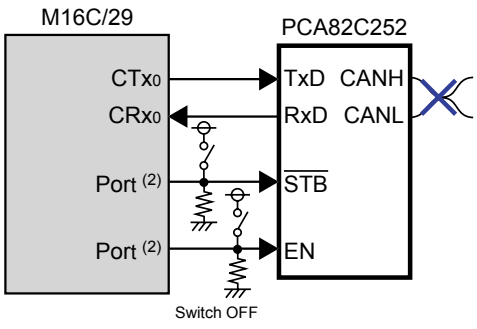
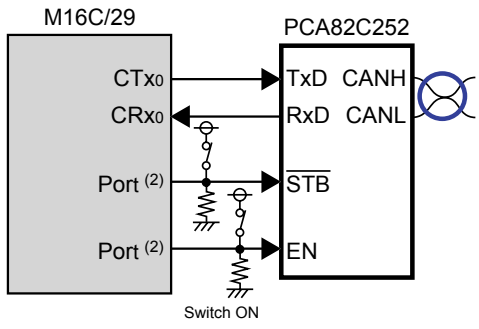
When programming the flash memory in boot mode via CAN bus, the operation mode of CAN transceiver should be set to “high-speed mode” or “normal operation mode”. If the operation mode is controlled by the MCU, CAN transceiver must be set the operation mode to “high-speed mode” or “normal operation mode” before programming the flash memory by changing the switch etc. **Tables 22.3 and 22.4** show pin connections of CAN transceiver.

Table 22.3 Pin Connections of CAN Transceiver (In case of PCA82C250: Philips product)

	Standby mode	High-speed mode
Rs pin (Note 1)	“H”	“L”
CAN communication	impossible	possible
Connection		

Note 1: The pin which controls the operation mode of CAN transceiver.
Note 2: Connect to enabled port to control CAN transceiver.

Table 22.4 Pin Connections of CAN Transceiver (In case of PCA82C252: Philips product)

	Sleep mode	Normal operation mode
$\overline{\text{STB}}$ pin (Note 1)	“L”	“H”
EN pin (Note 1)	“L”	“H”
CAN communication	impossible	possible
Connection		

Note 1: The pin which controls the operation mode of CAN transceiver.
Note 2: Connect to enabled port to control CAN transceiver.

22.14 Mask ROM Version

22.14.1 Internal ROM Area

In the masked ROM version, do not write to internal ROM area. Writing to the area may increase power consumption.

22.14.2 Reserved Bit

The b3 to b0 in addresses $0FFFFF_{16}$ are reserved bits. Set these bits to 1111_2.

Appendix 2. Functional Comparison

Appendix 2.1 Difference between M16C/28 Group and M16C/29 Group (Normal-ver.) (1)

Item	Description	M16C/28(Normal-ver.)	M16C/29(Normal-ver.)
Clock Generation Circuit	Clock output function (function of b1 to b0 bits in the CM0 register)	Not available (reserved bit)	Available (clock output function select bit)
Protection	Function of the PRC0 bit	Enable to set the CM0, CM1, CM2, POCR, PLC0 and PCLKR registers	Enable to set the CM0, CM1, CM2, POCR, PLC0, PCLKR and CCLKR registers
Interrupt	The IFSR20 bit setting in the IFSR2A register	Set to 1	Set to 0
	The b1 bit in the IFSR2A register	Not available (reseved bit)	Interrupt cause switching bit (0: A/D conversion, 1:key input)
	The b2 bit in the IFSR2A register	Not available (reseved bit)	Interrupt cause switching bit (0: CAN0 wake-up/ error)
	Interrupt cause in the Interrupt number 13	Key input interrupt	CAN0 error
	Interrupt cause in the Interrupt number 14	Key input interrupt	A/D, key input interrupt
Three-phase Motor Control Timer	Three-phase port switching function (function of 0358_{16})	Not available (reserved register)	Available (port function select register)
A/D	Number of A/D input pin	24 channels (excluding AN_{30} to AN_{32})	27 channels (including AN_{30} to AN_{32})
	Delayed trigger mode 0	Not available in the 1st chip version and chip version A	Available
	Delayed trigger mode 1	Not available in the 1st chip version and chip version A	Available
CAN module	compatible to 2.0B	Not available (all related registers are reserved registers)	Available (1 channel)
CRC Calculation	Available (compatible to CRC-CCITT and CRC-16 methods)	Not available (all related registers are reserved registers)	Available (1 circuit)
Pin Function	2 pins (80-pin/85-pin package), 62 pins (64-pin package)	$P9_3$/AN_{24}	$P9_3$/AN_{24}/CTX
	3 pins (80-pin/85-pin package), 64 pins (64-pin package)	$P9_2$/$TB2_{IN}$	$P9_2$/AN_{32}/$TB2_{IN}$/CRX
	4 pins (80-pin/85-pin package), 1 pin (64-pin package)	$P9_1$/$TB1_{IN}$	$P9_1$/AN_{31}/$TB1_{IN}$
	5 pins (80-pin/85-pin package), 2 pins (64-pin package)	$P9_0$/$TB0_{IN}$	$P9_0$/AN_{30}/$TB0_{IN}$/CLK_{OUT}
Flash Memory	$P9_3$ in standard serial I/O mode	I (other than 128 Kbyte version) I/O (128 Kbyte version)	CTX output

I: Input O: Output I/O: Input and output

NOTE:
1. Since the M16C/28 group uses the common emulator used in the M16C/29 group, all the functions are available for M16C/28. When evaluating M16C/28 group, do not access to the SFR which is not built-in the M16C/28 gorup. Refere to hardware manual for details and electrical characteristics.