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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	M16C/60
Core Size	16-Bit
Speed	20MHz
Connectivity	CANbus, I²C, IEBus, SIO, UART/USART
Peripherals	DMA, POR, PWM, Voltage Detect, WDT
Number of I/O	55
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30291fahp-u9a

4. List of Abbreviations and Acronyms

Abbreviation	Full Form
ACIA	Asynchronous Communication Interface Adapter
bps	bits per second
CRC	Cyclic Redundancy Check
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
GSM	Global System for Mobile Communications
Hi-Z	High Impedance
IEBus	Inter Equipment bus
I/O	Input/Output
IrDA	Infrared Data Association
LSB	Least Significant Bit
MSB	Most Significant Bit
NC	Non-Connection
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
SFR	Special Function Registers
SIM	Subscriber Identity Module
UART	Universal Asynchronous Receiver/Transmitter
VCO	Voltage Controlled Oscillator

Quick Reference to Pages Classified by Address

Address	Register	Symbol	Page
0100₁₆ 0101₁₆ 0102₁₆ 0103₁₆ 0104₁₆ 0105₁₆	CAN0 message box 10: Identifer/DLC		289
0106₁₆ 0107₁₆ 0108₁₆ 0109₁₆ 010A₁₆ 010B₁₆ 010C₁₆ 010D₁₆	CAN0 message box 10: Data field		289
010E₁₆ 010F₁₆	CAN0 message box 10: time stamp		289
0110₁₆ 0111₁₆ 0112₁₆ 0113₁₆ 0114₁₆ 0115₁₆	CAN0 message box 11: Identifier/DLC		289
0116₁₆ 0117₁₆ 0118₁₆ 0119₁₆ 011A₁₆ 011B₁₆ 011C₁₆ 011D₁₆	CAN0 message box 11: Data field		289
011E₁₆ 011F₁₆	CAN0 message box 11: time stamp		289
0120₁₆ 0121₁₆ 0122₁₆ 0123₁₆ 0124₁₆ 0125₁₆	CAN0 message box 12: Identifier/DLC		289
0126₁₆ 0127₁₆ 0128₁₆ 0129₁₆ 012A₁₆ 012B₁₆ 012C₁₆ 012D₁₆	CAN0 message box 12: Data field		289
012E₁₆ 012F₁₆	CAN0 message box 12: time stamp		289
0130₁₆ 0131₁₆ 0132₁₆ 0133₁₆ 0134₁₆ 0135₁₆	CAN0 message box 13: Identifier/DLC		289
0136₁₆ 0137₁₆ 0138₁₆ 0139₁₆ 013A₁₆ 013B₁₆ 013C₁₆ 013D₁₆	CAN0 message box 13: Data field		289
013E₁₆ 013F₁₆	CAN0 message box 13: time stamp		289

Address	Register	Symbol	Page
0140₁₆ 0141₁₆ 0142₁₆ 0143₁₆ 0144₁₆ 0145₁₆	CAN0 message box 14: Identifier/DLC		289
0146₁₆ 0147₁₆ 0148₁₆ 0149₁₆ 014A₁₆ 014B₁₆ 014C₁₆ 014D₁₆	CAN0 message box 14: Data field		289
014E₁₆ 014F₁₆	CAN0 message box 14: time stamp		289
0150₁₆ 0151₁₆ 0152₁₆ 0153₁₆ 0154₁₆ 0155₁₆	CAN0 message box 15: Identifier/DLC		289
0156₁₆ 0157₁₆ 0158₁₆ 0159₁₆ 015A₁₆ 015B₁₆ 015C₁₆ 015D₁₆	CAN0 message box 15: Data field		289
015E₁₆ 015F₁₆	CAN0 message box 15: time stamp		289
0160₁₆ 0161₁₆ 0162₁₆ 0163₁₆ 0164₁₆ 0165₁₆	CAN0 global mask register	C0GMR	291
0166₁₆ 0167₁₆ 0168₁₆ 0169₁₆ 016A₁₆ 016B₁₆	CAN0 local mask A register	C0LMAR	291
016C₁₆ 016D₁₆ 016E₁₆ 016F₁₆ 0170₁₆ 0171₁₆	CAN0 local mask B register	C0LMBR	291
0172₁₆			
0173₁₆			
0174₁₆			
0175₁₆			
0176₁₆			
0177₁₆			
0178₁₆			
0179₁₆			
017A₁₆			
017B₁₆			
017C₁₆			
017D₁₆			
017E₁₆			
017F₁₆			

Note: The blank areas are reserved and cannot be accessed by users.

Quick Reference to Pages Classified by Address

Address	Register	Symbol	Page
0380₁₆	Count start flag	TABSR	104, 118, 132
0381₁₆	Clock prescaler reset flag	CPSRF	105,118
0382₁₆	One-shot start flag	ONSF	105
0383₁₆	Trigger select register	TRGSR	105,132
0384₁₆	Up-down flag	UDF	104
0385₁₆			
0386₁₆ 0387₁₆	Timer A0 register	TA0	104
0388₁₆ 0389₁₆	Timer A1 register	TA1	104
038A₁₆ 038B₁₆	Timer A2 register	TA2	104
038C₁₆ 038D₁₆	Timer A3 register	TA3	104
038E₁₆ 038F₁₆	Timer A4 register	TA4	104
0390₁₆ 0391₁₆	Timer B0 register	TB0	118
0392₁₆ 0393₁₆	Timer B1 register	TB1	118
0394₁₆ 0395₁₆	Timer B2 register	TB2	118
0396₁₆	Timer A0 mode register	TA0MR	103
0397₁₆	Timer A1 mode register	TA1MR	133
0398₁₆	Timer A2 mode register	TA2MR	133
0399₁₆	Timer A3 mode register	TA3MR	103
039A₁₆	Timer A4 mode register	TA4MR	133
039B₁₆	Timer B0 mode register	TB0MR	117
039C₁₆	Timer B1 mode register	TB1MR	117
039D₁₆	Timer B2 mode register	TB2MR	133
039E₁₆	Timer B2 special mode register	TB2SC	131
039F₁₆			
03A0₁₆	UART0 transmit/receive mode register	U0MR	175
03A1₁₆	UART0 bit rate generator	U0BRG	174
03A2₁₆ 03A3₁₆	UART0 transmit buffer register	U0TB	174
03A4₁₆	UART0 transmit/receive control register 0	U0C0	176
03A5₁₆	UART0 transmit/receive control register 1	U0C1	177
03A6₁₆ 03A7₁₆	UART0 receive buffer register	U0RB	174
03A8₁₆	UART1 transmit/receive mode register	U1MR	175
03A9₁₆	UART1 bit rate generator	U1BRG	174
03AA₁₆ 03AB₁₆	UART1 transmit buffer register	U1TB	174
03AC₁₆	UART1 transmit/receive control register 0	U1C0	176
03AD₁₆	UART1 transmit/receive control register 1	U1C1	177
03AE₁₆ 03AF₁₆	UART1 receive buffer register	U1RB	174
03B0₁₆	UART transmit/receive control register 2	UCON	176
03B1₁₆			
03B2₁₆			
03B3₁₆			
03B4₁₆ 03B5₁₆	CRC snoop address register	CRCSAR	314
03B6₁₆	CRC mode register	CRCMR	314
03B7₁₆			
03B8₁₆	DMA0 request cause select register	DM0SL	93
03B9₁₆			
03BA₁₆	DMA1 request cause select register	DM1SL	94
03BB₁₆			
03BC₁₆ 03BD₁₆	CRC data register	CRCD	314
03BE₁₆	CRC input register	CRCIN	314
03BF₁₆			

Address	Register	Symbol	Page
03C0₁₆ 03C1₁₆	A/D register 0	AD0	226
03C2₁₆ 03C3₁₆	A/D register 1	AD1	226
03C4₁₆ 03C5₁₆	A/D register 2	AD2	226
03C6₁₆ 03C7₁₆	A/D register 3	AD3	226
03C8₁₆ 03C9₁₆	A/D register 4	AD4	226
03CA₁₆ 03CB₁₆	A/D register 5	AD5	226
03CC₁₆ 03CD₁₆	A/D register 6	AD6	226
03CE₁₆ 03CF₁₆	A/D register 7	AD7	226
03D0₁₆			
03D1₁₆			
03D2₁₆	A/D trigger control register	ADTRGCON	225
03D3₁₆	A/D convert status register 0	ADSTAT0	226
03D4₁₆	A/D control register 2	ADCON2	224
03D5₁₆			
03D6₁₆	A/D control register 0	ADCON0	224
03D7₁₆	A/D control register 1	ADCON1	224
03D8₁₆			
03D9₁₆			
03DA₁₆			
03DB₁₆			
03DC₁₆			
03DD₁₆			
03DE₁₆			
03DF₁₆			
03E0₁₆	Port P0 register	P0	324
03E1₁₆	Port P1 register	P1	324
03E2₁₆	Port P0 direction register	PD0	323
03E3₁₆	Port P1 direction register	PD1	323
03E4₁₆	Port P2 register	P2	324
03E5₁₆	Port P3 register	P3	324
03E6₁₆	Port P2 direction register	PD2	323
03E7₁₆	Port P3 direction register	PD3	323
03E8₁₆			
03E9₁₆			
03EA₁₆			
03EB₁₆			
03EC₁₆	Port P6 register	P6	324
03ED₁₆	Port P7 register	P7	324
03EE₁₆	Port P6 direction register	PD6	323
03EF₁₆	Port P7 direction register	PD7	323
03F0₁₆	Port P8 register	P8	324
03F1₁₆	Port P9 register	P9	324
03F2₁₆	Port P8 direction register	PD8	323
03F3₁₆	Port P9 direction register	PD9	323
03F4₁₆	Port P10 register	P10	324
03F5₁₆			
03F6₁₆	Port P10 direction register	PD10	323
03F7₁₆			
03F8₁₆			
03F9₁₆			
03FA₁₆			
03FB₁₆			
03FC₁₆	Pull-up control register 0	PUR0	325
03FD₁₆	Pull-up control register 1	PUR1	325
03FE₁₆	Pull-up control register 2	PUR2	325
03FF₁₆	Port control register	PCR	326

Note : The blank areas are reserved and cannot be accessed by users.

2.3 Frame Base Register (FB)

FB is configured with 16 bits, and is used for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is configured with 20 bits, indicating the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC is configured with 20 bits, indicating the address of an instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

Stack pointer (SP) comes in two types: USP and ISP, each configured with 16 bits.

Your desired type of stack pointer (USP or ISP) can be selected by the U flag of FLG.

2.7 Static Base Register (SB)

SB is configured with 16 bits, and is used for SB relative addressing.

2.8 Flag Register (FLG)

FLG consists of 11 bits, indicating the CPU status.

2.8.1 Carry Flag (C Flag)

This flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic/logic unit.

2.8.2 Debug Flag (D Flag)

The D flag is used exclusively for debugging purpose. During normal use, it must be set to 0.

2.8.3 Zero Flag (Z Flag)

This flag is set to 1 when an arithmetic operation resulted in 0; otherwise, it is 0.

2.8.4 Sign Flag (S Flag)

This flag is set to 1 when an arithmetic operation resulted in a negative value; otherwise, it is 0.

2.8.5 Register Bank Select Flag (B Flag)

Register bank 0 is selected when this flag is 0 ; register bank 1 is selected when this flag is 1.

2.8.6 Overflow Flag (O Flag)

This flag is set to 1 when the operation resulted in an overflow; otherwise, it is 0.

2.8.7 Interrupt Enable Flag (I Flag)

This flag enables a maskable interrupt.

Maskable interrupts are disabled when the I flag is 0, and are enabled when the I flag is 1.

The I flag is cleared to 0 when the interrupt request is accepted.

2.8.8 Stack Pointer Select Flag (U Flag)

ISP is selected when the U flag is 0; USP is selected when the U flag is 1.

The U flag is cleared to 0 when a hardware interrupt request is accepted or an INT instruction for software interrupt Nos. 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is configured with three bits, for specification of up to eight processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has priority greater than IPL, the interrupt is enabled.

2.8.10 Reserved Area

When write to this bit, write 0. When read, its content is undefined.

Table 4.2 SFR Information (2)

Address	Register	Symbol	After reset
0040₁₆			
0041₁₆	CAN0 wakeup interrupt control register	C01WKIC	XXXXX000₂
0042₁₆	CAN0 successful reception interrupt control register	C0RECIC	XXXXX000₂
0043₁₆	CAN0 successful transmission interrupt control register	C0TRMIC	XXXXX000₂
0044₁₆	INT3 interrupt control register	INT3IC	XX00X000₂
0045₁₆	ICOC 0 interrupt control register	ICOC0IC	XXXXX000₂
0046₁₆	ICOC 1 interrupt control register, I^2C bus interface interrupt control register 1	ICOC1IC,IICIC	XXXXX000₂
0047₁₆	ICOC base timer interrupt control register, SCL/SDA interrupt control register 2	BTIC,SCLDAIC	XXXXX000₂
0048₁₆	SI/O4 interrupt control register, INT5 interrupt control register	S4IC, INT5IC	XX00X000₂
0049₁₆	SI/O3 interrupt control register, INT4 interrupt control register	S3IC, INT4IC	XX00X000₂
004A₁₆	UART2 Bus collision detection interrupt control register	BCNIC	XXXXX000₂
004B₁₆	DMA0 interrupt control register	DM0IC	XXXXX000₂
004C₁₆	DMA1 interrupt control register	DM1IC	XXXXX000₂
004D₁₆	CAN0 error interrupt control register	C01ERRIC	XXXXX000₂
004E₁₆	A/D conversion interrupt control register, Key input interrupt control register (Note 2)	ADIC, KUPIC	XXXXX000₂
004F₁₆	UART2 transmit interrupt control register	S2TIC	XXXXX000₂
0050₁₆	UART2 receive interrupt control register	S2RIC	XXXXX000₂
0051₁₆	UART0 transmit interrupt control register	S0TIC	XXXXX000₂
0052₁₆	UART0 receive interrupt control register	S0RIC	XXXXX000₂
0053₁₆	UART1 transmit interrupt control register	S1TIC	XXXXX000₂
0054₁₆	UART1 receive interrupt control register	S1RIC	XXXXX000₂
0055₁₆	TimerA0 interrupt control register	TA0IC	XXXXX000₂
0056₁₆	TimerA1 interrupt control register	TA1IC	XXXXX000₂
0057₁₆	TimerA2 interrupt control register	TA2IC	XXXXX000₂
0058₁₆	TimerA3 interrupt control register	TA3IC	XXXXX000₂
0059₁₆	TimerA4 interrupt control register	TA4IC	XXXXX000₂
005A₁₆	TimerB0 interrupt control register	TB0IC	XXXXX000₂
005B₁₆	TimerB1 interrupt control register	TB1IC	XXXXX000₂
005C₁₆	TimerB2 interrupt control register	TB2IC	XXXXX000₂
005D₁₆	INT0 interrupt control register	INT0IC	XX00X000₂
005E₁₆	INT1 interrupt control register	INT1IC	XX00X000₂
005F₁₆	INT2 interrupt control register	INT2IC	XX00X000₂
0060₁₆	CAN0 message box 0: Identifier/DLC		XX₁₆
0061₁₆			XX₁₆
0062₁₆			XX₁₆
0063₁₆			XX₁₆
0064₁₆			XX₁₆
0065₁₆			XX₁₆
0066₁₆	CAN0 message box 0 : Data field		XX₁₆
0067₁₆			XX₁₆
0068₁₆			XX₁₆
0069₁₆			XX₁₆
006A₁₆			XX₁₆
006B₁₆			XX₁₆
006C₁₆			XX₁₆
006D₁₆			XX₁₆
006E₁₆	CAN0 message box 0 : Time stamp		XX₁₆
006F₁₆			XX₁₆
0070₁₆	CAN0 message box 1 : Identifier/DLC		XX₁₆
0071₁₆			XX₁₆
0072₁₆			XX₁₆
0073₁₆			XX₁₆
0074₁₆			XX₁₆
0075₁₆			XX₁₆
0076₁₆	CAN0 message box 1 : Data field		XX₁₆
0077₁₆			XX₁₆
0078₁₆			XX₁₆
0079₁₆			XX₁₆
007A₁₆			XX₁₆
007B₁₆			XX₁₆
007C₁₆			XX₁₆
007D₁₆			XX₁₆
007E₁₆	CAN0 message box 1 : Time stamp		XX₁₆
007F₁₆			XX₁₆

Note 1: The blank areas are reserved and cannot be used by users.
Note 2: A/D conversion interrupt control register is effective when the bit1(Interrupt source select register (address 35Eh IFSR2A) is set to "0". Key input interrupt control register is effective when the bit1 is set to "1".
X : Undefined

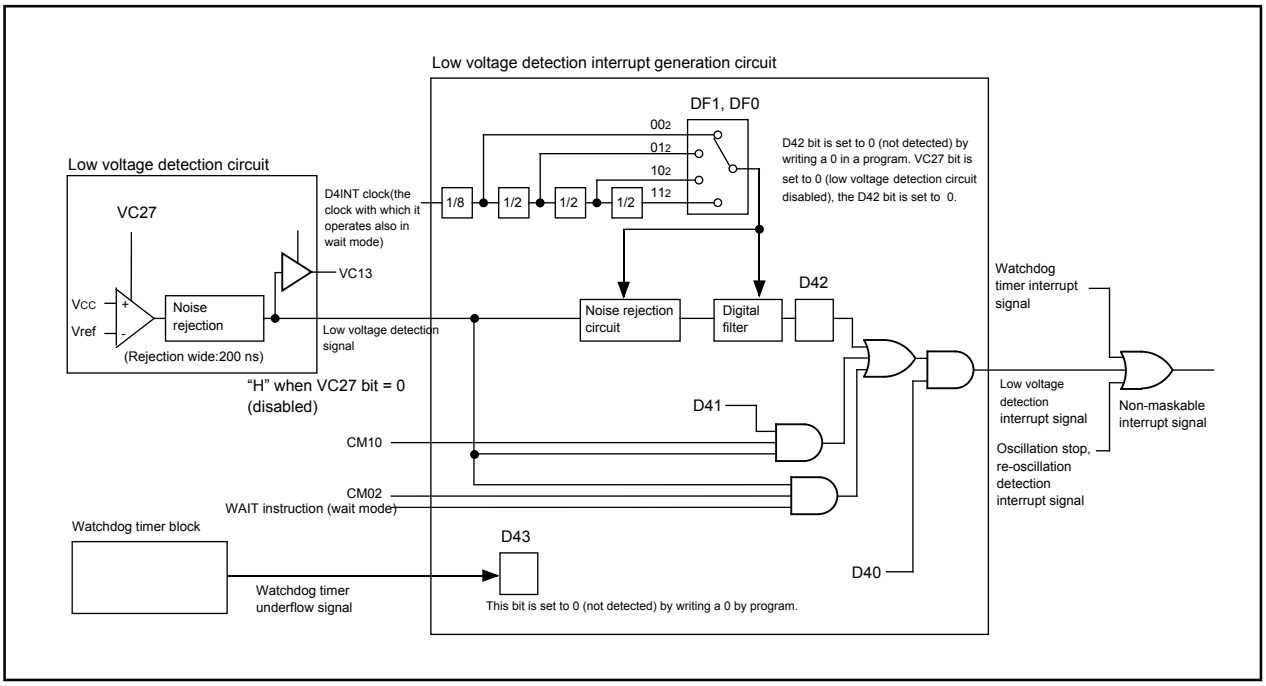
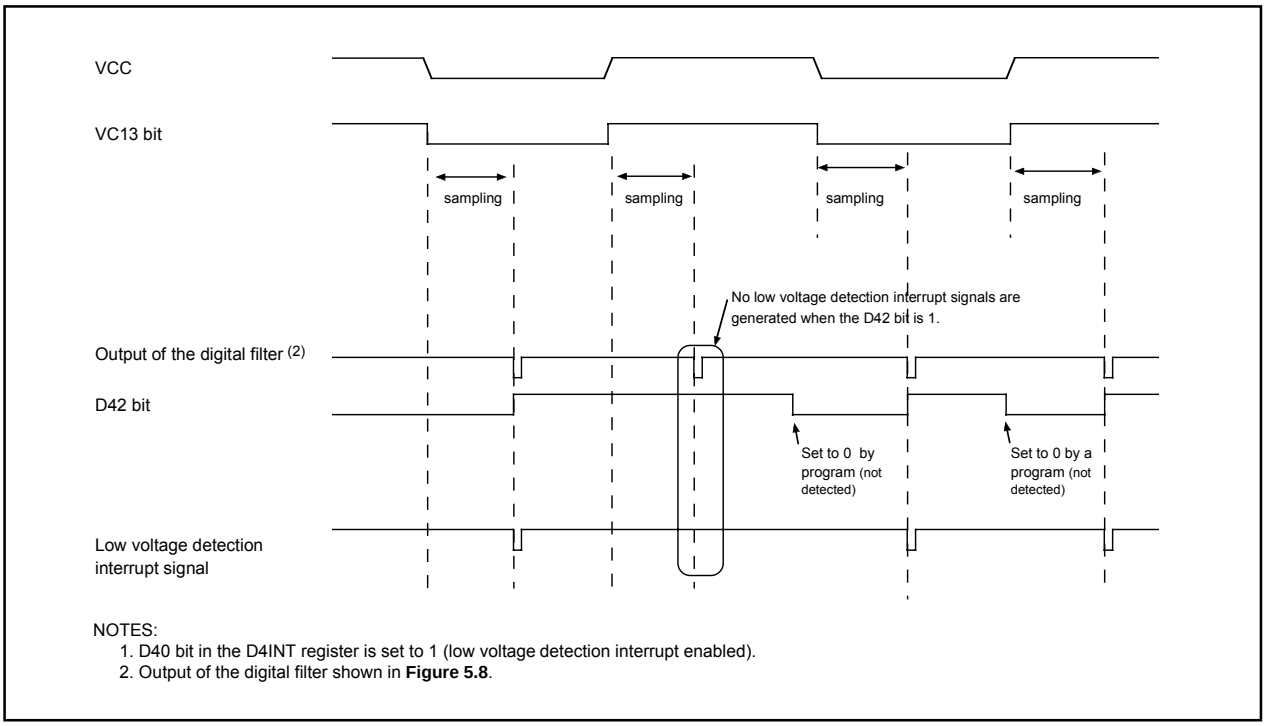


Figure 5.8 Low Voltage Detection Interrupt Generation Block



NOTES:
1. D40 bit in the D4INT register is set to 1 (low voltage detection interrupt enabled).
2. Output of the digital filter shown in **Figure 5.8**.

Figure 5.9 Low voltage Detection Interrupt Generation Circuit Operation Example

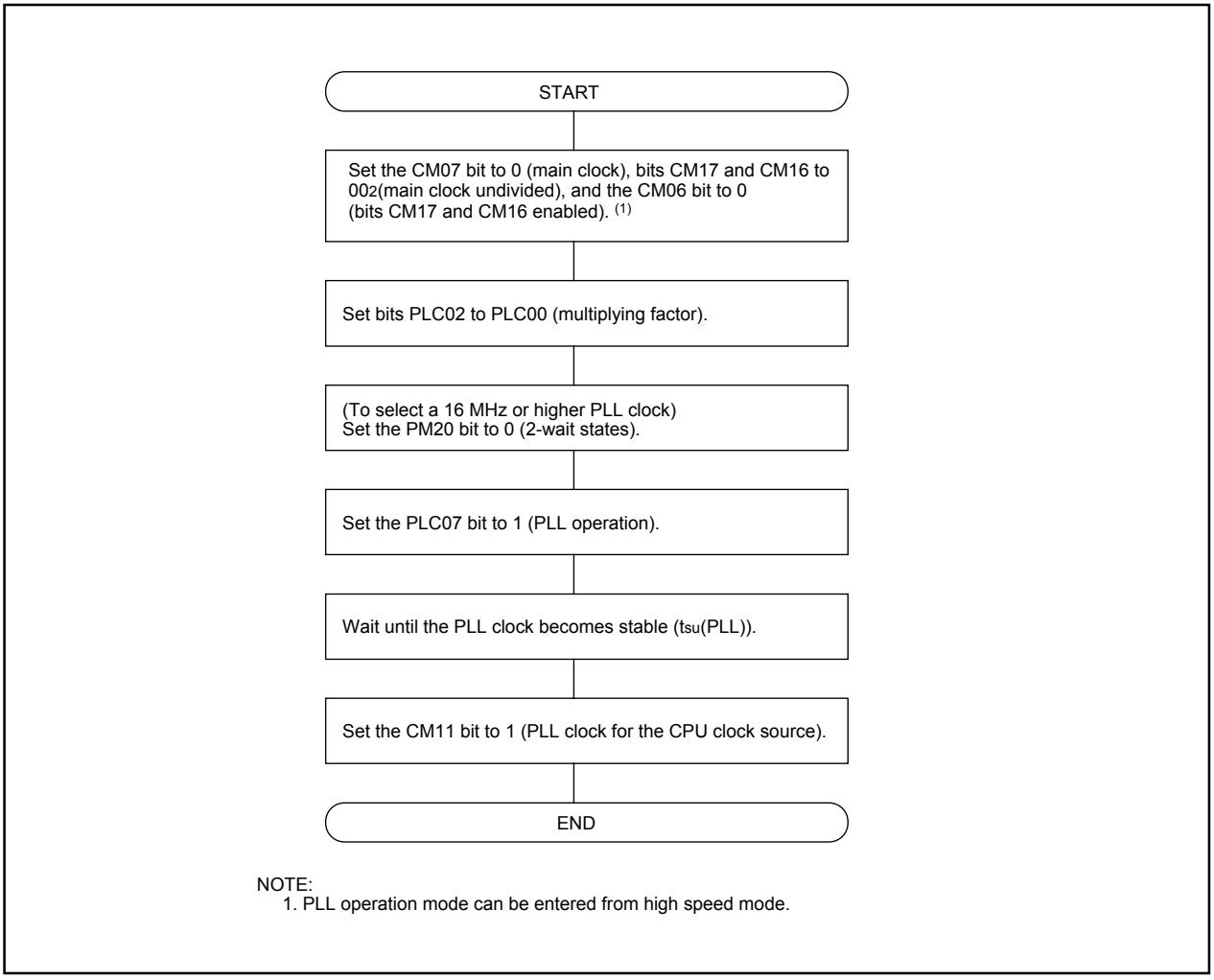


Figure 7.10 Procedure to Use PLL Clock as CPU Clock Source

9.2.2 Relocatable Vector Tables

The 256 bytes beginning with the start address set in the INTB register comprise a reloacatable vector table area. **Table 9.2** lists the relocatable vector tables. Setting an even address in the INTB register results in the interrupt sequence being executed faster than in the case of odd addresses.

Table 9.2 Relocatable Vector Tables

Interrupt source	Vector address (1) Address (L) to address (H)	Software interrupt number	Reference
BRK instruction (2)	+0 to +3 (0000 16 to 0003 16)	0	M16C/60, M16C/20 series software manual
CAN0 wakeup (3)	+4 to +7 (0004 16 to 0007 16)	1	CAN module
CAN0 receive completion	+8 to +11 (0008 16 to 000B 16)	2	
CAN0 transmit completion	+12 to +15 (000C 16 to 000F 16)	3	
$\overline{INT3}$	+16 to +19 (0010 16 to 0013 16)	4	$\overline{INT}$ interrupt
IC/OC interrupt 0	+20 to +23 (0014 16 to 0017 16)	5	Timer S
IC/OC interrupt 1, I2C bus interface (4)	+24 to +27 (0018 16 to 001B 16)	6	Timer S Multi-Master I2C bus interface
IC/OC base timer, SCL/SDA (4)	+28 to +31 (001C 16 to 001F 16)	7	
SI/O4, $\overline{INT5}$ (5)	+32 to +35 (0020 16 to 0023 16)	8	$\overline{INT}$ interrupt
SI/O3, $\overline{INT4}$ (5)	+36 to +39 (0024 16 to 0027 16)	9	Serial I/O
UART 2 bus collision detection (6)	+40 to +43 (0028 16 to 002B 16)	10	Serial I/O
DMA0	+44 to +47 (002C 16 to 002F 16)	11	DMAC
DMA1	+48 to +51 (0030 16 to 0033 16)	12	
CAN0 state, error	+52 to +55 (0034 16 to 0037 16)	13	CAN module
A/D, Key input interrupt (7)	+56 to +59 (0038 16 to 003B 16)	14	A/D convertor, Key input interrupt
UART2 transmit, NACK2 (8)	+60 to +63 (003C 16 to 003F 16)	15	Serial I/O
UART2 receive, ACK2 (8)	+64 to +67 (0040 16 to 0043 16)	16	
UART0 transmit	+68 to +71 (0044 16 to 0047 16)	17	
UART0 receive	+72 to +75 (0048 16 to 004B 16)	18	
UART1 transmit	+76 to +79 (004C 16 to 004F 16)	19	
UART1 receive	+80 to +83 (0050 16 to 0053 16)	20	
Timer A0	+84 to +87 (0054 16 to 0057 16)	21	Timer
Timer A1	+88 to +91 (0058 16 to 005B 16)	22	
Timer A2	+92 to +95 (005C 16 to 005F 16)	23	
Timer A3	+96 to +99 (0060 16 to 0063 16)	24	
Timer A4	+100 to +103 (0064 16 to 0067 16)	25	
Timer B0	+104 to +107 (0068 16 to 006B 16)	26	
Timer B1	+108 to +111 (006C 16 to 006F 16)	27	
Timer B2	+112 to +115 (0070 16 to 0073 16)	28	
$\overline{INT0}$	+116 to +119 (0074 16 to 0077 16)	29	$\overline{INT}$ interrupt
$\overline{INT1}$	+120 to +123 (0078 16 to 007B 16)	30	
$\overline{INT2}$	+124 to +127 (007C 16 to 007F 16)	31	
Software interrupt (2)	+128 to +131 (0080 16 to 0083 16) to +252 to +255 (00FC 16 to 00FF 16)	32 to 63	M16C/60, M16C/20 series software manual

NOTES:
1. Address relative to address in INTB.
2. These interrupts cannot be disabled using the I flag.
3. Set the IFSR22 bit in the IFSR register to 0.
4. Use bits IFSR26 and IFSR27 in the IFSR2A register to select.
5. Use bits IFSR6 and IFSR7 in the IFSR register to select.
6. Bus collision detection: In IEBus mode, this bus collision detection constitutes the cause of an interrupt. In I2C bus mode, however, a start condition or a stop condition detection constitutes the cause of an interrupt.
7. Use the IFSR21 bit in the IFSR2A register to select.
8. During I2C bus mode, NACK and ACK interrupts comprise the interrupt source.

Timer Ai Mode Register (i=2 to 4)
(When using two-phase pulse signal processing)

b6	b5	b4	b3	b2	b1	b0
		0	1	0	0	0	1

Symbol	Address	After Reset
TA2MR to TA4MR	0398_{16} to $039A_{16}$	00_{16}

Bit Symbol	Bit Name	Function	RW
TMOD0	Operation mode select bit	$^{b1\ b0}$ 0 1: Event counter mode	RW
TMOD1			RW
MR0	To use two-phase pulse signal processing, set this bit to 0		RW
MR1	To use two-phase pulse signal processing, set this bit to 0		RW
MR2	To use two-phase pulse signal processing, set this bit to 1		RW
MR3	To use two-phase pulse signal processing, set this bit to 0		RW
TCK0	Count operation type select bit	0: Reload type 1: Free-run type	RW
TCK1	Two-phase pulse signal processing operation select bit (1)(2)	0: Normal processing operation 1: Multiply-by-4 processing operation	RW

NOTES:
1. The TCK1 bit is valid for timer A3 mode register. No matter how this bit is set, timers A2 and A4 always operate in normal processing mode and x4 processing mode, respectively.
2. If two-phase pulse signal processing is desired, following register settings are required:
   - Set the TAiP bit in the UDF register to 1 (two-phase pulse signal processing function enabled).
   - Set bits TAiTGH and TAiTGL in the TRGSR register to 00_2 (TAiIN pin input).
   - Set the port direction bits for TAiIN and TAiOUT to 0 (input mode).

Figure 12.9 TA2MR to TA4MR Registers in Event Counter Mode (when using two-phase pulse signal processing with timer A2, A3 or A4)

12.2.3 Pulse Period and Pulse Width Measurement Mode

In pulse period and pulse width measurement mode, the timer measures pulse period or pulse width of an external signal (see **Table 12.8**). **Figure 12.20** shows the TBiMR register in pulse period and pulse width measurement mode. **Figure 12.21** shows the operation timing when measuring a pulse period. **Figure 12.22** shows the operation timing when measuring a pulse width.

Table 12.8 Specifications in Pulse Period and Pulse Width Measurement Mode

Item	Specification
Count source	f_1, f_2, f_8, f_{32}, f_{C32}
Count operation	• Increment • Counter value is transferred to reload register at an effective edge of measurement pulse. The counter value is set to 0000_{16} to continue counting.
Count start condition	Set TBiS (i=0 to 2) bit (3) to 1 (start counting)
Count stop condition	Set TBiS bit to 0 (stop counting)
Interrupt request generation timing	• When an effective edge of measurement pulse is input (1) • Timer overflow. When an overflow occurs, MR3 bit in the TBiMR register is set to 1 (overflowed) simultaneously. MR3 bit is cleared to 0 (no overflow) by writing to TBiMR register at the next count timing or later after MR3 bit was set to 1. At this time, make sure TBiS bit is set to 1 (start counting).
TBi_{IN} pin function	Measurement pulse input
Read from timer	Contents of the reload register (measurement result) can be read by reading TBi register (2)
Write to timer	Value written to TBi register is written to neither reload register nor counter

NOTES:
1. Interrupt request is not generated when the first effective edge is input after the timer started counting.
2. Value read from TBi register is undefined until the second valid edge is input after the timer starts counting.
3. Bits TB0S to TB2S are assigned to the bit 5 to bit 7 in the TABSR register .

Timer Bi Mode Register (i=0 to 2)

b7	b6	b5	b4	b3	b2	b1	b0
						1	0

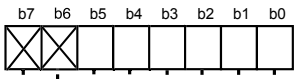
Symbol	Address	After Reset
TB0MR to TB2MR	$039B_{16}$ to $039D_{16}$	$00XX0000_2$

Bit Symbol	Bit Name	Function	RW
TMOD0	Operation mode select bit	b1 b0 1 0 : Pulse period / pulse width measurement mode	RW
TMOD1			RW
MR0	Measurement mode select bit	b3 b2 0 0: Pulse period measurement (Measurement between a falling edge and the next falling edge of measured pulse) 0 1: Pulse period measurement (Measurement between a rising edge and the next rising edge of measured pulse) 1 0: Pulse width measurement (Measurement between a falling edge and the next rising edge of measured pulse and between a rising edge and the next falling edge) 1 1: Do not set.	RW
MR1			RW
MR2	TB0MR register Set to 0 in pulse period and pulse width measurement mode		RW
	TB1MR, TB2MR registers Nothing is assigned. If necessary, set to 0. When read, its content is undefined		—
MR3	Timer Bi overflow flag (1)	0 : Timer did not overflow 1 : Timer has overflowed	RO
TCK0	Count source select bit	b7 b6 0 0: f_1 or f_2 0 1: f_8 1 0: f_{32} 1 1: f_{C32}	RW
TCK1			RW

NOTE:
1.This flag is undefined after reset. When the TBiS bit is set to 1 (start counting), the MR3 bit is cleared to 0 (no overflow) by writing to the TBiMR register at the next count timing or later after the MR3 bit was set to 1 (overflowed). The MR3 bit cannot be set to 1 by program. Bits TB0S to TB2S are assigned to the bit 5 to bit 7 in the TABSR register.

Figure 12.20 TBiMR Register in Pulse Period and Pulse Width Measurement Mode

Port Function Control Register (1)

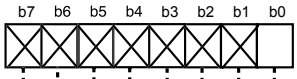


Symbol	Address	After Reset
PFCR	0358_{16}	$0011\ 1111_2$

Bit Symbol	Bit Name	Function	RW
PFC0	Port $P8_0$ output function select bit	0: Input/Output port $P8_0$ 1: Three-phase PWM output (U phase output)	RW
PFC1	Port $P8_1$ output function select bit	0: Input/Output port $P8_1$ 1: Three-phase PWM output ($\overline{U}$ phase output)	RW
PFC2	Port $P7_2$ output function select bit	0: Input/Output port $P7_2$ 1: Three-phase PWM output (V phase output)	RW
PFC3	Port $P7_3$ output function select bit	0: Input/Output port $P7_3$ 1: Three-phase PWM output ($\overline{V}$ phase output)	RW
PFC4	Port $P7_4$ output function select bit	0: Input/Output port $P7_4$ 1: Three-phase PWM output (W phase output)	RW
PFC5	Port $P7_5$ output function select bit	0: Input/Output port $P7_5$ 1: Three-phase PWM output ($\overline{W}$ phase output)	RW
$\overline{\text{(b7-b6)}}$	Nothing is assigned. If necessary, set to 0. When read, the contents are 0		—

NOTE:
1. This register is valid only when the INVC03 bit in the INVC0 register is 1 (Three-phase motor control timer.

Three-phase Protect Control Register



Symbol	Address	After Reset
TPRC	$025A_{16}$	00_{16}

Bit Symbol	Bit Name	Function	RW
TPRC0	Three-phase protect control bit	Enable write to PFCR register 0: Write protected 1: Write enabled	RW
$\overline{\text{(b7-b1)}}$	Nothing is assigned. If necessary, set to 0. When read, the contents are 0		—

Figure 12.38 PFCR Register, and TPRC Register

14.1.1.1 Counter Measure for Communication Error Occurs

If a communication error occurs while transmitting or receiving in clock synchronous serial I/O mode, follow the procedures below.

•Resetting the UiRB register (i=0 to 2)

(1) Set the RE bit in the UiC1 register to 0 (reception disabled)

(2) Set bits SMD2 to SMD0 in the UiMR register to 000_2 (Serial I/O disabled)

(3) Set bits SMD2 to SMD0 in the UiMR register to 001_2 (Clock synchronous serial I/O mode)

(4) Set the RE bit in the UiC1 register to 1 (reception enabled)

•Resetting the UiTB register (i=0 to 2)

(1) Set bits SMD2 to SMD0 in the UiMR register to 000_2 (Serial I/O disabled)

(2) Set bits SMD2 to SMD0 in the UiMR register to 001_2 (Clock synchronous serial I/O mode)

(3) 1 is written to TE bit in the UiC1 register (reception enabled), regardless to the TE bit.

14.1.3.1 Detection of Start and Stop Condition

Whether a start or a stop condition has been detected is determined.

A start condition-detected interrupt request is generated when the SDA2 pin changes state from high to low while the SCL2 pin is in the high state. A stop condition-detected interrupt request is generated when the SDA2 pin changes state from low to high while the SCL2 pin is in the high state.

Because the start and stop condition-detected interrupts share the interrupt control register and vector, check the BBS bit in the U2SMR register to determine which interrupt source is requesting the interrupt.

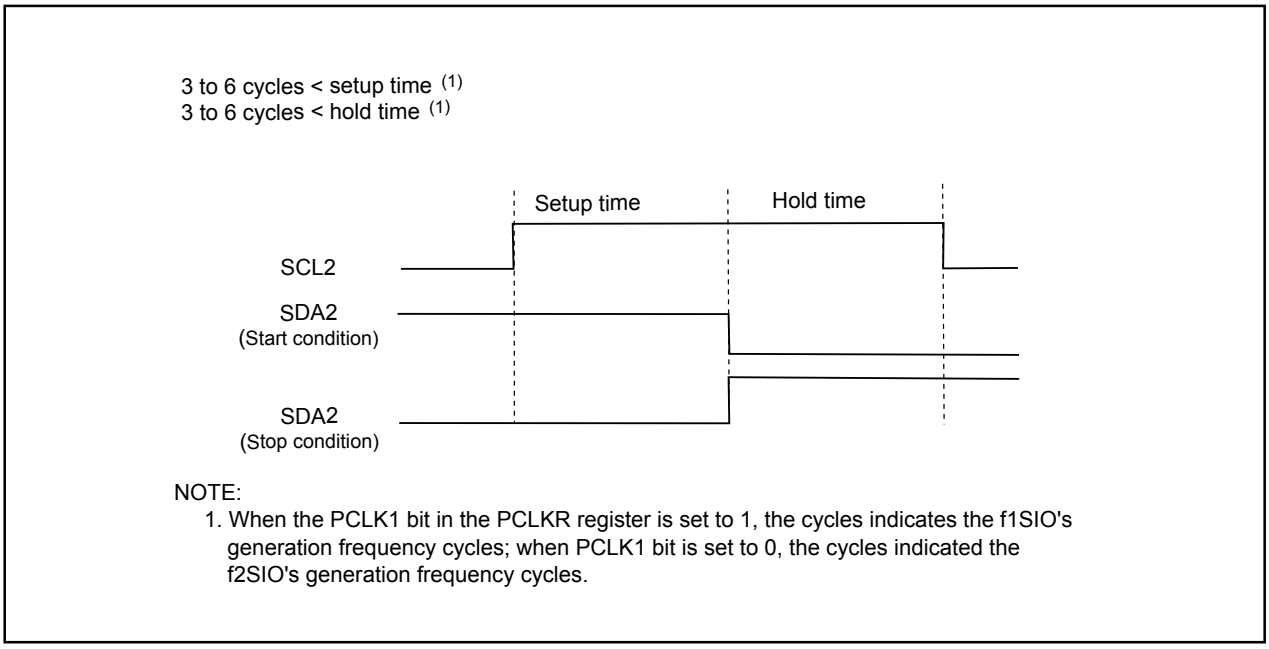


Figure 14.24 Detection of Start and Stop Condition

14.1.3.2 Output of Start and Stop Condition

A start condition is generated by setting the STAREQ bit in the U2SMR4 register to 1 (start).

A restart condition is generated by setting the RSTAREQ bit in the U2SMR4 register to 1 (start).

A stop condition is generated by setting the STPREQ bit in the U2SMR4 register to 1 (start).

The output procedure is described below.

(1) Set the STAREQ bit, RSTAREQ bit or STPREQ bit to 1 (start).

(2) Set the STSPSEL bit in the U2SMR4 register to 1 (output).

Make sure that no interrupts or DMA transfers will occur between (1) and (2).

The function of the STSPSEL bit is shown in **Table 14.14** and **Figure 14.25**.

15.1.8 Delayed Trigger Mode 1

In delayed trigger mode 1, analog voltages applied to the selected pins are converted one-by-one to a digital code. When the input of the $\overline{\text{ADTRG}}$ pin (falling edge) changes state from "H" to "L", a single sweep conversion is started. After completing the AN_0 pin conversion, the AN_1 pin is not sampled and converted until the second $\overline{\text{ADTRG}}$ pin falling edge is generated. When the second $\overline{\text{ADTRG}}$ falling edge is generated, the single sweep conversion of the pins after the AN_1 pin is restarted. **Table 15.12** shows the delayed trigger mode 1 specifications. **Figure 15.24** shows the operation example of delayed trigger mode 1. **Figure 15.25** and **15.26** show each flag operation in the ADSTAT0 register that corresponds to the operation example. **Figure 15.27** shows registers ADCON0 to ADCON2 in delayed trigger mode 1. **Figure 15.28** shows the ADTRGCON register in delayed trigger mode 1. **Table 15.13** shows the trigger select bit setting in delayed trigger mode 1.

Table 15.12 Delayed Trigger Mode 1 Specifications

Item	Specification
Function	Bits SCAN1 and SCAN0 in the ADCON1 register and bits ADGSEL1 and ADGSEL0 in the ADCON2 register select pins. Analog voltages applied to the selected pins are converted one-by-one to a digital code. At this time, the $\overline{\text{ADTRG}}$ pin falling edge starts AN_0 pin conversion and the second $\overline{\text{ADTRG}}$ pin falling edge starts conversion of the pins after AN_1 pin
A/D Conversion Start Condition	AN_0 pin conversion start condition The $\overline{\text{ADTRG}}$ pin input changes state from "H" to "L" (falling edge) (1) AN_1 pin conversion start condition (2) The $\overline{\text{ADTRG}}$ pin input changes state from "H" to "L" (falling edge) •When the second $\overline{\text{ADTRG}}$ pin falling edge is generated during A/D conversion of the AN_0 pin, input voltage of AN_1 pin is sampled or after at the time of $\overline{\text{ADTRG}}$ falling edge. The conversion of AN_1 and the rest of the sweep starts when AN_0 conversion is completed. •When the $\overline{\text{ADTRG}}$ pin falling edge is generated again during single sweep conversion of pins after the AN_1 pin, the conversion is not affected
A/D Conversion Stop Condition	•A/D conversion completed •Set the ADST bit to 0 (A/D conversion halted) (3)
Interrupt Request Generation Timing	Single sweep conversion completed
Analog Input Pin	Select from AN_0 to AN_1 (2 pins), AN_0 to AN_3 (4 pins), AN_0 to AN_5 (6 pins) and AN_0 to AN_7 (8 pins) (4)
Readout of A/D Conversion Result	Readout one of registers AN0 to AN7 that corresponds to the selected pins

NOTES:

1. Do not generate the next $\overline{\text{ADTRG}}$ pin falling edge after the AN1 pin conversion is started until all selected pins complete A/D conversion. When an $\overline{\text{ADTRG}}$ pin falling edge is generated again during A/D conversion, its trigger is ignored. The falling edge of $\overline{\text{ADTRG}}$ pin, which was input after all selected pins complete A/D conversion, is considered to be the next AN0 pin conversion start condition.
2. The $\overline{\text{ADTRG}}$ pin falling edge is detected synchronized with the operation clock fAD. Therefore, when the $\overline{\text{ADTRG}}$ pin falling edge is generated in shorter periods than fAD, the second $\overline{\text{ADTRG}}$ pin falling edge may not be detected. Do not generate the $\overline{\text{ADTRG}}$ pin falling edge in shorter periods than fAD.
3. Do not write 1 (A/D conversion started) to the ADST bit in delayed trigger mode 1. When write 1,unexpected interrupts may be generated.
4. $AN0_0$ to $AN0_7$, $AN2_0$ to $AN2_7$, and $AN3_0$ to $AN3_2$ can be used in the same way as AN_0 to AN_7. However, all input pins need to belong to the same group.

17.1 CAN Module-Related Registers

The CAN0 module has the following registers.

(1) CAN Message Box

A CAN module is equipped with 16 slots (16 bytes or 8 words each). Slots 14 and 15 can be used as Basic CAN.

- Priority of the slots: The smaller the number of the slot, the higher the priority, in both transmission and reception.
- A program can define whether a slot is defined as transmitter or receiver.

(2) Acceptance Mask Registers

A CAN module is equipped with 3 masks for the acceptance filter.

- CAN0 global mask register (C0GMR register: 6 bytes)
  Configuration of the masking condition for acceptance filtering processing to slots 0 to 13
- CAN0 local mask A register (C0LMAR register: 6 bytes)
  Configuration of the masking condition for acceptance filtering processing to slot 14
- CAN0 local mask B register (C0LMBR register: 6 bytes)
  Configuration of the masking condition for acceptance filtering processing to slot 15

(3) CAN SFR Registers

- CAN0 message control register j (C0MCTLj register: 8 bits × 16) (j = 0 to 15)
  Control of transmission and reception of a corresponding slot
- CANi control register (CiCTLR register: 16 bits) (i = 0, 1)
  Control of the CAN protocol
- CAN0 status register (C0STR register: 16 bits)
  Indication of the protocol status
- CAN0 slot status register (C0SSTR register: 16 bits)
  Indication of the status of contents of each slot
- CAN0 interrupt control register (C0ICR register: 16 bits)
  Selection of “interrupt enabled or disabled” for each slot
- CAN0 extended ID register (C0IDR register: 16 bits)
  Selection of ID format (standard or extended) for each slot
- CAN0 configuration register (C0CONR register: 16 bits)
  Configuration of the bus timing
- CAN0 receive error count register (C0RECR register: 8 bits)
  Indication of the error status of the CAN module in reception: the counter value is incremented or decremented according to the error occurrence.
- CAN0 transmit error count register (C0TECR register: 8 bits)
  Indication of the error status of the CAN module in transmission: the counter value is incremented or decremented according to the error occurrence.
- CAN0 time stamp register (C0TSR register: 16 bits)
  Indication of the value of the time stamp counter
- CAN0 acceptance filter support register (C0AFS register: 16 bits)
  Decoding the received ID for use by the acceptance filter support unit

Explanation of each register is given as follows.

20.3 Functions To Prevent Flash Memory from Rewriting

The flash memory has a built-in ROM code protect function for parallel I/O mode and a built-in ID code check function for standard input/output mode to prevent the flash memory from reading or rewriting.

20.3.1 ROM Code Protect Function

The ROM code protect function disables reading or changing the contents of the on-chip flash memory in parallel I/O mode. **Figure 20.4** shows the ROMCP address. The ROMCP address is located in a user ROM area. To enable ROM code protect, set the ROMCP1 bit to "00_2", "01_2", or "10_2" and set the bit 5 to bit 0 to "111111_2".

To cancel ROM code protect, erase the block including the the ROMCP register in CPU rewrite mode or standard serial I/O mode.

20.3.2 ID Code Check Function

Use the ID code check function in standard serial input/output mode. Unless the flash memory is blank, the ID code sent from the programmer and the 7-byte ID code written in the flash memory are compared for match. If the ID codes do not match, the commands sent from the programmer are not acknowledged. The ID code consists of 8-bit data, starting with the first byte, into addresses, $0FFFDF_{16}$, $0FFFE3_{16}$, $0FFFEB_{16}$, $0FFFEF_{16}$, $0FFFF3_{16}$, $0FFFF7_{16}$, and $0FFFFB_{16}$. The flash memory must have a program with the ID code set in these addresses.

20.4.1 EW Mode 0

The MCU enters CPU rewrite mode by setting the FMR01 bit in the FMR0 register to 1 (CPU rewrite mode enabled) and is ready to accept software commands. EW mode 0 is selected by setting the FMR11 bit in the FMR1 register to 0.

To set the FMR01 bit to 1, set to 1 after first writing 0. The software commands control programming and erasing. The FMR0 register or the status register indicates whether a programming or erasing operations is completed.

When entering the erase-suspend during the auto-erasing, set the FMR40 bit to 1 (erase-suspend enabled) and the FMR41 bit to 1 (suspend request). After waiting for td(SR-ES) and verifying the FMR46 bit is set to 1 (auto-erase stop), access to the user ROM area. When setting the FMR41 bit to 0 (erase restart), auto-erasing is restarted.

20.4.2 EW Mode 1

EW mode 1 is selected by setting the FMR11 bit to 1 after the FMR01 bit is set to 1 (set to 1 after first writing 0).

The FMR0 register indicates whether or not a programming or an erasing operation is completed. Read status register cannot be read in EW mode 1.

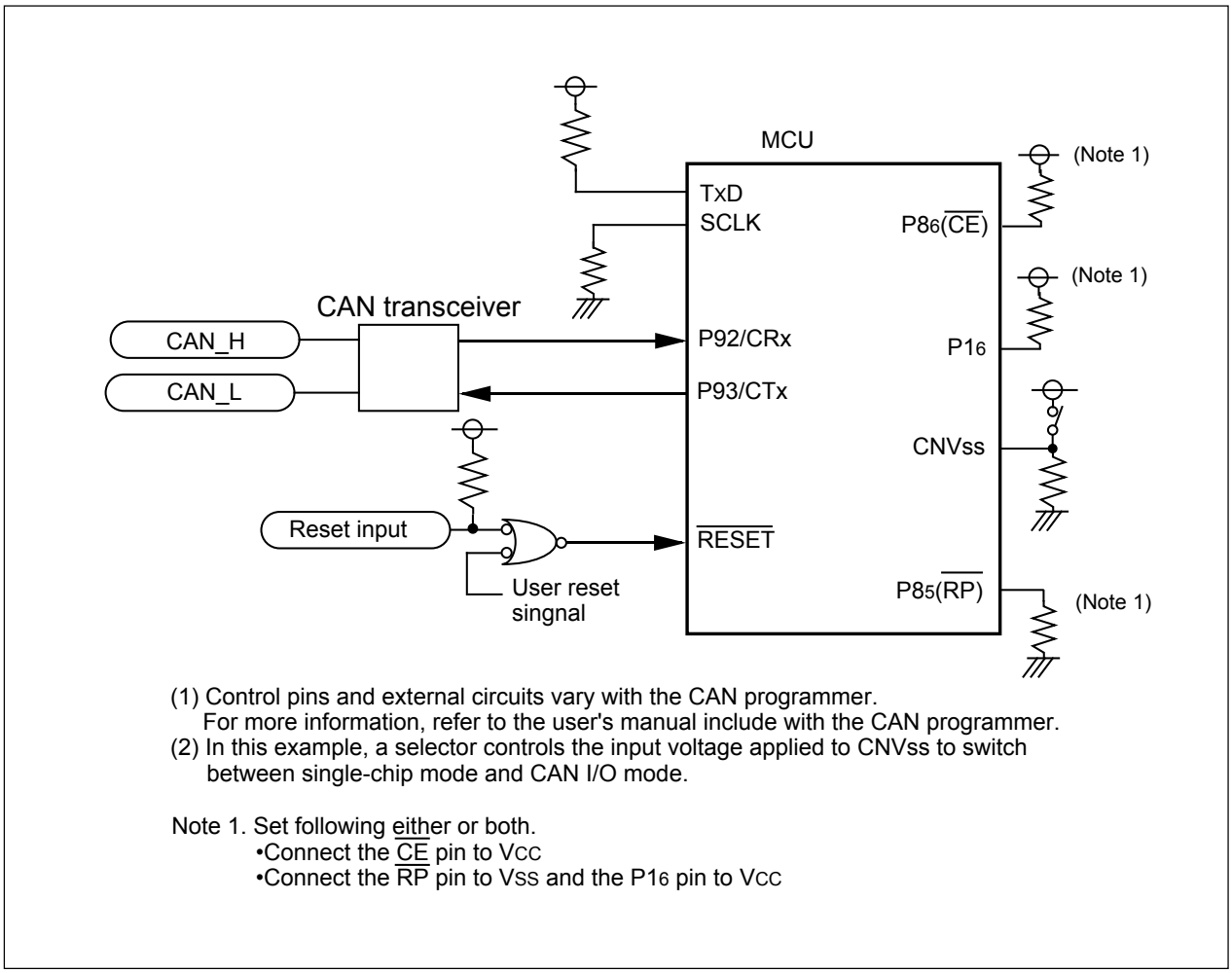
When an erase/program command is initiated, the CPU halts all program execution until the command operation is completed or erase-suspend request is generated.

When enabling an erase-suspend function, set the FMR40 bit to 1 (erase suspend enabled) and execute block erase commands. Also, the interrupt to transfer to erase-suspend must be set enabled preliminarily. When entering erase-suspend after td(SR-ES) from an interrupt is requested, interrupts can be accepted.

When an interrupt request is generated, the FMR41 bit is automatically set to 1 (suspend request) and an auto-erasing is suspended. If an auto-erasing has not completed (when the FMR00 bit is 0) after an interrupt process is completed, set the FMR41 bit to 0 (erase restart) and execute block erase commands again.

20.11.2 Example of Circuit Application in CAN I/O Mode

Figure 20.21 shows example of circuit application in CAN I/O mode. Refer to the user's manual for CAN programmer to handle pins controlled by a CAN programmer.



(1) Control pins and external circuits vary with the CAN programmer.
For more information, refer to the user's manual include with the CAN programmer.
(2) In this example, a selector controls the input voltage applied to CNVss to switch between single-chip mode and CAN I/O mode.

Note 1. Set following either or both.
•Connect the $\overline{CE}$ pin to V_{CC}
•Connect the $\overline{RP}$ pin to V_{SS} and the $P1_6$ pin to V_{CC}

Figure 20.21 Circuit Application in CAN I/O Mode

V_{CC} = 5V

Timing Requirements

(V_{CC} = 5V, V_{SS} = 0V, at Topr = – 20 to 85°C / – 40 to 85°C unless otherwise specified)

Table 21.23 Multi-master I^2C bus Line

Symbol	Parameter	Standard clock mode		High-speed clock mode		Unit
		Min.	Max.	Min.	Max.	
tBUF	Bus free time	4.7		1.3		µs
tHD;STA	The hold time in start condition	4.0		0.6		µs
tLOW	The hold time in SCL clock 0 status	4.7		1.3		µs
tR	SCL, SDA signals' rising time		1000	20+0.1Cb	300	ns
tHD;DAT	Data hold time	0		0	0.9	µs
tHIGH	The hold time in SCL clock 1 status	4.0		0.6		µs
tF	SCL, SDA signals' falling time		300	20+0.1Cb	300	ns
tSU;DAT	Data setup time	250		100		ns
tSU;STA	The setup time in restart condition	4.7		0.6		µs
tSU;STO	Stop condition setup time	4.0		0.6		µs

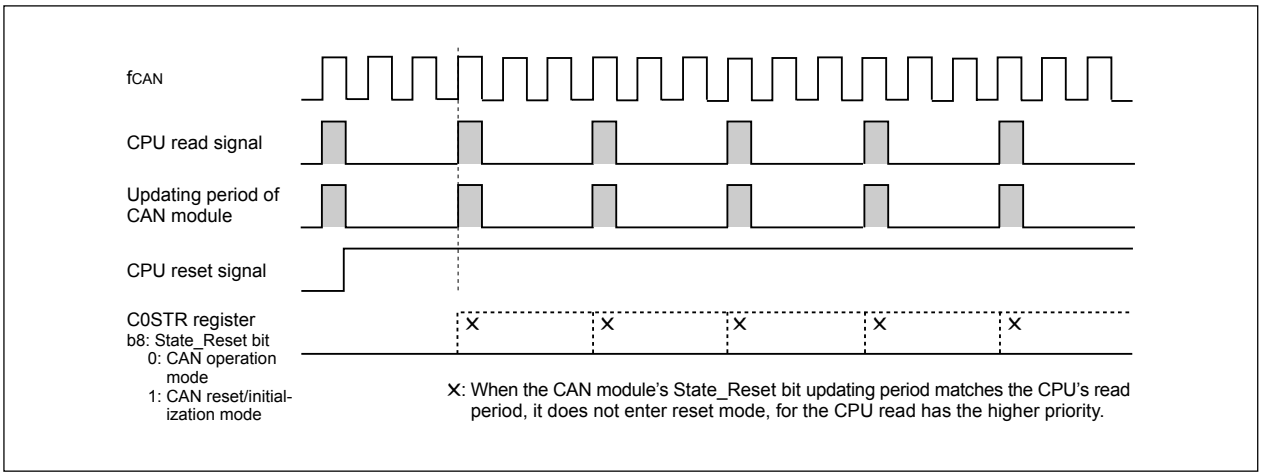


Figure 22.5 When Updating Period of CAN Module Matches Access Period from CPU

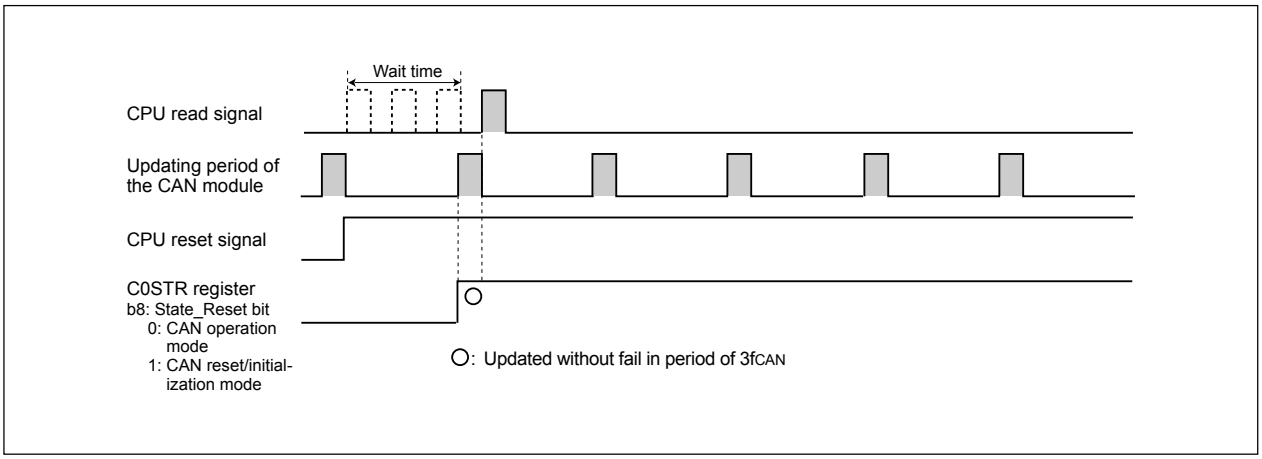


Figure 22.6 With a Wait Time of 3fCAN Before CPU Read

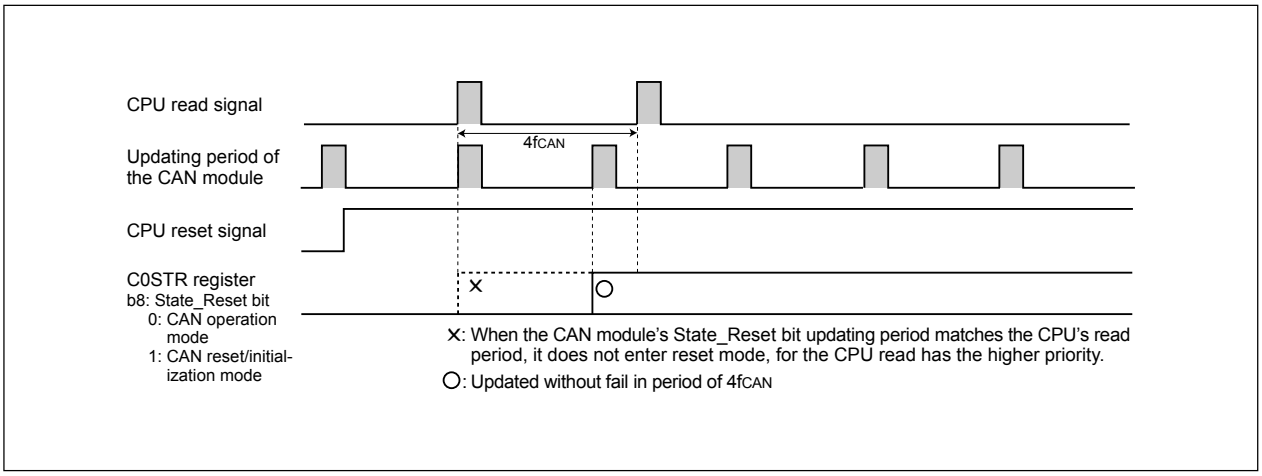


Figure 22.7 When Polling Period of CPU is 3fCAN or Longer